Microelectromechanical Configuration of an Optically Reconfigurable Gate Array

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Abstract—This paper presents a proposal of a novel optically reconfigurable gate array architecture with a microelectromechanical system (MEMS) mirror array that allows high-speed reconfiguration by exploiting large-bandwidth optical connections between the MEMS mirror array and a programmable gate array. The MEMS mirror array is used as a holographic memory. Four configuration contexts can be programmed electrically and dynamically onto the MEMS mirror array as holographic memory information. The configuration procedure is executed by switching both a laser array and an MEMS mirror array. This experiment demonstrated a four-context 146 ns microelectromechanical configuration for a programmable gate array. Sub-microsecond configuration is attainable.

Index Terms—Field-programmable gate arrays (FPGAs), microelectromechanical system (MEMS), optical interconnections, optical logic devices, optoelectronic devices.

I. INTRODUCTION

RECENTLY, demand for fast-context switching devices has increased. If circuit information can be programmed rapidly from memory to a gate array, then idle circuits can be removed. With such a configuration, only necessary circuits would need be programmed into the gate array at any one time, thereby increasing the gate array activity. As rapidly reconfigurable devices, optically reconfigurable gate arrays (ORGAs) have been developed that combine a holographic memory and an optically programmable gate array—very large scale integration (VLSI) [1]–[6]. In such a device, the gate array contexts are stored in a holographic memory, from which they are read out optically and programmed optically onto the gate array VLSI using photodiodes. Such a parallel configuration enables extremely fast reconfiguration. The reconfiguration time of such ORGA architecture reaches nanosecond-order [1]. In addition to date, 100 reconfiguration context implementations have been reported [2]–[4]. Consequently, huge virtual

gate quantities are attainable by exploiting the large storage capacity of a holographic memory.

However, a holographic memory with a large storage capacity is always an optically writable device. To rewrite it, a dedicated writer is required. Rewriting an ORGA is impossible while it is functioning, since its holographic memory is effectively read-only. However, among operations on ORGAs, some operations might require some optically applied parameters for a circuit. In this case, many configuration contexts are necessary for the single circuit since a configuration context must be allocated to each parameter of a circuit. Therefore, even if the number of configuration contexts of a future ORGA will be increased, the number must become insufficient to implement many circuits with many different parameters. Moreover, although an ORGA's gate array has a large bandwidth optical connection for reconfigurations, certain data given by an operation on an ORGA's gate array can not be transferred to its gate array using the optical connection because a transmission device or a holographic memory is read-only. For that reason, the optical advantage of an optoelectronic device cannot be extracted fully for data transfer. Therefore, future ORGAs must have some means to treat optically applied parameters in addition to an optical configuration capability.

To date, a liquid crystal spatial light modulator has been adapted for ORGAs [5], [6]. This device is an easily rewritable holographic memory. However, since the liquid crystal spatial light modulator's switching speed is very low—on the order of a dozen milliseconds—in previously proposed ORGAs, fast reconfiguration was achieved only by switching a laser array, not by switching a holographic memory. For that reason, a dozen milliseconds is too slow for preparation of parameters.

On the other hand, recently, as a new development of microelectromechanical system (MEMS) technology, a digital micromirror device (DMD) has been produced by Texas Instruments, Inc. (<http://dlp.com/>) [8]. The DMD chip is a type of spatial light modulator used in many video projectors. The switching speed and light efficiency far surpass those of other spatial light modulators such as liquid crystal spatial light modulators. Such devices are useful as electrically rewritable holographic memories.

This paper presents a new type of optically reconfigurable gate array with an MEMS binary hologram that is capable of exploiting both switching of a MEMS holographic memory and a laser array to achieve fast and flexible optical reconfigurations and optical parameter generations. This experiment

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Fig. 1. New concept of an optically reconfigurable gate array combining an optically read-only holographic memory with an electrically writable MEMS holographic memory.

Fig. 2. Block diagram of a MEMS optically reconfigurable gate array.

assesses a four-context 146 ns microelectromechanical configuration for a programmable gate array. Results show that sub-microsecond configuration is attainable.

II. MEMS ORGA ARCHITECTURE

A. Concept of a New ORGA Construction

Fig. 1 presents a new concept of an optically reconfigurable gate array combining an optically read-only holographic memory with an electrically writable MEMS holographic memory. This concept supports optical parameters in addition to optical reconfigurations. Here, the optical parameter means a certain constant data. For example, when implementing an image parallel processing operation onto an ORGA, some spatial filters—a smoothing filter, a Laplacian–Gaussian filter, user definition filters, and so on—are required [10]. Such filter data can be treated as a parameter. By separating the architecture of image processing and filtering parameters, a variety of operations can be realized. The ORGA comprises a gate array VLSI (ORGA-VLSI), an optically read-only holographic memory, an electrically writable MEMS holographic memory, and a laser diode array. The optically read-only holographic memory is used for storing numerous reconfiguration contexts by exploiting its large storage capacity. On the other hand, an electrically writable MEMS holographic memory is used for supplying a few optical parameters and/or optical reconfiguration contexts. A laser array is mounted on the top of both holographic memories for use in addressing the reconfiguration contexts on the optically read-only holographic

Fig. 3. Reconfiguration procedure when switching both a laser array and a MEMS device.

memory and parameters and reconfiguration contexts on the electrically writable MEMS holographic memory. One laser corresponds to a configuration context, a configuration context with a parameter, or a parameter. Of course, the parameter information of the electrically writable MEMS holographic memory can be superimposed to configuration context information stored on a read-only holographic memory by turning both corresponding lasers on. Therefore, a combination of any configuration context and any parameters is possible. Of course, a certain configuration context can be programmed onto the electrically writable MEMS holographic memory instead of parameters. For that reason, an implementation is realized in which a circuit itself generates a configuration context and in which the circuit itself is reconfigured similarly to Evolvable Hardware [7]. Therefore, this architecture is extremely useful for use in next-generation reconfigurable applications.

B. Demonstration System Overview of the New ORGA

Since this report describes a demonstration of the MEMS part only, Fig. 2 presents the overview of an experimental MEMS optically reconfigurable gate array. Here, the MEMS optically reconfigurable gate array has four configuration contexts as an example. However, the configuration contexts are not limited numerically to four in this architecture. The MEMS optically reconfigurable gate array consists of four lasers, a MEMS mirror array device used as a holographic memory, and a programmable gate array VLSI. The MEMS holographic memory is partitioned into four regions. Each region stores a configuration context, a configuration context with a set of parameters, or a set of parameters corresponding to one laser. The four reconfiguration contexts and/or a set of parameters on the MEMS holographic memory are addressed using four lasers. When a laser is turned on, the laser beam impinges on a single corresponding region on the MEMS holographic memory. Then, the corresponding region on the MEMS holographic memory generates a reconfiguration context and/or a set of parameters onto a photodiode-array of a gate array on an ORGA-VLSI chip. After reconfiguration, the gate array functions as a

circuit of the configuration context and/or a set of parameters. Laser-based reconfiguration is executed merely by switching a laser. In this case, this architecture enables nanosecond-order reconfiguration by exploiting the large bandwidth optical connections between MEMS holographic memory and the gate array of the ORGA-VLSI and using the rapid switching capability of lasers.

In addition, the MEMS holographic memory can be electrically programmed easily. Dynamic reconfiguration that exploits both switching of a MEMS holographic memory and a laser array can be executed using the following method. The reconfiguration procedure is presented in Fig. 3. Each laser turns on at the end of adjustment of the corresponding MEMS holographic memory region. The #4 configuration is executed by turning laser 1 at the end of adjustment of MEMS holographic memory region 1; the #5 configuration is executed by turning laser 2 at the end of adjustment of MEMS holographic memory region 2, and so on in turn. Switching of each MEMS holographic memory region is executed with 1/4 phase difference. During changes of the state of the region on the MEMS holographic memory, the other laser configurations can be executed continuously. Here, assuming the number of lasers as N , the response time of a MEMS holographic memory is T ; the average reconfiguration time is estimated as T/N . For that reason, once a MEMS holographic memory is programmed, up to N th configuration procedures can be executed within a nanosecond-order period by switching a laser array. Additionally, many configuration procedures can be executed constantly during the T/N period by switching both the laser array and MEMS. Therefore, this architecture is useful for treating flexible reconfigurations.

III. EXPERIMENTAL SYSTEM

A. Prototype ORGA-VLSI Chip

An ORGA-VLSI chip was fabricated using a $0.35\ \mu\text{m}$ triple-metal CMOS process [5]. The ORGA-VLSI chip consists of four logic blocks, five switching matrices, and 12 input/output (I/O) bits. The VLSI chip functionality is fundamentally identical to that of typical FPGAs. However, each programming element of all blocks of the ORGA-VLSI is connected to an optical reconfiguration circuit including a photodiode. For that reason, the gate array can be reconfigured optically. The total number of photodiodes is 340. The photodiode size and distance between photodiodes were designed, respectively, as $20.1\ \mu\text{m}$ and $18.9\ \mu\text{m}$ and as $90\ \mu\text{m}$. Each photodiode was constructed using a junction between the P-substrate and N-Well of a $0.35\ \mu\text{m}$ standard CMOS process. The gate array's gate count is 68. It has been confirmed experimentally that the ORGA-VLSI itself can be reconfigured in less than 10 ns.

B. MEMS Holographic Memory

Recently, as one MEMS technology, DMD have been developed by Texas Instruments Inc. [8], [9]. The device is called DLP; it is used in many video projectors. The DMD device chip is a type of spatial light modulator. Its specifications

TABLE I
SPECIFICATIONS OF A DIGITAL MIRROR ARRAY DEVICE

	0.55 XGA
Resolution	1024×768
Mirror tilt angle	12°
Mirror size	$10.8\ \mu\text{m}$
Package size (inch)	1.6×1.25

Fig. 4. Photograph of a MEMS holographic memory device.

are presented in Table I. In addition, a chip photograph is portrayed in Fig. 4. It consists of 1024×768 mirrors, each having a size of $10.8 \times 10.8\ \mu\text{m}^2$. The DMD device is controlled using a personal computer. When a light beam is applied onto the device, the mirrors on the DMD chip can reflect a binary data pattern with high speed and high efficiency far surpassing those of other spatial light modulators such as liquid crystal spatial light modulators. The micromirrors are mounted on tiny hinges, which enable them to tilt either toward the light source or away from it. Consequently, the DLP device has a more rapid switching capability than that of liquid crystal spatial light modulators. Such a device is useful as a holographic memory that is rewritable quickly and electrically.

C. Binary Holographic Memory Calculation Method for an MEMS Mirror Array Device

For these experiments, an MEMS mirror array device that has a binary state is assumed [8]. Therefore, the following calculation method is based on that of a 2-D binary holographic memory. A laser aperture plane, a holographic plane, and an ORGA-VLSI plane are parallelized. The laser beam is expanded. It is assumed that the aperture size is sufficiently wide for each holographic memory region. Consequently, the laser beam can be considered as a plane wave. The reference wave from the laser propagates into the holographic plane. The holographic medium comprises rectangular pixels on the x_1 - y_1 holographic plane. Each pixel is assumed as taking a binary value. On the other hand, the input object is made up of rectangular pixels on the x_2 - y_2 object plane. The pixels can also be modulated to be either on or off. The intensity distribution of a holographic medium is calculable using the

Fig. 5. Binary holographic memory pattern comprising 1024×768 pixels. The size of each pixel was designed as $10.8 \mu\text{m} \times 10.8 \mu\text{m}$. The holographic memory includes an XOR circuit at the upper left side, an AND circuit at the upper right side, an NAND circuit at the lower right side, and an OR circuit at the lower left side. The distance between holographic memory regions corresponding to circuits is two pixels.

following equation:

$$H(x_1, y_1) \propto \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} O(x_2, y_2) \sin(kr) dx_2 dy_2$$

$$r = \sqrt{Z_L^2 + (x_1 - x_2)^2 + (y_1 - y_2)^2}.$$
(1)

In (1), $O(x_2, y_2)$ is a binary value of a reconfiguration context, k is the wave number, and Z_L represents the distance between the holographic plane and the object plane. After the calculation shown above, the following threshold operation is done:

$$H'(x_1, y_1) = \begin{cases} 1 & H(x_1, y_1) > t \\ 0 & \text{otherwise.} \end{cases}$$
(2)

If the value $H(x_1, y_1)$ is larger than the threshold value t , then $H'(x_1, y_1)$ takes 1, and otherwise, 0. Finally, the image $H'(x_1, y_1)$ is used for implementing the holographic memory. Other areas on the holographic plane are opaque to the illumination.

D. Holographic Memory Pattern Generation

We assumed a four-context ORGA system. Each parameter was selected to fit the MEMS mirror array device and a fabricated ORGA-VLSI. Respective distances between photodiodes on ORGA-VLSI were set to $90 \mu\text{m}$ and $90 \mu\text{m}$. Each configuration context consists of 20×17 pixels. On the other hand, a holographic memory pattern was constructed by 1024×768 pixels. The size of each pixel is $10.8 \mu\text{m} \times 10.8 \mu\text{m}$. Using the conditions described above, a MEMS holographic memory pattern was calculated using (1) and (2), as presented in Fig. 5. Each value of pixels takes a binary value of H or L. The holographic memory includes an XOR circuit at the upper left side, an AND circuit at the upper right side, an NAND circuit at the lower right side, and an OR circuit at the lower left side. Each region consists of 300×300 pixels. The distance between holographic memory

(a)

(b)

(c)

(d)

Fig. 6. Photographs of the experimental system. Panels (a) and (b) show top view photographs. Panels (c) and (d) show side view photographs.

regions corresponding to circuits is two pixels. The distance between the ORGA-VLSI and MEMS holographic memory is 100 mm.

Fig. 7. CCD captured images of configuration contexts of: (a) XOR circuit; (b) AND circuit; (c) NAND circuit; and (d) OR circuit at the position of an ORGA-VLSI. The XOR circuit, the AND circuit, the NAND circuit, and the OR circuit were generated, respectively, from the upper left side region, the upper right side region, the lower right side region, and the lower left side region of a MEMS holographic memory.

E. Experimental System

Fig. 2 portrays a block diagram of a MEMS optically reconfigurable gate array. Fig. 6 shows photographs of the MEMS optically reconfigurable gate array. The MEMS optically reconfigurable gate array was constructed using a 532 nm, 300 mW laser (torus 532; Laser Quantum), a MEMS holographic memory, and an ORGA-VLSI. The laser was shared and used as emulating four lasers. The holographic memory pattern shown in Fig. 5 is electrically programmed onto the MEMS holographic memory through a personal computer. The MEMS holographic memory consists of 1024×768 pixels, each having a size of $10.8 \times 10.8 \mu\text{m}^2$, which was provided by Texas Instruments Inc. [8]. After programming, all mirror angles on the MEMS holographic memory were adjusted depending on the holographic memory pattern of Fig. 5. The beam from the laser source, the diameter of which is 1.7 mm. The collimated beam is incident to the MEMS holographic memory. Then, the beam is reflected to the ORGA-VLSI. The ORGA-VLSI was placed at a distance of 350 mm from the MEMS holographic memory.

IV. EXPERIMENTAL RESULTS

Using the experimental system explained above, an XOR circuit, an AND circuit, an NAND circuit, and an OR circuit were implemented on the system. The holographic memory pattern shown in Fig. 5 was implemented onto an MEMS holographic memory. The holographic memory pattern includes information of four circuits: an XOR circuit, an AND circuit, a NAND circuit, and an OR circuit. Such circuits were implemented on one logic block, one switching matrix and three I/O bits, as shown in Fig. 9(a). The detailed logic block, switching matrix, and I/O block structures are shown, respectively, in Figs. 9(b), (c), and (d) [5]. The charge-coupled

Fig. 8. Configuration context maps of: (a) XOR circuit; (b) AND circuit; (c) NAND circuit; and (d) OR circuit which correspond to CCD captured images in Fig. 7. The map shows a 20×17 photodiode array. The LB, SM, and IOB stands for a logic block, a switching matrix, and an I/O bit, respectively. The corresponding photodiodes can be found in Fig. 9(b), (c), and (d).

device (CCD) captured images of configuration contexts of the XOR circuit, the AND circuit, the NAND circuit, and the OR circuit at the position of the ORGA-VLSI are portrayed in Fig. 7(a), (b), (c), and (d), which were generated, respectively,

Fig. 9. Gate array structure. (a) 2 input-1 output circuit implementation. (b) Logic block. (c) Switching matrix. (d) I/O block.

from the upper left side region, the upper right side region, the lower right side region, and the lower left side region of the MEMS holographic memory. The corresponding configuration context maps are portrayed in Fig. 8. The map shows a 20×17 photodiode array. LB, SM, and IOB, respectively, stand for a logic block, a switching matrix, and an I/O bit. The corresponding photodiodes can be found in Fig. 9(b), (c), and (d), respectively. Such configuration context patterns were

Fig. 10. Timing diagrams of reconfiguration procedures of: (a) XOR circuit; (b) AND circuit; (c) NAND circuit; and (d) OR circuit. The reconfiguration times were measured as 146 ns. In time scale at the bottom of each plot, 0 μs means the end of each configuration procedure. After the configuration end, each circuit works correctly.

programmed onto an ORGA-VLSI in turn. The product of the photodiode response time $T_{\text{reconfiguration}}$ on the ORGA-VLSI and laser power P_{Laser} necessary for each photodiode was measured as $T_{\text{reconfiguration}} \cdot P_{\text{Laser}} = 0.77 \text{ pJ}$ (532 nm). Therefore, the diffraction efficiency of the MEMS holographic configuration including all optical component losses were estimated as 0.0176–0.0211%. When using a liquid crystal

Fig. 11. Response time of a MEMS mirror array device. The turn-on time is 22 μ s, the turn-off time is 12 μ s. (a) Rising time. (b) Falling time.

holographic memory, the diffraction efficiency was reported as about 0.05% [1]. On the other hand, in the case of using a photopolymer-type holographic memory, the diffraction efficiency was estimated about 0.06% [11]. Therefore, the diffraction efficiency of the MEMS holographic memory is lower than that of the other holographic memories. However, the effect is not large. A slightly powered-up laser can recover from such a low-diffraction-efficiency problem.

The timing diagrams of laser-based reconfiguration procedures are portrayed in Fig. 10(a)–(d). The four laser-based configuration procedures were executed. Laser-based reconfiguration times were measured as 146 ns using a 4 GHz oscilloscope [54854A; Agilent Technologies, Inc. (<http://www.chem.agilent.com/en-US/Pages/Homepage.aspx>)]. Consequently, the experiments show that the four-context MEMS ORGA architecture supports very high-speed reconfiguration by switching a laser array.

Additionally, we have estimated the switching speed of mirrors on the MEMS holographic memory. Experimental results are presented in Fig. 11. The turn-on and turn-off times were measured, respectively, as 12 μ s and 22 μ s. Results confirmed that a less than 22 μ s refresh cycle or MEMS-based reconfiguration cycle is possible. Therefore, the MEMS ORGA can be reconfigured in 146 ns up to four configuration contexts by switching a laser array and can be reconfigured constantly and electrically in less than 7.3 μ s by switching a MEMS device.

V. CONCLUSION

This paper has presented a novel optically reconfigurable gate array architecture with a MEMS mirror array allowing 146 ns high-speed reconfiguration and flexible reconfiguration by both switching of an electrically rewritable MEMS holographic memory and a laser array. This experiment has demonstrated a four-context 146 ns microelectromechanical configuration for a programmable gate array. Results show that sub-microsecond configuration is attainable. A new rapidly reconfigurable and electrically reconfigurable device can be developed.

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