A Study on Clock Skew Calibration for Time-interleaved A/D Converters and Time-Resolved CMOS Image Sensors

（課程博士・様式７）（Doctoral qualification by coursework,Form 7）

学 位 論 文 要 旨

Abstract of Doctoral Thesis

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論文題目：　インターリーブ型 A/D 変換器と時間分解型 CMOS イメージセンサのクロックスキュー補正に関する研究

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論文要旨：

Abstract：The clock skew causes a lot of problems both in time-interleaved analog-to-digital converters (TiADCs) and time-resolved (TR) CMOS image sensors. This thesis studies the clock skew in TiADCs and TR CMOS image sensors, the clock skew calibration methods are proposed and their effectiveness are demonstrated for these two devices.

First, the TiADCs are considered to achieve high speed and high resolution data conversion by using several channels of ADCs working in parallel, the pipeline based TiADC is widely used in wireless communication systems. However, the TiADCs are sensitive to the mismatches due to process, voltage and temperature variations. Each of the sub-ADCs may have a different gain error, offset, and clock skew. Mismatches between the channels cause large distortion and decrease the system performance. The clock skew because of different delay between channels causes sampling error in sample-and-hold (S/H) circuits in sub-ADCs and the sampling error becomes serious when input signal frequency is much higher. In order to calibrate the clock skew, a new approach of simple clock skew measurement and calibration circuit used in S/H stages is proposed. The proposed clock skew measurement technique is a new method using an analog-based delay-locked loop (DLL) and a common bang-bang phase detector (BPD). In order to investigate the effectiveness of proposed clock skew calibration circuits, a 2-channel 200 MHz time-interleaved S/H circuits for 12-bit pipeline based TiADC is designed using 65-nm CMOS technology. The simulation results show the improvement of spurious-free dynamic range (*SFDR*) value after skew calibration by 19.6 dB at Nyquist frequency.

Second, the TR CMOS image sensors have recently been paid much attention in applications

of time-of-flight (TOF) range imaging, biological imaging, and so on. A state-of-the-art TOF range imager has demonstrated the high range resolution of 0.3 mm, which corresponds to time resolution of 2 ps. Higher time resolution is strongly required for extending the application area of TOF range imagers. In TR CMOS image sensors, a gating clock is supplied to pixels by column-parallel clock drivers. Because the clock driver has to drive a large capacitance due to a large number of gates in one pixel column, a large clock skew because of different delay may occur between columns. The clock skew includes both random and systematic components, which are mainly due to device mismatches (especially clock drivers) and a voltage drop of power supply line, respectively. As the time resolution of TR imagers increases, for example, TR imager with high time resolution such as sub-millimeter range, a clock skew of gating clock between pixels becomes a serious problem, because the clock skew causes the reduction of measurable maximum range in particular pixels or unmeasurable pixels. To address this problem, an electronic-only column-parallel clock skew self-calibration circuit is proposed. The proposed clock skew calibration technique is a method of digital-based DLL, it uses a coarse-fine two-stage delay line for each column and a dual low-skew clock tree for supplying skew-corrected gating pulses to a pixel area. The two-stage delay line comprised with voltage-controlled delay line (VCDL) and digitally-controlled delay line (DCDL) covers a wide calibration range with high resolution. The dual low-skew clock tree technique is essential for controlling clock skews of all the pixels within a specified tolerance range of skews. This technique is effective for embedding the skew calibration circuit unit in the small pixel pitch while attaining the specified accuracy of skew calibrations. For a proof of concept, a typical TOF range image sensor with the proposed clock skew calibration circuitry is designed and implemented in 0.11-μm CMOS image sensor (CIS) technology. The experimental results show that the clock skew calibration circuit successfully reduces the clock skew from 247 ps_{rms} to 25 ps_{rms}. The calibration time is 12 μs which is much faster than 1-9 hrs of previous work. This technique can widely be used for TR CMOS image sensors.