A Study on Clock Skew Calibration for Time-interleaved A/D Converters and Time-Resolved CMOS Image Sensors

THESIS

A Study on Clock Skew Calibration for Time-interleaved A/D Converters and Time-Resolved CMOS Image Sensors

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A Study on Clock Skew for Time-Interleaved A/D Converters and Time-Resolved CMOS Image Sensors

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Abstract

The clock skew causes a lot of problems both in time-interleaved analog-to-digital converters (TiADCs) and time-resolved (TR) CMOS image sensors. This thesis studies the clock skew in TiADCs and TR CMOS image sensors, the clock skew calibration methods are proposed and their effectiveness are demonstrated for these two devices.

First, the TiADCs are considered to achieve high speed and high resolution data conversion by using several channels of ADCs working in parallel, the pipeline based TiADC is widely used in wireless communication systems. However, the TiADCs are sensitive to the mismatches due to process, voltage and temperature variations. Each of the sub-ADCs may have a different gain error, offset, and clock skew. Mismatches between the channels cause large distortion and decrease the system performance. The clock skew because of different delay between channels causes sampling error in sample-and-hold (S/H) circuits in sub-ADCs and the sampling error becomes serious when input

signal frequency is much higher. In order to calibrate the clock skew, a new approach of simple clock skew measurement and calibration circuit used in S/H stages is proposed. The proposed clock skew measurement technique is a new method using an analog-based delay-locked loop (DLL) and a common bang-bang phase detector (BPD). In order to investigate the effectiveness of proposed clock skew calibration circuits, a 2-channel 200 MHz time-interleaved S/H circuits for 12-bit pipeline based TiADC is designed using 65-nm CMOS technology. The simulation results show the improvement of spurious-free dynamic range (*SFDR*) value after skew calibration by 19.6 dB at Nyquist frequency.

Second, the TR CMOS image sensors have recently been paid much attention in applications of time-of-flight (TOF) range imaging, biological imaging, and so on. A state-of-the-art TOF range imager has demonstrated the high range resolution of 0.3 mm, which corresponds to time resolution of 2 ps. Higher time resolution is strongly required for extending the application area of TOF range imagers. In TR CMOS image sensors, a gating clock is supplied to pixels by column-parallel clock drivers. Because the clock driver has to drive a large capacitance due to a large number of gates in one pixel column, a large clock skew because of different delay may occur between columns. The clock skew includes both random and systematic components, which are mainly due to device mismatches (especially clock drivers) and a voltage drop of power supply line, respectively. As the time resolution of TR imagers increases, for example, TR imager with high time resolution such as sub-millimeter range, a clock skew of gating clock between pixels becomes a serious problem, because the clock skew causes the reduction of measurable maximum range in particular pixels or unmeasurable pixels. To address this problem, an electronic-only column-parallel clock skew self-calibration circuit is proposed. The proposed clock skew calibration technique is a method of digital-based DLL, it uses a coarse-fine two-stage delay line for each column and a dual low-skew clock tree for supplying skew-corrected gating pulses to a pixel area. The two-stage delay line comprised with voltage-controlled delay line (VCDL) and digitally-controlled delay line (DCDL) covers a wide calibration range with high resolution. The dual low-skew clock tree technique is essential for controlling clock skews of all the pixels within

a specified tolerance range of skews. This technique is effective for embedding the skew calibration circuit unit in the small pixel pitch while attaining the specified accuracy of skew calibrations. For a proof of concept, a typical TOF range image sensor with the proposed clock skew calibration circuitry is designed and implemented in 0.11-μm CMOS image sensor (CIS) technology. The experimental results show that the clock skew calibration circuit successfully reduces the clock skew from 247 ps_{rms} to 25 ps_{rms}. The calibration time is 12 μs which is much faster than 1-9 hrs of previous work. This technique can widely be used for TR CMOS image sensors.

Declaration

The work in this thesis is based on research carried out at the Imaging Devices Laboratory, Research Institute of Electronics, Shizuoka University. No part of this thesis has been submitted elsewhere for any other degree or qualification and it all my own work unless referenced to the contrary in the text.

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Chapter 1

Introduction

1.1 Background

In Japan, from June 2011, the analog signal TV broadcasting has been stopped and changes to digital signal. The most popular electronic products in our daily life such as notebook, smart phone, tablets, digital camera, and digital TV etc. are based on digital signal and digital-signal-process (DSP).

But the signals in the real nature, such as sound, light, temperature etc. are almost analog signals. So, how to make a connection between the real nature and the digital world?

What we need is just a “bridge”! The analog-to-digital converters (ADCs) were born to be the role of this “bridge”, an ADC is a device that converts an input analog voltage or current to a digital number proportional to the magnitude of the voltage or current as shown in Fig.1.1. The ADCs play an extremely important role in electronic field, and the technology advancements have been a strong driving force for the development of ADCs.

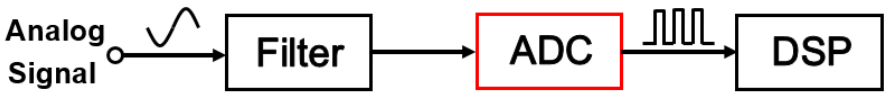

Fig.1.1. Analog-to-digital converter.

Main types of ADCs and their application are shown in Fig.1.2. The ADCs are classified by the sample rate and resolution. Different type of ADCs could be applied

in different area. The ADC with high sample rate (from several ten MHz to several thousand MHz) and low resolution (from 4 bits to 8 bits) such as flash ADC are used in HDD or DVD system. The ADCs with high sample rate (from several ten MHz to several hundred MHz) and high resolution (from 10 bits to 16 bits) such as pipeline ADC are widely used in video, communications, flat-panel displays and imaging signal processing applications.

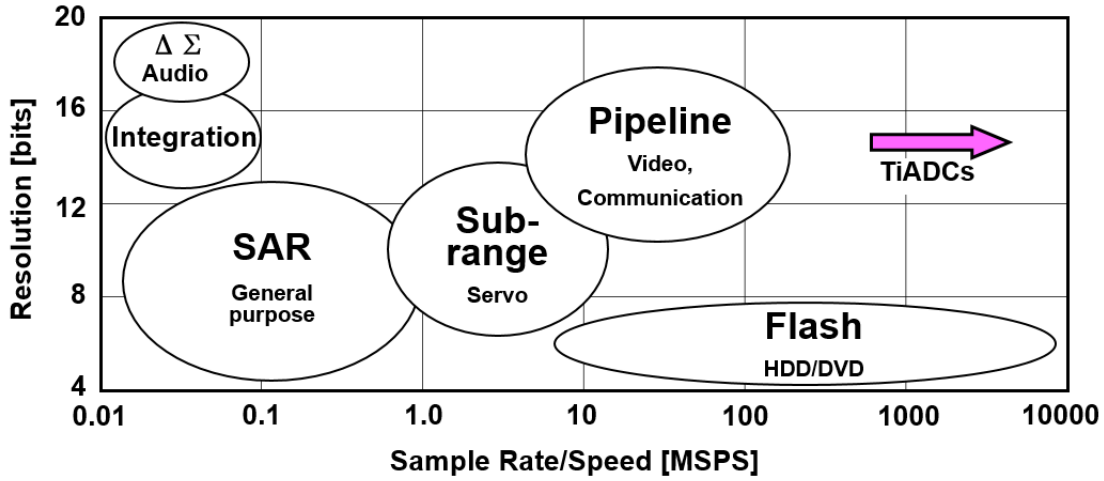

Fig.1.2. The ADCs and their applications.

Because of the big growth of mobile terminal products and environmental protection, low power consumption electronic products are strongly desired even than before. The trends to the battery powered portal digital devices also make the low power consumption more and more important in circuit design.

Fig.1.3 shows the evolution of handset converters in modern wireless communication system. For better communication system, higher sample rate and high resolution ADCs are strongly required. Although trade-offs are usually unavoidable, it is a big challenge for engineers to design high speed, high resolution and low power consumption ADC in one chip.

This research is interested in development of high speed and high resolution ADCs. For the purpose of higher sample rate, pipeline ADC based time-interleaved ADC

(TiADC) is universally used. TiADCs were introduced by Black and Hodges [1], Fig. 1.4 shows a simplified block diagram of an M-channel ($M = 2^N$, and N is an integer) TiADC. A pipeline ADC based TiADC is a useful architecture for realizing very high sample rate but remaining same high resolution as pipeline ADC [2]. And researches also show that due to the sample rate, TiADC could reduce the power consumption ($Power/f_s$) to lower than half of that of pipeline ADC when the sample rate is higher than 100 MHz [3] as shown in Fig. 1.5. Because the higher sample rate requires high-gain high-speed amplifier in pipeline ADC, and the high-gain high-speed amplifier always require high power consumption. But the entire sample rate can be divided by M when using the TiADC structure which in each channel the sub-ADCs is working in low speed.

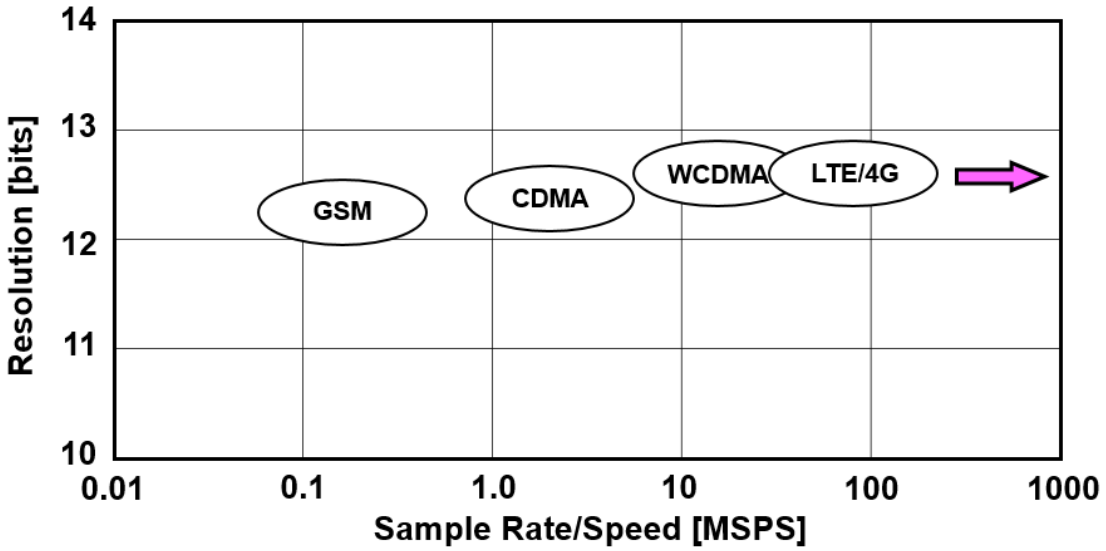

Fig.1.3. Evolution of handset converters.

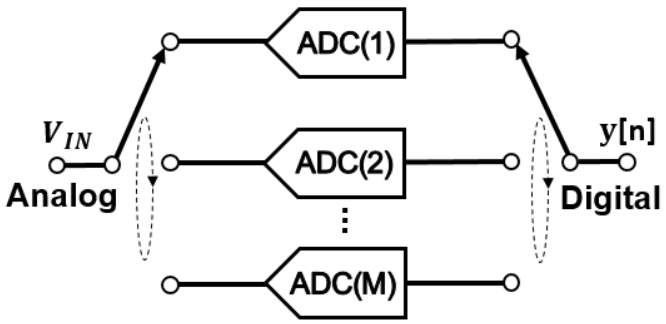

Fig.1.4. Simplified block diagram of TiADCs.

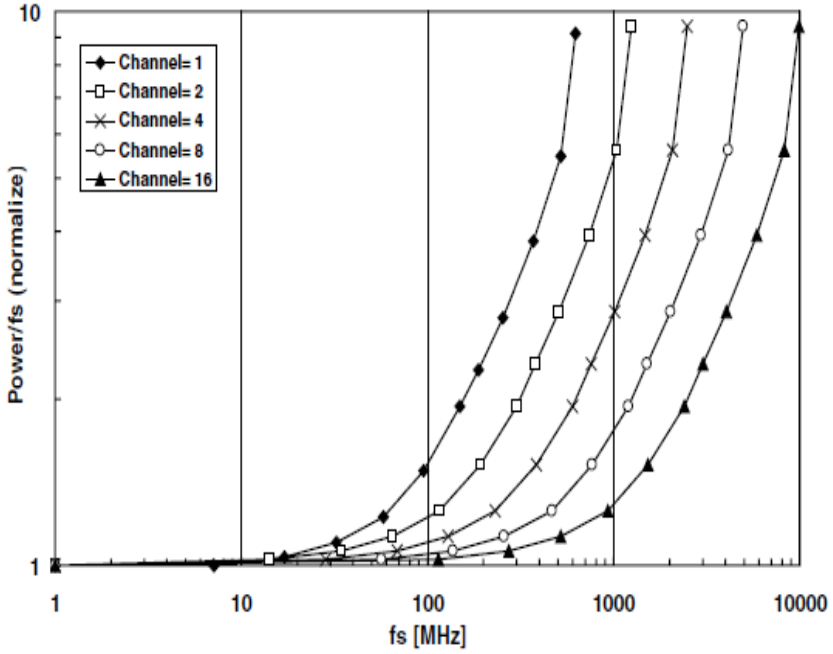

Fig.1.5. *Power/f_s* in pipeline ADC and TiADC. [3]

But to use the TiADC architecture in a high-speed high-resolution ADC，a special design consideration is necessary. The TiADC architecture is sensitive to mismatches due to process, voltage and temperature variations. Each of the ADC may have a different gain error, offset, and clock skew [4]. Mismatches between the channels cause large distortion and decrease the system performance. The clock skew because of different delay between channels causes sampling error and the sampling error becomes serious when input signal frequency is much higher.

On the other hand, time-resolved (TR) CMOS image sensors have recently been paid much attention in applications of time-of-flight (TOF) range imaging [5, 6, 7, 8], biological imaging [9, 10, 11], and so on. The TOF range image sensors are applied in a lot of area due to the range and resolution, such as automotive security (range: kilometer, resolution: meter), game gesture recognition and 3D scanner (range several millimeter, resolution: micrometer) as shown in Fig.1.6. A state-of-the-art TOF range image sensor [8] has demonstrated the high range resolution of 0.3 mm, which corresponds to time resolution of 2 ps. As shown in Fig.1.7, an application of TR CMOS imager in fluorescence lifetime imaging microscopy (FLIM), the fluorescence lifetime of

nanosecond order has been measured with the resolution of sub-nanosecond.

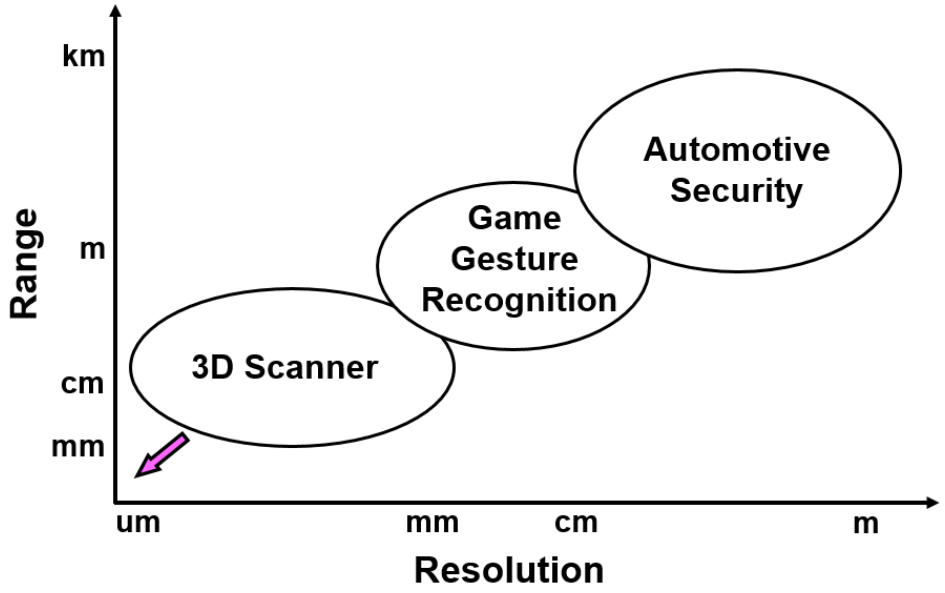

Fig.1.6. Applications of TOF range imagers.

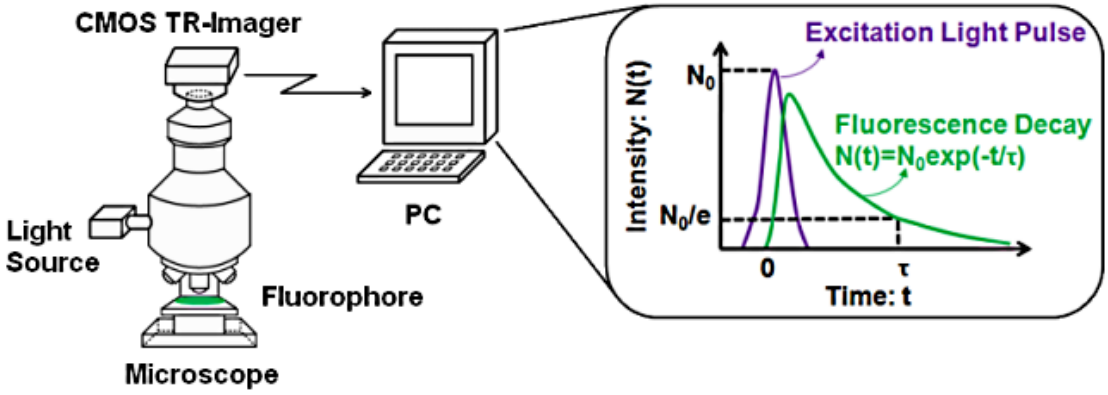

Fig.1.7. Applications of TR imager in FLIM [9].

Higher time resolution is strongly required for extending the application area of TR CMOS image sensors, especially for TOF range imagers. In TR CMOS imagers, a gating clock is supplied to pixels by column-parallel clock drivers. Because the clock driver has to drive a large capacitance due to a large number of gates in one pixel column, a large clock skew because of the different delay may occur between columns. The skew includes both random and systematic components, which are mainly due to device mismatches

(especially clock drivers) and a voltage drop of power supply line, respectively. The systematic skew due to the power-supply voltage drop of a clock driver is dominant according to [8]. As the time resolution increases, especially in TR imager with high time resolution such as sub-millimeter range resolution, if the skew is comparable or larger than the measurable range, each pixel has a different measureable range. Thereby, simultaneous capturing for all the pixels cannot be achieved [8].

1.2 Motivation and Objectives

In TiADCs, the time-varying errors are caused by clock skew, bandwidth mismatch, jitter, offset and gain mismatch [12]. The sampling error as a result of clock skew becomes serious when input signal frequency is much higher. Although in reality all mismatches are presented, for simplify, this study focuses on the clock skew but the gain mismatch and offset are set to zero.

There are many papers which have studied the clock skew calibration techniques for TiADCs, the proposed method is compensating or reducing the clock skew as following.

First, a TiADC can be made insensitive to the effect of timing skew by adding a single front-end sample-and-hold amplifier (SHA) in the front of the sub-ADC array [13, 14], where the front-end SHA works at the aggregate clock frequency. As shown in Fig.1.8, the front-end SHA creates staircase waveforms at the inputs of the sub-ADCs, then the SHAs of sub-ADCs sample a nearly constant voltage and can accept some skew in its sampling point. But this solution tends to be only practical in moderate speed designs due to full speed of the converter for the front-end SHA and the additional power consumption due to high-speed operation and high-gain operational amplifier driving a large capacitance load in sample-and-hold (S/H) circuit.

Second, a method is using low-skew clock generator [15, 16] for S/H circuits. In [15], a low-jitter skew-calibrated delay-locked loop (DLL) based multi-phase clock generator is introduced. In [16], a dual-channel pipeline ADC without channel mismatch calibration is introduced, a single clock-edge sampling named technique is used for the clock skew calibration, it uses a phase detector and a delay cell for one of the sampling clock.

Third, in [17, 18], a global passive sampling technique is used for the skew insensitive sampling, but this method cause large parasitic capacitance due to additional switch components and the global sampling timing reduces the sampling period of S/H circuits.

Fourth, some clock skew calibration techniques detect clock skew by using a ramp calibration signal has been reported in [19, 20], but the calibration depends on the slope

of the ramp calibration signal and it is not easy way to generate the high frequency ramp calibration signal.

The other clock skew compensating techniques based on digital phase detector for skew measurement have been reported. The first technique works in the full digital domain, employing a digital processor at the outputs of the sub-ADCs [21], as shown in Fig.1.9. As shown in Fig.1.10, the second technique follows a mixed-signal approach [22, 23], it uses a digital processor to detect certain characteristics of the discrete-time output and then adjusts analog circuits to eliminate the effects of timing skew. Both of these two techniques use the digital processer to detect the clock skew, but the first technique suffers from the large at-speed computation burden of a fully digital approach and the second technique requires complex mix-signal designing.

In this study, a new simple and effective clock skew calibration approach is proposed. The proposed skew calibration technique is a method of analog-based DLL and the calibration circuit operates in the S/H stage only.

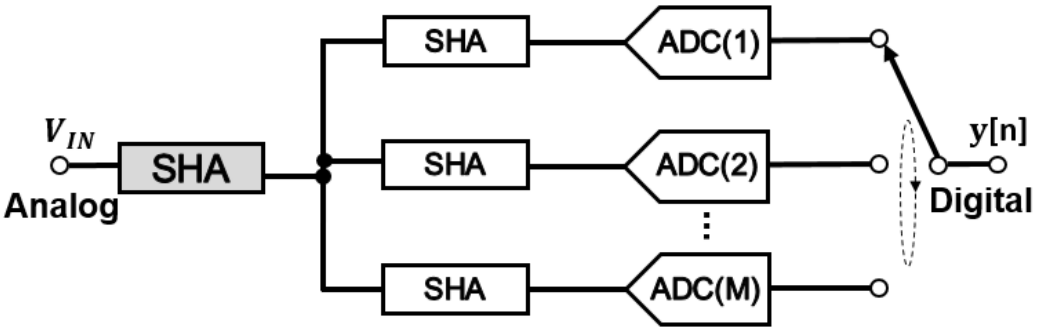

Fig.1.8. TiADCs with a front-end sample-and-hold amplifier.

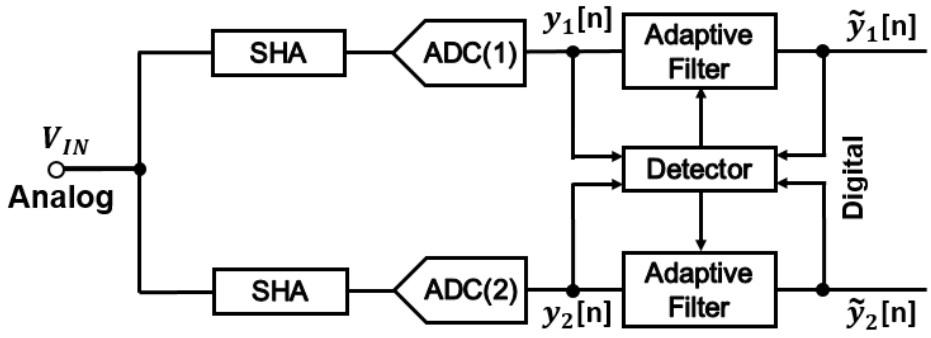

Fig.1.9. Digital timing clock skew correction.

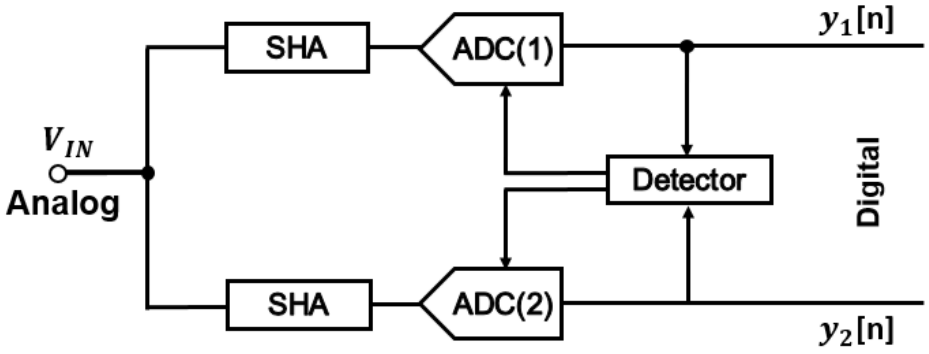

Fig.1.10. Mixed-signal clock skew correction.

On the other hand, in order to address the clock skew problem in TR CMOS image sensors, column-parallel skew calibration circuit has been proposed and demonstrated its effectiveness [8]. However, the calibration procedure takes a lot of time, because the delay characteristics of the skew calibration circuits are measured by using optical response and approximately 10^5 to 10^6 measurements or 1 to 9 hours are required for the skew calibration when the frame rate is 30 fps. Electronics-only self-calibration techniques are desired for reduced calibration time and the calibration cost. Moreover, the clock skew calibration techniques used in the TiADCs targeted for relatively small number of channels are not suitable for the column-parallel multi-channel skew calibration in TR CMOS image sensors which have typically more than 100 columns.

In this thesis, a new electronics-only column-parallel multi-channel clock skew self-calibration circuit for TR CMOS image sensors is presented. The proposed clock skew calibration technique is a method of digital-based DLL.

1.3 Organization of the Thesis

This thesis includes 5 chapters. The chapters are organized as following. In Chapter 2, an overview of pipeline ADC based TiADC and TR CMOS image sensors are introduced. First, the fundamental knowledge of pipeline ADC, the S/H circuit and amplifier are introduced. The static and dynamic characteristics of ADC also been introduced. The mismatches which include clock skew are discussed in brief. Second, the TR CMOS image sensor is introduced and the clock skew in TR CMOS image sensor is discussed in short.

In Chapter 3, a proposed method of clock skew calibration for TiADCs is given. TiADCs are considered to achieve high speed and high resolution data conversion by using M-channel low-speed ADCs worked in parallel. However, the TiADCs are sensitive to the mismatches between the channels. The clock skew because of different delay between channels is caused by the mismatch due to process, voltage and temperature variations and it degrades the system performance. The sampling error due to the clock skew becomes serious when input signal frequency is much higher. In order to calibrate the clock skew, a new approach of clock skew measurement and calibration circuit is proposed. To investigate the effectiveness of proposed clock skew calibration in TiADCs, a 2-channel 200 MHz time-interleaved S/H circuits for 12-bit pipeline ADC based TiADC is designed using 65-nm CMOS technology. The simulation results show the improvement of spurious-free dynamic range (*SFDR*) value of 2-channel interleaved S/H circuits without and with skew calibration by 19.6 dB at Nyquist frequency. The simulation results investigate the effectiveness of the proposed clock skew calibration circuit in TiADCs.

In Chapter 4, the electronics-only column-parallel multi-channel clock skew self-calibration circuit for TR CMOS image sensors is studied in detail. TR CMOS image sensors have recently been paid much attention in applications of TOF range imaging, biological imaging, and so on. In TR CMOS image sensors, a gating clock is supplied to

pixels by column-parallel clock drivers. Because the clock driver has to drive a large capacitance due to a large number of gates in one pixel column, a large clock skew because of different delay may occur between columns. The clock skew includes both random and systematic components, which are mainly due to device mismatches (especially clock drivers) and a voltage drop of power supply line, respectively. As the time resolution of TR CMOS imagers increases, a skew of gating clock between pixels becomes a difficult problem, because the clock skew causes the reduction of measurable maximum range in particular pixels or unmeasurable pixels. To address the problem, an optical response method is proposed in [8], but the calibration takes a lot of time and cost. To calibrate the skew in short time, an electronic-only column-parallel multi-channel clock skew self-calibration circuit based on coarse-fine two-stage delay line and a dual low-skew clock tree is proposed. For a proof of concept, an particular TOF range image sensor with the proposed skew calibration circuitry is designed and implemented in 0.11-μm CMOS image sensor (CIS) technology, and the experimental results show that the skew calibration circuit successfully reduces the clock skew from 247 ps_{rms} to 25 ps_{rms}, and the calibration time is only 12 μs, which is much faster than the previous work [24].

In Chapter 5, a conclusion of this thesis is discussed.

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Chapter 2

Overview of Time-Interleaved A/D Converters and Time-Resolved CMOS Image Sensors

In this chapter, the time-interleaved analog-to-digital converters (TiADCs) and time-resolved (TR) CMOS image sensors are introduced. First, the fundamental knowledge of pipeline ADC, the sample-and-hold (S/H) circuit and amplifier are introduced. The ADC performance also be introduced [1, 2, 3, 4, 5, 6, 7]. The pipeline ADC based TiADC and the mismatches including clock skew between the channels are introduced. Second, the TR CMOS image sensors are introduced and the clock skew in TR CMOS image sensors is discussed.

2.1 Introduction to Pipeline ADC

Pipeline ADC has the advantage of high sample rate and high resolution, it is widely used in video and communication area. Fig.2.1 shows the block diagram of a 1.5 b/stage pipeline ADC. In the front of pipeline ADC, there is an S/H stage, the analog input signal is sampled and held by the S/H circuit. The following ADC stages convert the stored

analog signal in the S/H stage to digital code. Every ADC stage has same structure including an S/H circuit, a sub-ADC, a digital-to-analog converter (DAC) and a residue amplifier. Different from the main S/H stage, the S/H circuits in ADC stages sample and hold the residue signal from the previous stage. At the transient when end of sampling, the sub-ADC converts the sampled signal into a 2-bit digital code, the code is inverted to analog signal by the DAC for residue calculation. After residue amplifier, the residue value is amplified by *2* for converting in the next stage. When the data converting of last stage is ended, the digital collection is active, the codes from every stage are collected. Since the codes from every ADC stage are not available at the same time, alignment circuits are added for reading out the digital codes.

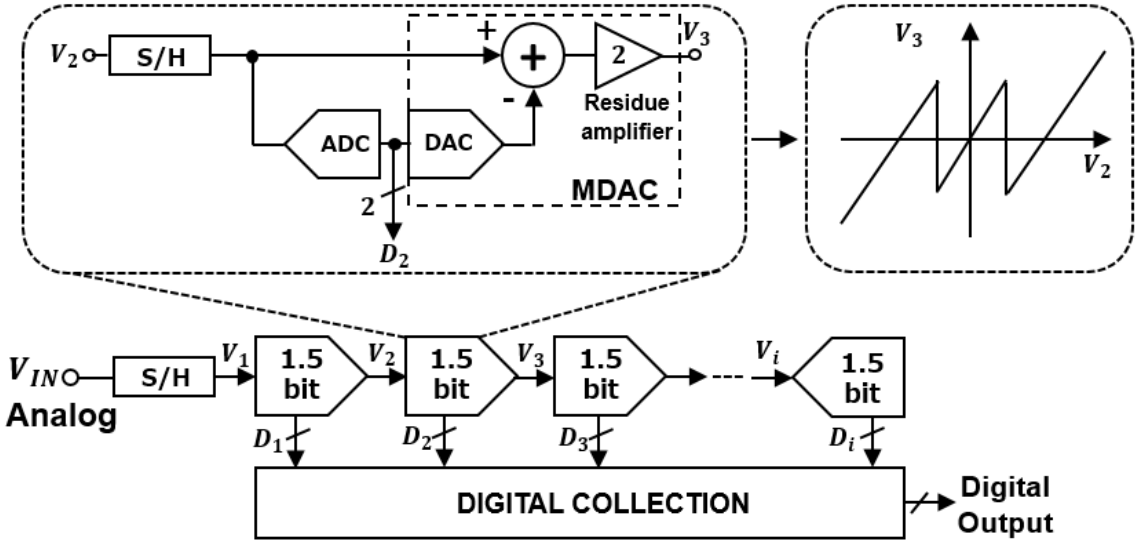


Fig.2.1. Block diagram of 1.5 b/stage pipeline ADC and transfer characteristics.

The output of ADC stage can be expressed by

$$V_{OUT}[V] = 2^n V_{IN} - (d_0 + 2^1 d_1 + \cdots + 2^{n-1} d_{n-1}) V_{REF} \tag{2.1}$$

where $d_i \in \{-1, 1\}$, ($i = 0,1,\ldots, k-1$) when non-redundant code is used or $d_i \in \{-1, 0, 1\}$ when redundant code is used.

2.1.1 Sample-and-hold Stage in Pipeline ADC

In pipeline ADC, at the beginning, the input analog signal is sampled and held by S/H circuit. The S/H stage is one of the key components that determines the performances of

pipeline ADC, carful design of S/H stage is strongly required.

Fig.2.2 shows a common switched capacitor S/H circuit. It is using flip-around sampling and bottom plate techniques and bootstrapped circuit. The circuit timing is shown in Fig.2.3. The flip-around sampling technique relaxes the high requirements in sample-and-hold amplifier (SHA) and the power consumption is lower than traditional charge transferring sampling technique [4]. The benefit of bottom plate technique is: from the switches timing as shown in Fig.2.3, the switch S_2 is turned off faster than S_1. Usually, S_2 is connected to a fixed potential node, so the charge injection of S_2 is fixed but only offset occurred when S_2 is turned off. And because of the turning off timing of S_2, at the transient there is no loop through the sampling capacitance C_S and switch S_1, so the charge injection from S_1 can be minimized. But in practice, the parasitic capacitance at the top plate will store a small amount of charge. This change error can be minimized when using a metal-insulator-metal (MIN) capacitor which has smaller parasitic capacitance at the top plate.

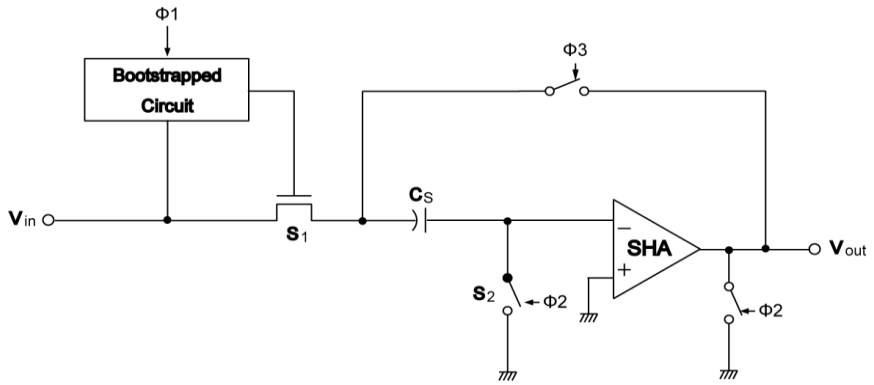


Fig.2.2. S/H circuit.

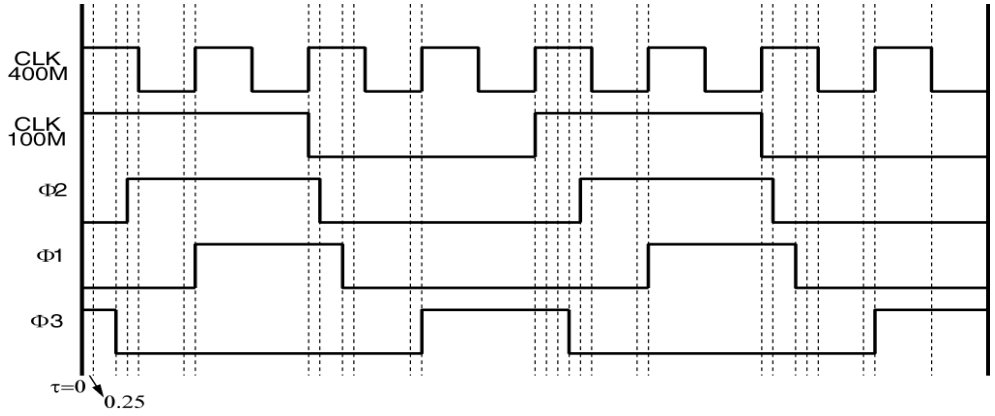


Fig.2.3. Timing chart of S/H circuit.

The reason why the bootstrapped circuit is used in S/H circuit, especially in high

frequency input signal case will be given as following.

In S/H circuit, in sampling period, the switches S_1 and S_2 are closed, and the amplifier is reset, the input signal is charged in C_S; in holding period, the switches S_1 and S_2 are open, the switch S_3 is closed. The amplifier is working, the charge in C_S can be read out from amplifier output terminal.

In this study both S_1 and S_2 are NMOS switch which using a NMOS transistor. Acting as a switch, the NMOS transistor is working in linear region, the path from the source to the drain can be represented by a linear resistor [7] equals to

$$R_{on} = \frac{1}{\beta\,(V_{GS} - V_{TH})} \tag{2.2}$$

Where β is the factor of transistor, V_{GS} is the gate-source overdrive voltage, V_{TH} is the threshold voltage. The on-resistance of the transistor (R_{on}) is depending on V_{GS}. And as shown in Fig.2.2, the source of transistor S_1 is connected to the input signal. As a result, the R_{on} is depending on the input signal V_{in}, a large amount of error will be injected in this situation if the input signal frequency is much higher.

In order to avoid this error, the bootstrapped circuit is added. Fig.2.4 shows a simple bootstrapped circuit, $\overline{\Phi_1}$ terminal is connected to the sampling clock, V_{in} terminal is connected to the signal input, V_{boot} is connected to the sample and hold switch, and V_{ref} is the outside input terminal with the function of adjusting the value of boost. Ideal bootstrapped circuit ensures the difference between V_{boot} and V_{in} is constant to V_{ref} and the timing of V_{boot} is same to Φ_1.

For the bootstrapped circuit, we have

$$V_{boot} = V_{in} + V_{ref} \tag{2.3}$$

In equation (2.3), V_{boot} is always constant to V_{in}, and the difference is V_{ref}. That means V_{GS} value of the transistor is equals to V_{ref}, the R_{on} in equation (2.2) is then become independent

of the input signal V_{in} and be approach kept constant. But because of V_{TH} is depend on the input signal too, the R_{on} can't be kept constant ideally. This error can be minimized if low-V_{TH} transistor is used.

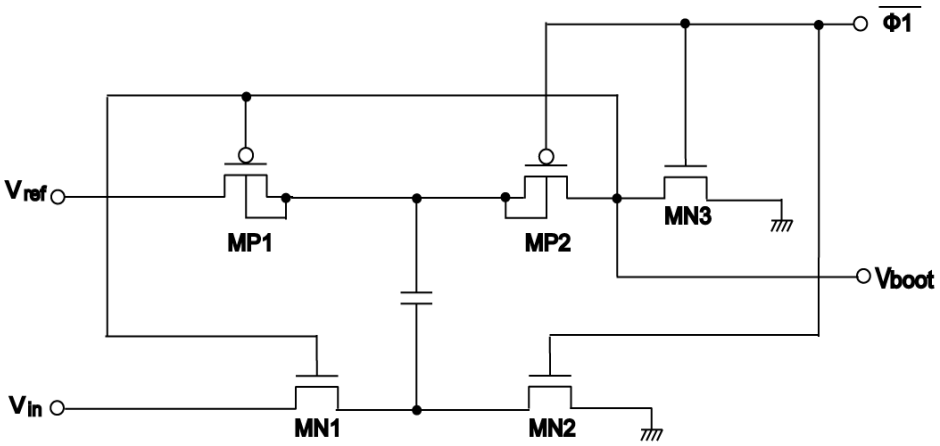


Fig.2.4 Bootstrapped circuit.

From above analysis, in sampling period, we can replace the switches S_1 and S_2 with resistors of their on-resistance R_{on1} and R_{on2}. Two switches together with C_S can be modeled as a RC circuit as shown in Fig.2.5.

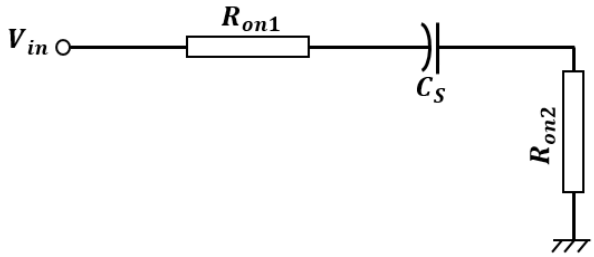


Fig.2.5. S/H circuit model in sampling period.

2.1.2 1.5 b/stage MDAC in Pipeline ADC

In pipeline ADC, another important component in each ADC stage is multiplying DAC (MDAC). The MDAC includes the DAC, the sub-tractor and residue amplifier, as shown in Fig.2.6. A 1.5 b/stage MDAC has two comparators which the reference value of $\pm V_{REF}$ /4. The sub-ADC is a 2-bit ADC with 3 outputs as

$$D(i)=\begin{cases} 1 & \left(\text{if } V_{IN}(i)\geq V_{REF}/4\right) \\ 0 & \left(\text{if } -V_{REF}/4<V_{IN}(i)<V_{REF}/4\right) \\ -1 & \left(\text{if } V_{IN}(i)\leq -V_{REF}/4\right) \end{cases} \tag{2.4}$$

The output of *i*-th stage can be expressed by

$$V(i)=2V(i-1)-D(i)V_{REF} \tag{2.5}$$

The transfer curve of 1.5 b/stage MDAC is shown in Fig.2.7. Comparing to 1 b/stage MDAC, the 1.5 b/stage MDAC relaxes the high precision requirement of the comparator reference value. If there is offset error in the comparator, when the offset error is small than $\pm V_{REF}/4$, the output is still within the output range of $\pm V_{REF}$. The ideal transfer curve and comparator with offset are shown in Fig.2.7 (a) and Fig.2.7 (b), respectively.

The MDAC is controlled by the clocks Φ_1, Φ_{1s} and Φ_2 which are operating alternately in sampling phase and amplification phase as shown in Fig.2.8. In sampling phase, the residue amplifier is reset. In amplification phase, the gain of residue amplifier is determined by the ratio of the two capacitors. If same capacitors are used in the 1.5 b/stage MDAC, the gain of residue amplifier is 2.

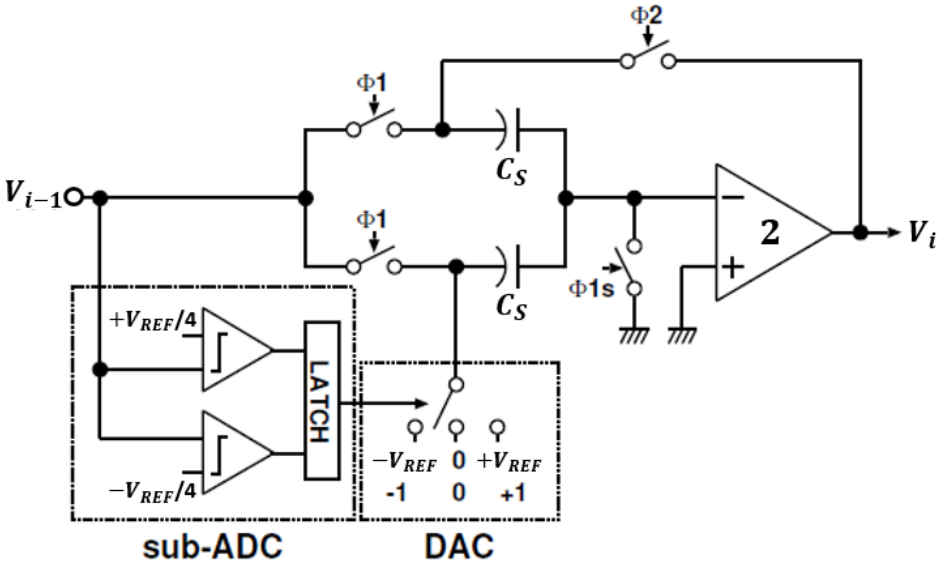
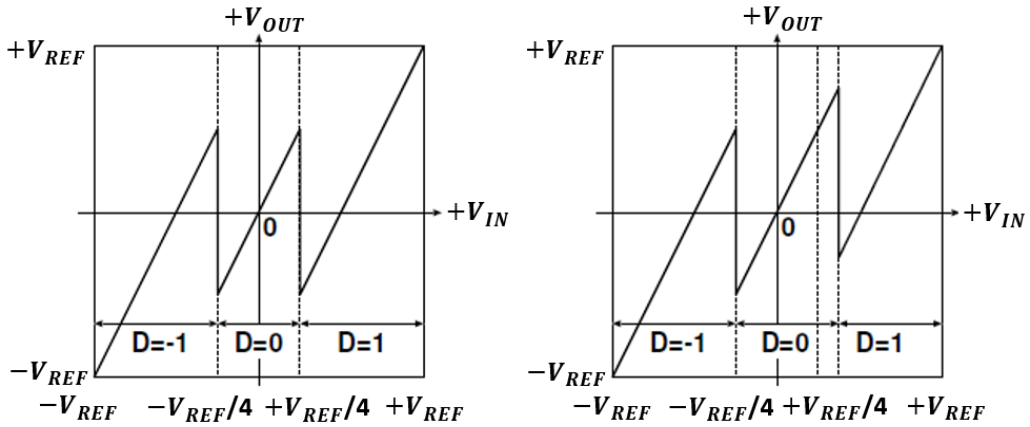
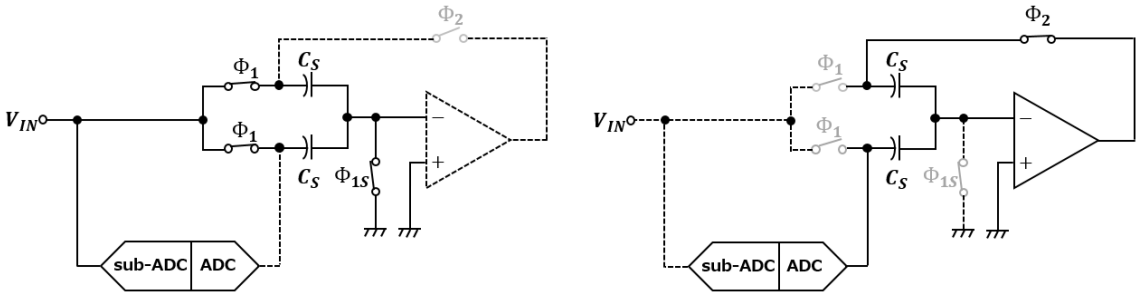


Fig.2.6. Block diagram of 1.5 b/stage MDAC.



(a) Ideal transfer curve. (b) Comparator with offset.

Fig.2.7. Transfer curve of 1.5 b/stage MDAC.



(a) Sampling phase. (b) Amplification phase.

Fig.2.8. 1.5 b/stage MDAC.

2.1.3 Amplifier for SHA and MDAC

There are many types of amplifiers such as folded-cascode, telescopic, two-stage and so on. The amplifiers in S/H stage and MDAC limit the conversion speed and determine the power consumption. It is very important to choose a suitable amplifier with carefully designed for SHA and MDAC. The architecture and determination of the specification are discussed briefly in this section.

Comparing to one-pole amplifiers, differential amplifiers have good power-supply-rejection-ratio (PSRR), good common-mode-rejection-ratio (CMRR), high-precision and so on.

In this study, the folded-cascode amplifier is used, the structure is shown in Fig.2.9. Folded-cascode amplifier has its own advantages compared to the other 2 popular

amplifiers： telescopic amplifiers and two-stage amplifiers. Compared to telescopic amplifiers, folded-cascode amplifiers have larger input and output range, and they are easier to be properly biased but requires larger static biasing current; compared to two-stage amplifiers, the folded-cascode amplifiers are easier to compensate, since two-stage amplifiers are instinct one-pole systems, the compensation is not easy.

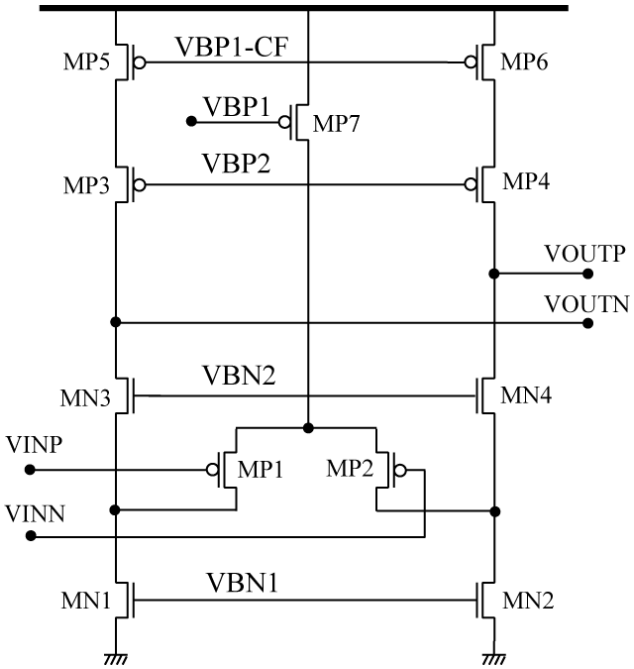


Fig.2.9. Folded-cascode amplifier.

Gain of amplifier

Usually, high-gain amplifier is required. For a 14-bit ADC, the gain of amplifier in S/H stage should be larger than 100 dB. But for the reason of device scaling in CMOS process, high gain amplifier is not easy to achieve when small channel length transistors are used. But the finite gain error can be corrected in digital domain as many paper reported.

Bandwidth

Bandwidth of an amplifier limits the settling speed, larger bandwidth means shorter settling time. But in S/H stage, the bandwidth of amplifier can’t be increased much bigger

than the maximum input signal frequency, because this action potentially reduces the characteristics of S/H stage if the ADC input contains high-frequency noise.

As discussed above, carefully designed amplifier with properly gain and bandwidth is strongly required in SHA and MDAC.

2.2 ADC Performance

2.2.1 Static Performance

For ADCs, the static performance is determined by the input-output transfer characteristics and is mainly defined by quantization error, offset error, gain error, differential non-linearity (DNL) and integral non-linearity (INL). The gain errors and offset errors are shown in each step transition, and both cause non-linearity of ADC. In Fig.2.10, an ideal input-output transfer curve of a 3-bit ADC is given. DNL and INL are two parameters describe the non-linearity of ADCs. The DNL is the difference between every real and ideal step. The INL is the difference between real transfer curve to the ideal transfer curve as show in Fig.2.11.

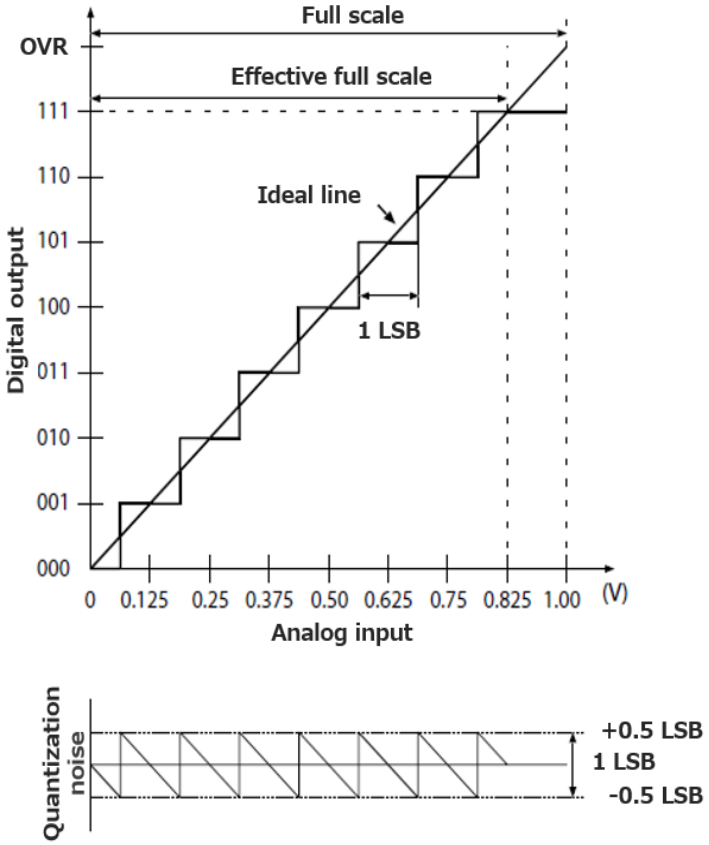


Fig.2.10. Ideal 3-bit ADC transfer curve and quantization error. [6]

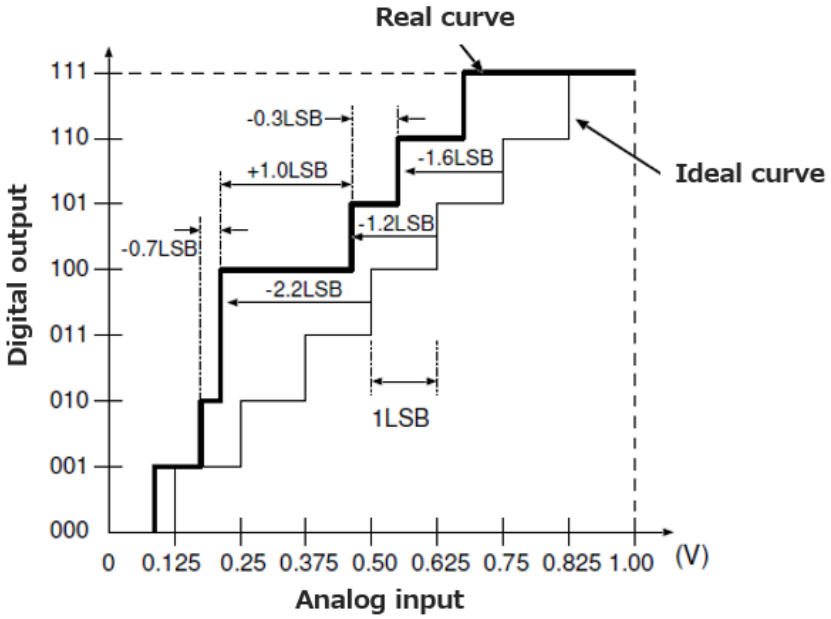


Fig.2.11. Illustration of DNL and INL in a 3-bit ADC. [6]

2.2.2 Dynamic Performance

The dynamic performance of ADCs is evaluated by fast-fourier-transform (FFT). Using a single tone sinusoid signal as the input, the ADC outputs are collected. The dynamic characteristics can be obtained from the analyzation of output data forming a power spectrum by FFT.

According to the Nyquist sampling theorem，carefully choosing a test signal frequency or using window function in FFT, the input signal can be separated from the noises in the power spectrum. In ideal case, there is only the input signal in the spectrum. But in real case, the output induces harmonic distortions and additional noise etc. As shown in Fig.2.12, an example of the power spectrum (normalized to the signal power) is presented, it includes the input signal, high order harmonics and noise. The dynamic characteristic of ADCs is mainly defined by SNR, SNDR, SFDR and THD. The definitions are given as followings.

SNR

SNR stands for signal-to-noise ratio, it is defined by the ratio of signal power and the sum of power at all other frequency excluding the highest 9 harmonics. Thermal noise in

transistors and sampling instance uncertainties etc. will increase noise in S/H circuit.

$$SNR[\mathrm{d}B] = 10\log\frac{P_{signal}}{P_{other\cdot under\cdot Fs/2} - P_{2HD+3HD+\cdots\cdot 9HD}} \tag{2.6}$$

SNDR

SNDR stands for signal-to-noise and distortion ratio, it is defined by the ratio of signal power to the power of noise and all harmonic distortions.

$$SNDR[\mathrm{d}B] = 10\log\frac{P_{signal}}{P_{noise}} \tag{2.7}$$

Usually, an ADC can hardly achieve the maximum SNDR limited only by quantization noise but with the additional noise. The additional noise induced by noise in transistors and non-linearity in all component circuits. Adding the consideration of low power consumption, normally, the practical SNDRs for 10b, 12b and 14b ADCs are set to 59dB, 68dB and 74dB, respectively.

SFDR

SFDR stands for spurious-free dynamic range, it's defined as the ratio of signal power to the power of the maximum harmonic distortion (usually, the 3rd harmonic distortion in a full differential circuit).

$$SFDR[\mathrm{d}B] = 10\log\frac{P_{signal}}{P_{\max imun\cdot harmonic}} \tag{2.8}$$

THD

THD stands for total-harmonics distortion, it is defined as the ratio of power of all harmonics to the power of signal (usually, the power of the maximum 9 harmonic distortions are included).

$$THD[\mathrm{d}B] = 10\log\frac{P_{2HD+3HD+\cdots 9HD}}{P_{signal}} \tag{2.9}$$

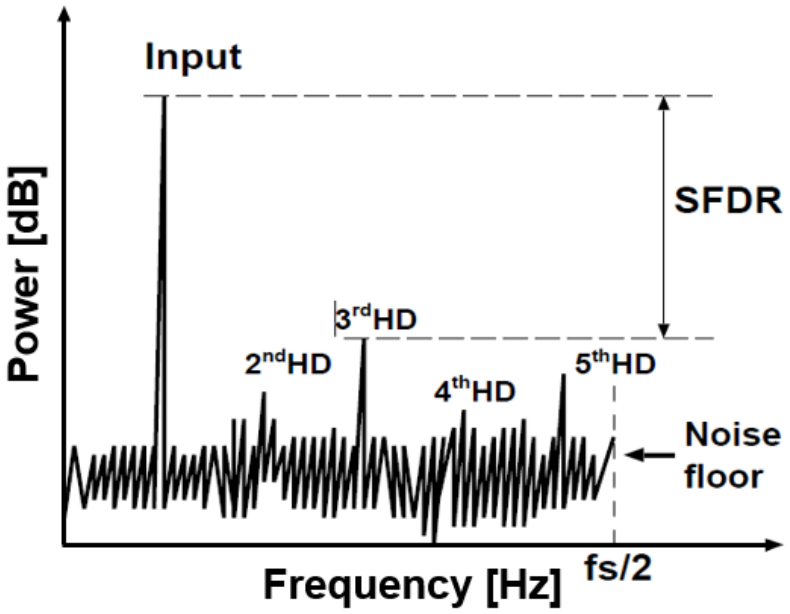


Fig.2.12. Spectrum of ADC outputs.

2.3 Introduction to Time-interleaved ADCs

TiADCs were introduced by Black and Hodges [8]. Fig.2.13 shows a simplified block diagram of the TiADC. An analog input signal V_{in} is sampled and held in M time-interleaved parallel channels, and the digital multiplexer (MUX) is used to combine the digital outputs of sub-ADCs from the channels. Because each sub-ADC is operating at sampling period of T_S, using M-channel ADCs, the sampling frequency is increased by a factor M, giving an overall sampling period of $M \times T_S$. TiADCs are considered to achieve very high speed and high resolution data conversion by using lower-speed ADCs such as a pipeline ADC [9].

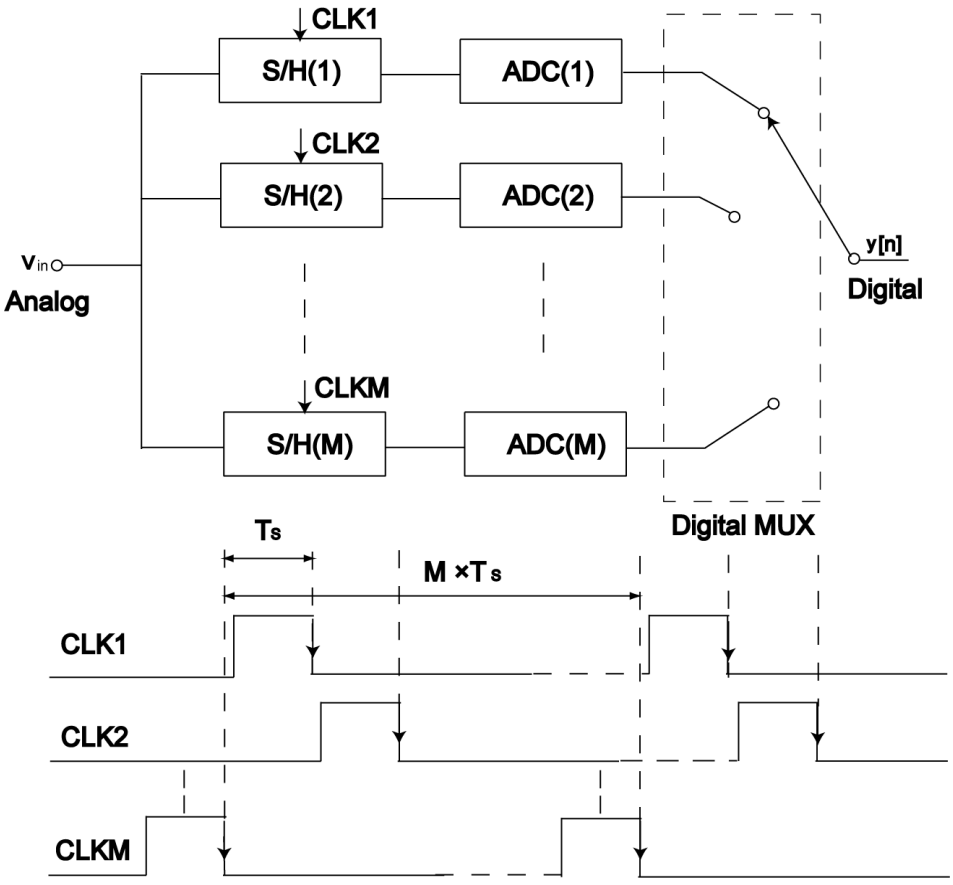
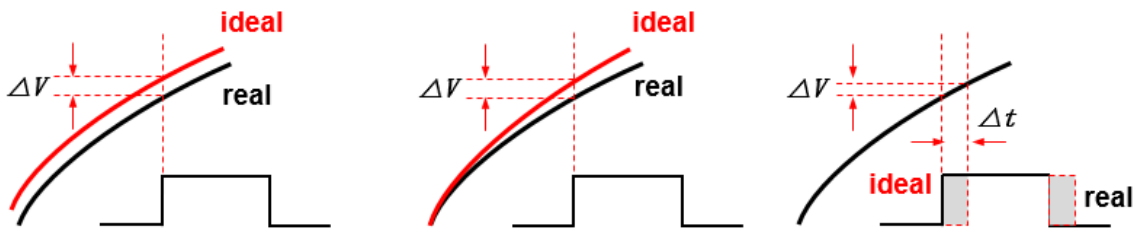


Fig.2.13. A simplified block diagram of TiADC.

2.4 Mismatches in Time-interleaved ADCs

The mismatches between TiADCs channels and their effects are introduced briefly in this section [11,12,13,14]. The TiADC architecture is sensitive to mismatches between the channels due to process, voltage and temperature variations. Mismatches include offset mismatch, gain mismatch and clock skew will cause sampling error as shown in Fig.2.14. The sampling error is defined as the difference between the real and ideal sampling value.

The offset and gain mismatch are the differences between the static characteristics of ADCs. The clock skew because of the different delay among the multi-channel makes the sampling in time-interleaved system a kind of non-uniform sampling with a whole period of MT [11]. Sampling error due to mismatches causes large distortions and decreases the ADC performance. It is possible to quantify the impact of such mismatches on the performance of the TiADC in terms of SNR. This allows the derivation of deterministic and statistical bounds on the acceptable mismatch given a target ADC resolution, as published in [15, 16].



(a) (b) (c)

Fig.2.14. Sampling error caused by mismatches when M=2. (a) Offset mismatch. (b) Gain mismatch. (c) Clock skew.

Although in reality, all mismatches are presented, but for simplify, this study focuses on the clock skew but the other mismatches are set to zero. A global clock skew in M-channel TiADCs is shown in Fig.2.15. If the *CLK2* has a delay of t_{e1} and the *CLK3* has a delay of

t_{e2} , when $t_{e1} \neq t_{e2}$, the different delay cause clock skew in global sampling.

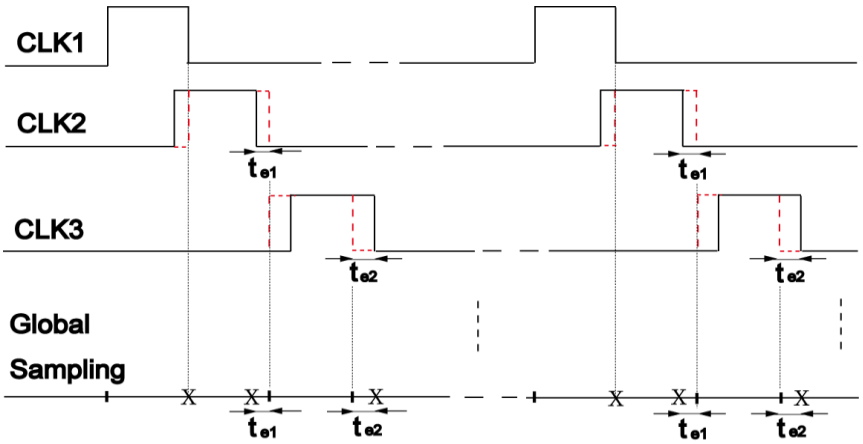


Fig.2.15. Clock skew in TiADCs.

A detailed overview of clock skew is shown in Fig.2.16. (a) and (b). When *M=2* for simplify, sampling clocks *CLK1* and *CLK2* for the two sub-ADCs are ideally spaced as shown in Fig.2.16. (a). The sub-ADC of second channel samples the signal exactly at T_S after the sampling in the first channel sub-ADC. However, if clock skew τ existed, signal is sampled at $T_S+\tau$, as shown in Fig.2.16. (b). Clock skew results in the non-uniform sampling of the input signal, which creates voltage sampling errors, as shown in Fig.2.16. （c）and (d). For a given clock skew, it is obviously that the magnitude of this sampling error changes as a function of the input signal frequency. The sampling error as a result of the clock skew becomes serious when the input signal frequency is much higher.

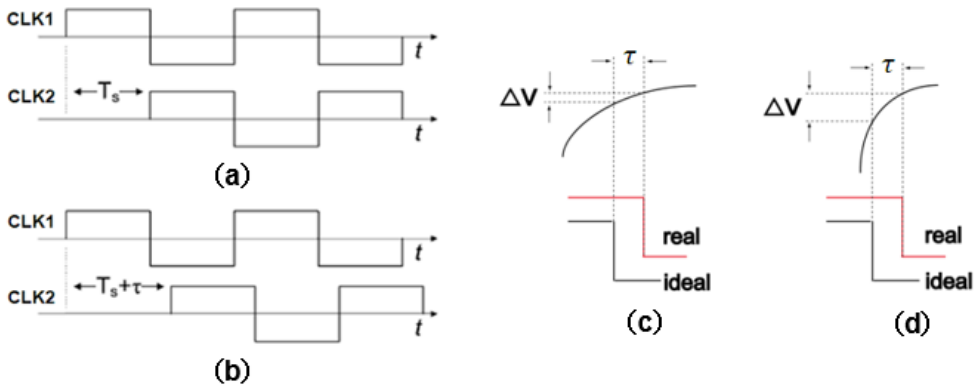


Fig.2.16. (a) Ideal and (b) non-ideal timing relationship between sub-ADC clocks for M=2. Sampling error as a result of clock skew for (c) low frequency and (d) high frequency.

A simple estimation for the maximum tolerate skew is obtained when the input clock skew is assumed to be a sinusoid with frequency f_{in}, and when the clock skew induced error is bounded in magnitude to the quantization error of a B-bit converter. This yields [16]

$$\sigma_\tau^2 \le \left(\frac{M}{M-1}\right)\cdot\left(\frac{2}{3\cdot 2^{2B}}\right)\cdot\left(\frac{1}{(2\pi f_{in})^2}\right) \tag{2.10}$$

where σ_τ is the standard deviation of the clock skew among the channels and M is the interleaving factor. From the inequality, for example in 2-channel 12-bit TiADC, when the sinusoidal input signal frequency is 50 MHz, the toleration clock skew is approximated by 2.94 ps.

2.5 Clock Jitter in ADCs

Beside mismatches introduced in Section 2.4, clock jitter is another factor that causes sampling error, it is probably most obscure specification in ADCs. It basically describes the timing errors in the S/H circuit due to clock distribution. Different to systematic clock skew in TiADCs, jitter has same effects no matter in single or multi-channel. Clock jitter statistics are typically similar to random noise that causes sampling error but the jitter sampling error is not affected by the actual clock frequency, it raises the noise floor and as a result of decreasing the SNR. SNR performance at low input signal frequency is not impacted by clock jitter but at high frequency clock jitter can be the dominant limiting factor on SNR performance [17].The effect of clock jitter is shown in Fig.2.17.

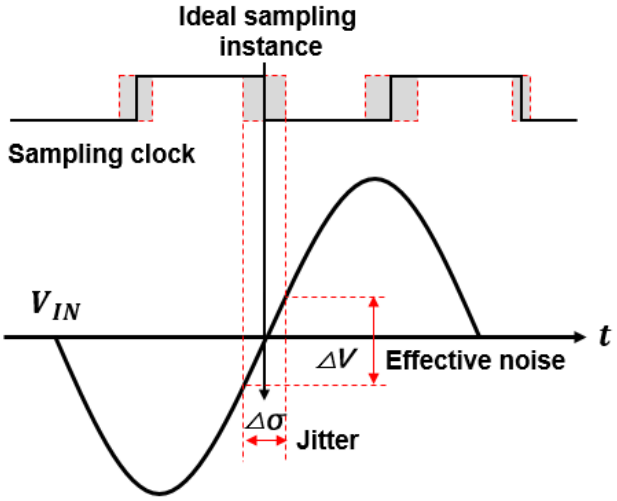


Fig.2.17. Error caused by jitter.

Assuming the standard deviation of clock jitter is $\sigma_{j,rms}$, the resulting SNR_{Jitter} of the sampled sinewave is then[18]

$$SNR_{Jitter} = -20\log\left[(2\pi\sigma_{j.rms} f_{in})\right] \tag{2.11}$$

The SNR_{Jitter} limitation must be added to the intrinsic ADC SNR limitation, SNR_{ADC}. The overall SNR of the ADC SNR_{Total} is then given by

$$SNR_{Total} = -20\log\sqrt{10(\frac{-SNR_{ADC}}{10})+10(\frac{-SNR_{Jitter}}{10})} \tag{2.12}$$

Fig.2.18 shows the equation for an SNR_{ADC} of 65 dB. It shows the SNR_{Total} as a function of sampling clock jitter $\sigma_{j,rms}$ and input sinewave frequency. When the input frequency is higher than 50 MHz, the SNR_{Total} is reduced strongly because of the clock jitter.

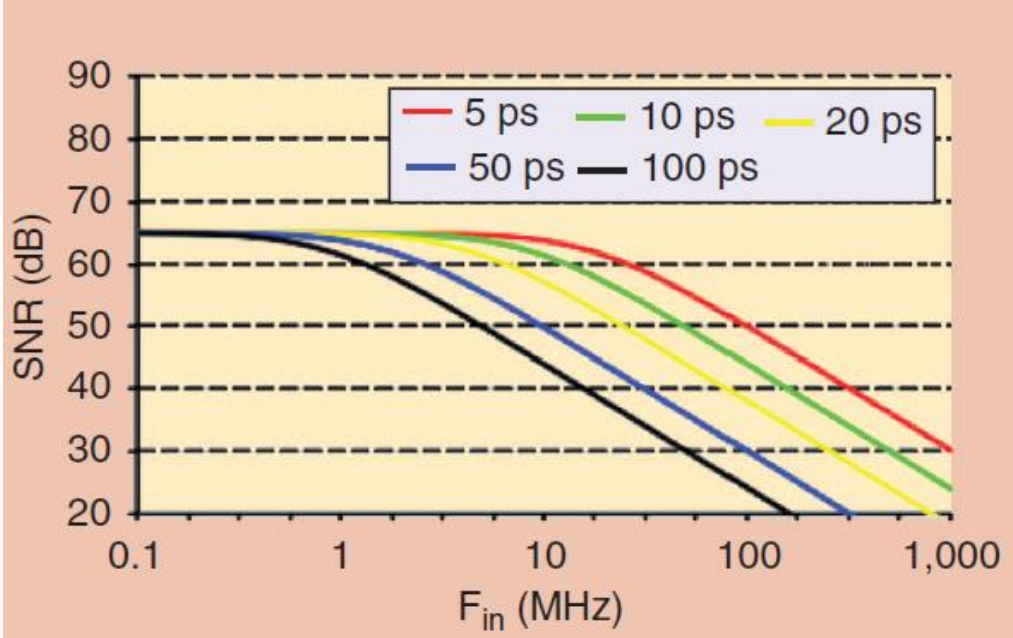


Fig.2.18. Error caused by jitter. [18]

2.6 Introduction to Time-resolved CMOS Image Sensors

TR CMOS image sensors have recently been paid much attention in applications of time-of-flight (TOF) range imaging, biological imaging, and so on. The TOF range imagers are applied in a lot of area due to the range and resolution, such as automotive security, game gesture recognition and 3D scanner. Another application of TR CMOS imager is fluorescence lifetime imaging microscopy (FLIM), the fluorescence life-time of nanosecond order has been measured with the resolution of sub-nanosecond. Fig.2.19 shows the TR CMOS imagers used in TOF [19], FLIM [20], and 3D scanner [21]. Higher time resolution TR image sensors is strongly required for extending the application area of TOF imager especially 3D scanner.

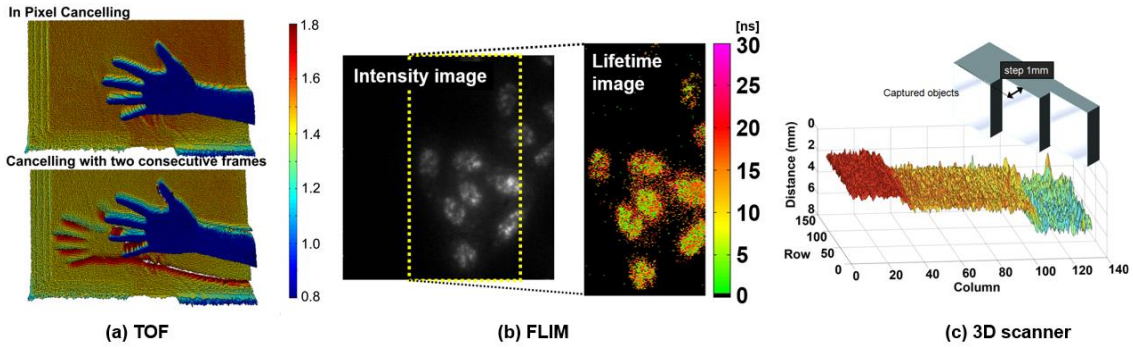


Fig.2.19. Applications of TR image sensors.

A block diagram of TR CMOS image sensor is shown in Fig.2.20, it includes a clock tree which supply the gating clock (TD) to pixels by column-parallel clock drivers. The unit pixel is based on draining-only modulation (DOM) [22] or lateral electric field modulation (LEFM) [23] structure.

In TOF measurement method, the distance between light source and target object can be calculated if the delay time between the emitted light and received light is measured. For a typical TOF range imager with high time resolution such as sub-millimeter range resolution, the principle of the indirect TOF measuring technique is shown in Fig.2.21.

Different to the conventional method which is using a squared or sinusoidal light source, a short-pulse laser with a pulse of about a hundred picoseconds is used. In the time-gated photo-charge detector, a gating clock for modulating the channel potential is formed along the channels to perform lock-in detection [24].

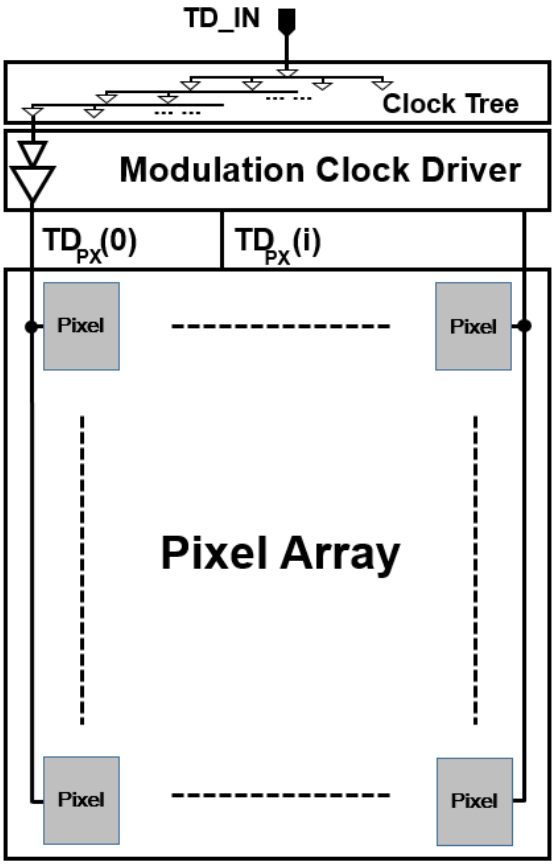


Fig.2.20. TR image sensor diagram.

The laser echo from the target object is received and converted to a photocurrent in the photo diode. The time-of-flight (t_{TOF}) can be calculated by the response time of the detector τ_0 and the photocurrent. When the photocurrent response is assumed to be linear, the t_{TOF} is expressed by [24]

$$t_{TOF} = T_{offset} - \tau_0 \sqrt{2r} \tag{2.13}$$

where T_{offset} is the time difference between a light trigger and TD(2). r is the signal charge ratio defined by [24]

$$r = \frac{N_2 - N_3}{N_1 - N_3} \tag{2.14}$$

where N_1 , N_2 and N_3 are the accumulated electrons which are determined by the gating-clock signals TD(1), TD(2) and TD(3), respectively.

In equation (2.13), the T_{offset} determines the minimum measureable range. The amount of measurable range is determined by τ_0. Because the measurable range is shifted by changing the T_{offset}, if the T_{offset} is outside of measurable range, the depth calculation is failed, therefore the T_{offset} for all the pixels in columns must be same [24].

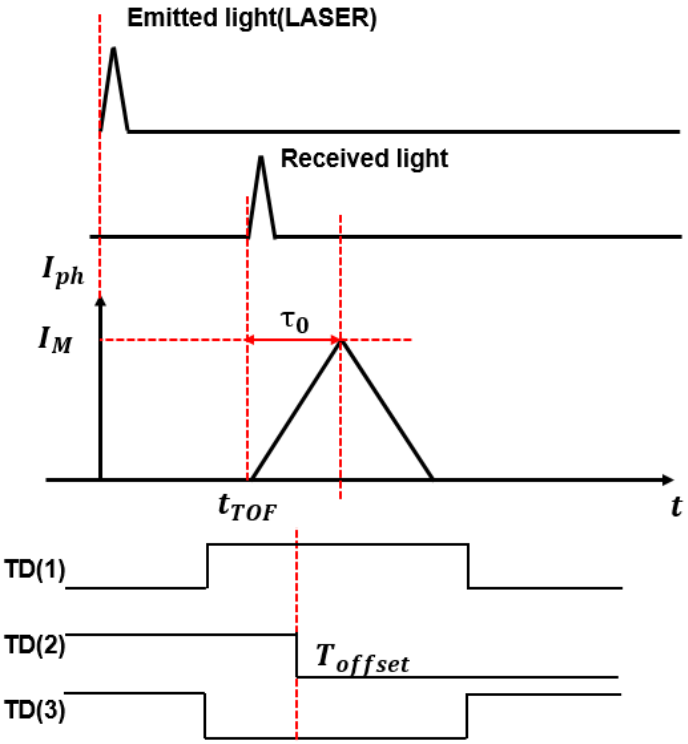


Fig.2.21. Indirect TOF measurement technique base on an impulse photocurrent response.

2.7 Clock Skew in Time-resolved CMOS Image Sensors

Because the clock driver has to drive a large capacitance due to a large number of gates in one pixel column, a large clock skew may occur because of a different delay from pixel to pixel in columns. The skew includes both random and systematic components, which are mainly due to device mismatches (especially clock drivers) and a voltage drop of power supply line, respectively. The systematic skew due to the power-supply voltage drop of a clock driver is dominant according to [24].

Fig.2.22 shows a normalized pixel modulation characteristic of TR CMOS image sensor, if a clock skew is existed, the modulation characteristic will be shifted. In high time resolution TR image sensor, if the skew is comparable or larger than the measurable range, each pixel has a different measureable range. Thereby, simultaneous capturing for all the pixels cannot be achieved. For example, in [24], in reality, the T_{offset} is different from pixel to pixel due to a clock skew of the gating clock, $\triangle T_{offset}$. If the skew is of a particular pixel is larger than the measurable range, simultaneous TOF measurement for all the pixels will be failed. Therefore, $\triangle T_{offset}$ must be much smaller than τ_0, which is only several hundred picoseconds[21]

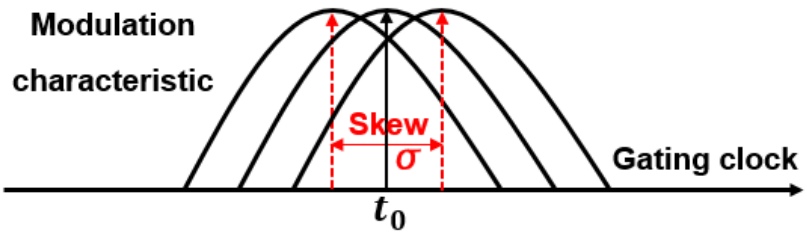


Fig.2.22. Clock skew in TR image sensor.

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Chapter 3

A Clock Skew Calibration for Time-Interleaved A/D Converters

This chapter studies clock skew calibration of sample-and-hold stages (S/H stages) in time-interleaved analog-to-digital converters (TiADCs). TiADCs are considered to achieve high speed and high resolution data conversion by using M-channel low-speed ADCs worked in parallel. However, the TiADCs are sensitive to mismatches between the channels, which cause large undesired spectral distortion and therefore degrade the system performance. In order to address the clock skew problem, a new approach of simple clock skew measurement and calibration circuit used in S/H stages is proposed. The proposed clock skew measurement circuit is using an analog-based delay-locked loop (DLL) and a common phase detector (PD). The clock skew calibration effectiveness is discussed by circuit simulation based on 65-nm CMOS technology. The simulation results show the improvement of spurious-free dynamic range (*SFDR*) value of 2-channel interleaved S/H circuits without and with skew calibration by 19.6 dB at Nyquist frequency.

3.1 Introduction

TiADCs were introduced by Black and Hodges [1]. TiADC is an useful architecture for realizing very high sampling rate. Fig.2.13 in Chapter 2 shows a simplified block diagram of TiADC. An analog input signal V_{in} is sampled and held in M time-interleaved parallel channels, and the digital multiplexer (MUX) is used to combine the digital output of sub-ADCs from the channels. Because each sub-ADC is operating at sampling period of T_S, using M-channel ADCs, the sampling frequency is increased by a factor of M, giving an overall sampling period of $M \times T_S$. TiADCs are considered to achieve very high speed and high resolution data conversion by using low-speed ADCs such as a pipeline ADC [2].

To use the TiADC architecture in a high-resolution ADC， a special design consideration is necessary. The TiADC architecture is sensitive to mismatches due to process, voltage and temperature variations. Each of the sub-ADCs may have a different gain error, offset, and clock skew [3]. Mismatches between the channels cause large distortion and decrease the system performance. It is possible to quantify the impact of such mismatches on the performance of the TiADC in terms of signal-to-noise ratio (SNR). This allows the derivation of deterministic and statistical bounds on the acceptable mismatch given a target ADC resolution, as published in [4, 5].

In the TiADCs, the time-varying errors are caused by clock skew, bandwidth mismatch, jitter, offset and gain mismatch [6]. The sampling error as a result of clock skew becomes serious when the input signal frequency is much higher.

Although in reality all mismatches are presented, for simplify, this study focuses on the clock skew but the bandwidth mismatch, gain mismatch and offset are set to zero.

In order to calibrate the clock skew, a new approach of simple clock skew measurement and calibration circuit used in S/H stages is proposed. The proposed clock skew measurement circuit is an analog-based DLL circuit. The circuit is using a common SR latch based bang-bang phase detector (BPD) with common reference clock and analog current-controlled delay lines (CCDLs). The skew calibration effectiveness is discussed

by circuit simulation based on 65-nm CMOS technology.

The remaining sections are organized as follows. In Section 3.2, the technique of clock skew calibration is proposed and each part of the circuit is introduced in detail. Considerations in the design of analog feedback control loop are given in Section 3.3. The circuit simulation results are presented in Section 3.5 and a brief conclusion is given at last.

3.2 Proposed Clock Skew Calibration for TiADCs

A lot of papers reported the clock skew calibration for TiADCs as summarized in Chapter 1. A TiADC can be made insensitive to the effect of timing skew by adding a single front-end sample-and-hold amplifier (SHA) in front of the sub-ADC array [9, 10], where the SHA works at the aggregate clock frequency. Second, another method of using a low-skew clock generator [11, 12] for S/H circuits. Third, in [13, 14], a global passive sampling technique is proposed. Fourth, some calibration techniques to detect skew by using a ramp calibration signal has been reported in [15, 16]. The other clock skew compensating techniques based on digital phase detector for skew measurement have been reported [17, 18, 19]. The advantages and limitations of the above clock skew calibration are also discussed in Chapter 1.

In this study, a new simple and effective clock skew measurement and calibration approach is proposed. The skew calibration circuit operates in the S/H stages of M-channel TiADCs is shown in Fig.3.1, a common clock reference (*CKR*) is used for skew measurement for sampling clocks (*CLK1~CLKM*). After skew calibration, the delay corrected clocks (*CLK1*~CLKM**) are used for the S/H stages in each channel.

Fig.3.2. (a) shows the details of the calibration circuit of *CLK1* for channel 1, the calibration circuit includes a common BPD for skew detector, a CCDL, a low pass filter (LPF), a voltage-controlled current source (VCCS), a 7-bit ADC, 7-bit register (REG.) and 7-bit DAC, the skew calibration circuit includes two phases: measurement phase and calibration phase, the phase diagram and timing chart is show in Fig.3.2 (b). In measurement phase, the switches S_1, S_2 and S_3 are closed by Φ_{MEAS}, the skew between *CKR* and *CLK1* is detected by the BPD and measured by the analog-cased closed-loop feedback circuit. The measured skew is formed as output voltage of LPF and stored in the register through an ADC. In the calibration phase, the switches S_1, S_2 and S_3 are turned off, the switches S_4 and S_5 are closed by Φ_{CALI}, the stored value in the register value is converted to a voltage by the DAC. After VCCS, the voltage is converted to the current.

The delay of *CLK1* is corrected by the CCDL due to the current, the delay corrected clock *CLK1** is then used for the S/H stage in channel 1 in ADC phase.

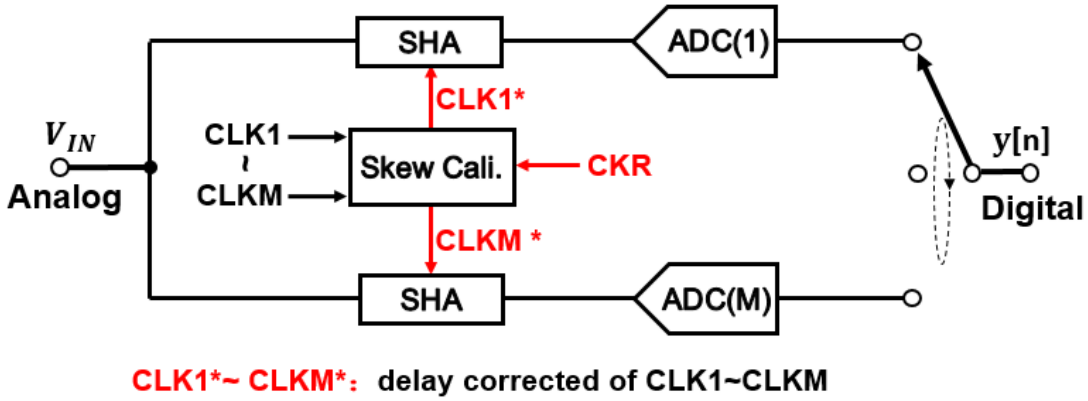
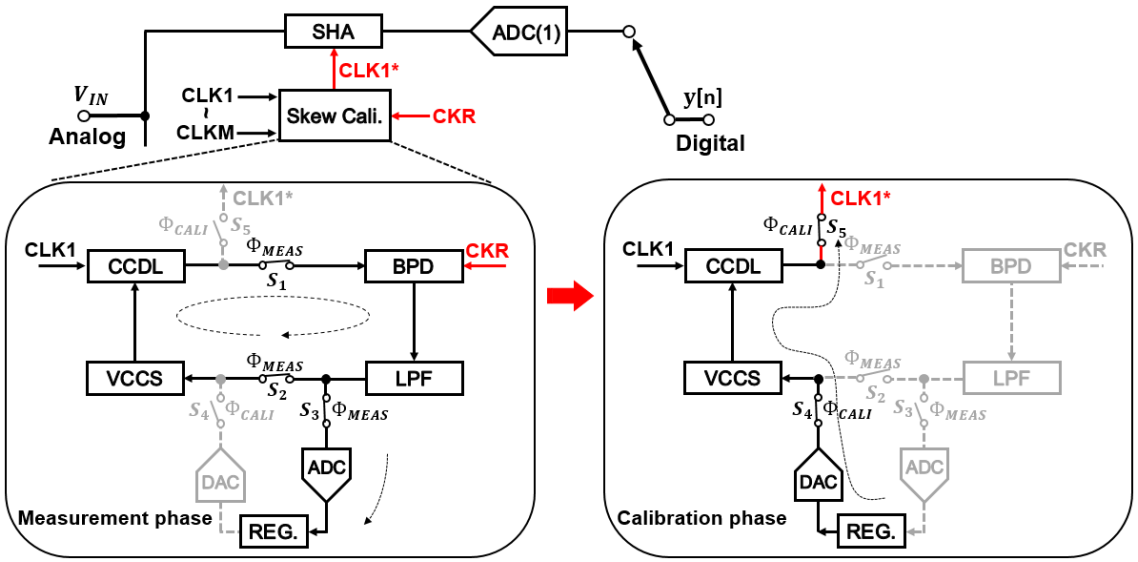
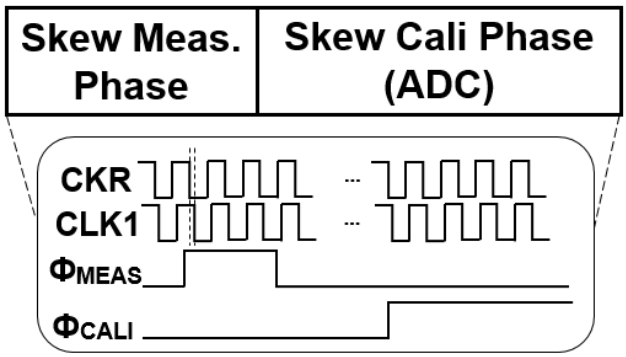


Fig.3.1. Proposed clock skew calibration circuit used in S/H stages.



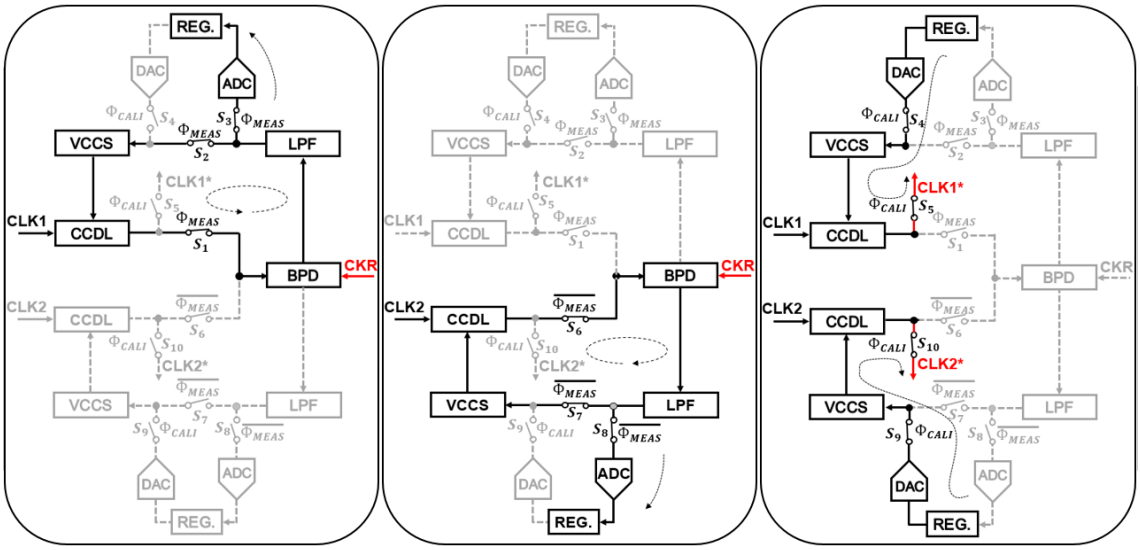
(a)



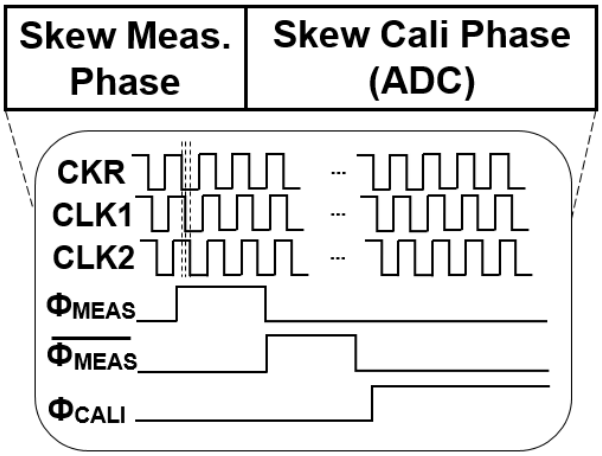
(b)

Fig.3.2. Proposed clock skew calibration circuit and phase diagram.

For simply, in a 2-channel TiADC, the diagram block of the skew calibration circuit and phase diagram are shown in Fig.3.3. The BPD for skew detector is common for *CLK1* and *CLK2*. The skew measurement of both sampling clock can be working inversely in the skew measurement phase, while in the calibration phase both calibration circuits are working in the same time and the ADC is carried out. Since the BPD and CKR are common to CLK1 and CLK2, there is no offset. The details of each parts are described as followings.



(a) (b) (c)



(d)

Fig.3.3. (a) Skew measurement for CLK1. (b) Skew measurement for CLK2. (c) Skew calibration for CLK1 and CLK2. (d) Skew calibration circuit phase diagram. (M=2)

3.2.1 SR latch based Bang-bang Phase Detector

The BPD is widely used in digital phase-locked loops (PLLs) and DLLs [20]. Difference to the conventional PD or phase frequency detector (PFD) which the output is linear to the phase difference of the inputs, the BPD detects the polarity of the phase difference only and lacks the magnitude of phase difference with the feature of no systematic timing offset. Fig.3.4 shows a conventional BPD, in this design 4 D flip-flops (DFFs) are used, the total transistors number is more than 38.

In the study, the SR latch based BPD is used as the skew detector for skew measurement in TiADCs. The SR latch based BPD is shown in Fig.3.5, the two inputs of BPD are assigned to sampling clock (*CLK*) and clock reference (*CKR*). It requires only 8 transistors which is obviously less than conventional BPD.

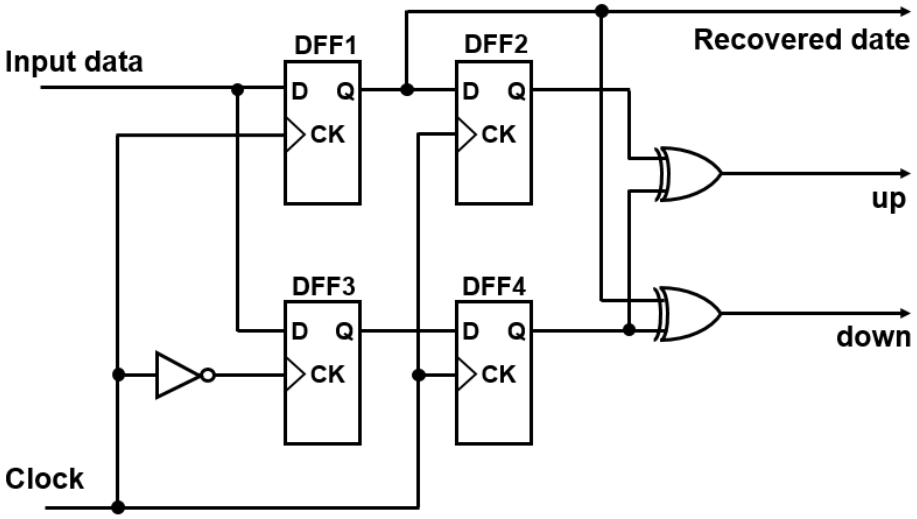


Fig. 3.4. Conventional BPD.

The BPD is designed with a SR latch which is constructed by feeding the outputs of two NOR gates back to the other NOR gates inputs. The operation of the SR latch is shown in Tab. 3.1. If a sampling clock (*CLK*) is assigned to the input of "Reset" and a clock reference *CKR* is assigned to the input of "Set", at the transient of falling edge, there are 4 cases may exist:

1. If the *CLK* is faster than *CKR* (S: 0, R: 1), the output QP is 0;

2. If the *CLK* is slower than *CKR* (S: 1, R: 0), the output QP is 1;
3. If the *CLK* is close to the *CKR* and assumed there is a small random noise (for example: jitter), the output QP will be a 0/1 pulse and the number of 1 (N_1) in *N* cycles depends on how much faster the sampling clock than *CKR* is but not the same situation as case 1. In ideal case, if the sampling clock is same to *CKR*, the output rate of 1 is 50%.
4. Because the SR latch is working when if the *CLK* and *CKR* aren't changed at same transient, the SR latch is working in hold state, there is no change to the previous output.

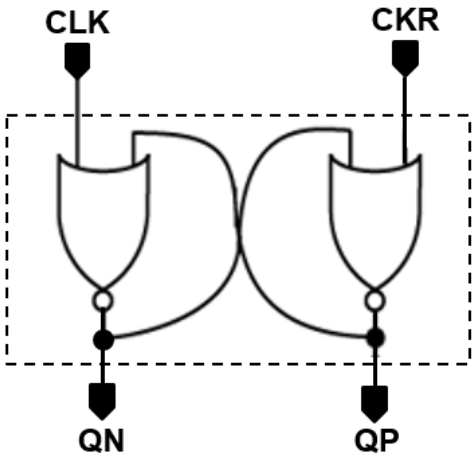


Fig.3.5. SR latch based BPD.

From the above analysis, the SR latch is operating in a racing function, the *CLK* is always racing to the clock reference *CKR*, and therefore in some case we name this circuit as racing circuit. The phase characteristics of BPD is shown in Fig.3.6.

In 2-channel time-interleaved case, the period of *CKR* could be half of *CLK1* or *CLK2*. In normal case, the *CKR* period is $T_S \div M$, as well as the falling edge of sampling clock in the sub-ADCs coincide with the *CKR*. Fig.3.7 shows the timing of sampling clock and *CKR* when M=8.

TABLE 3.1

SR LATCH OPERATION

S	R	$QP^{(i)}$	$QN^{(i)}$	Comment
0	0	$QP^{(i-1)}$	$QN^{(i-1)}$	Hold State
0	1	1	0	Set
1	0	0	1	Reset
1	1	0	0	/

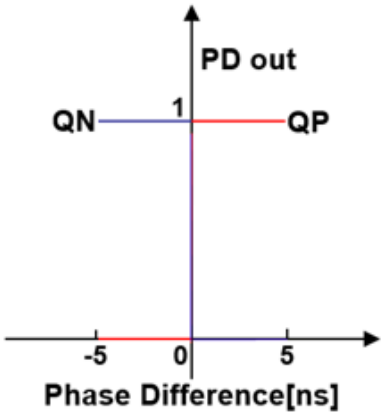


Fig. 3.6. Phase characteristics of BPD.

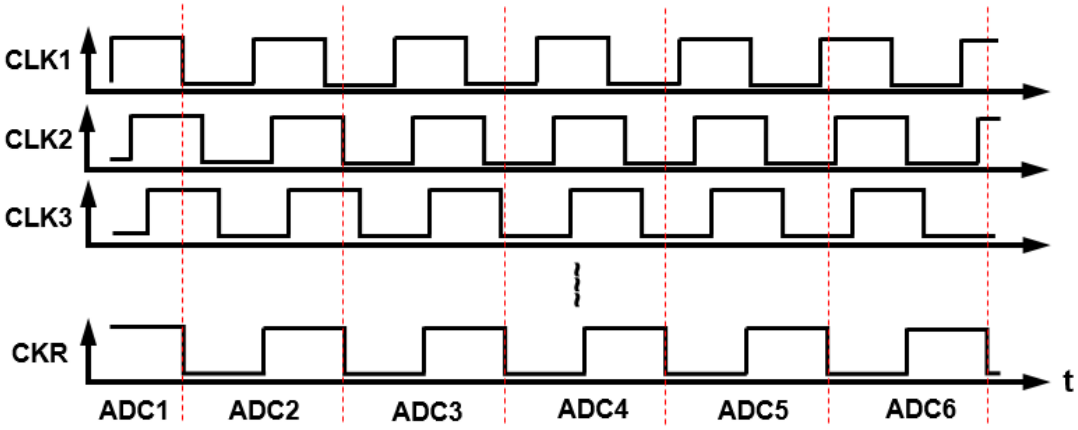


Fig.3.7. Timing of sampling clock and clock reference.(M=8)

3.2.2 Low Pass Filter

A simple RC circuit type low pass filter is used in this design. It transfers the 0/1 pulse

output of the racing circuit to DC voltage. The DC voltage is defined by,

$$V_{LPF} \propto \frac{N_1}{N} = K_1 \times \Delta t \tag{3.4}$$

where N_1 is the number of "1" in N cycles from BPD output (QP), K_1 is the gain of BPD, $\triangle t_d = t_{dR} - t_{dK}$ is the delay difference of $CLK(t_{dK})$ and $CKR(t_{dR})$.

In measurement phase, the clock skew is formed as the voltage output of LPF and the voltage value is stored in a 7-bit register through an ADC. In calibration mode, the time delay of CLK is adjusted by the stored value from the register through a DAC.

3.2.3 Voltage-Controlled Current Source

The VCCS is used for converting the input voltage to current output. As shown in Fig.3.8, the VCCS concludes a basic amplifier and current mirror. In the differential pair, for a fixed input of V_{ref} (in this design, V_{DD} =1.2 V, V_{ref} =1/2V_{DD}=0.6 V), the differential pair current output value $\triangle I_R$ is decided by the difference of V_{ref} and V_{LPF} , if $V_{ref} = V_{LPF}$, the $\triangle I_R$=0. It can be conveyed by this equation:

$$\Delta I_R = I_{R2} - I_{R1} = G_m \times (V_{LPF} - V_{ref}) \tag{3.5}$$

where G_m is the trans-conductance factor of VCCS. The output of VCCS is given by the bias current I_{ref} and the differential current $\triangle I_R$.

$$I_{OUT} = I_{ref} + \Delta I \tag{3.6}$$

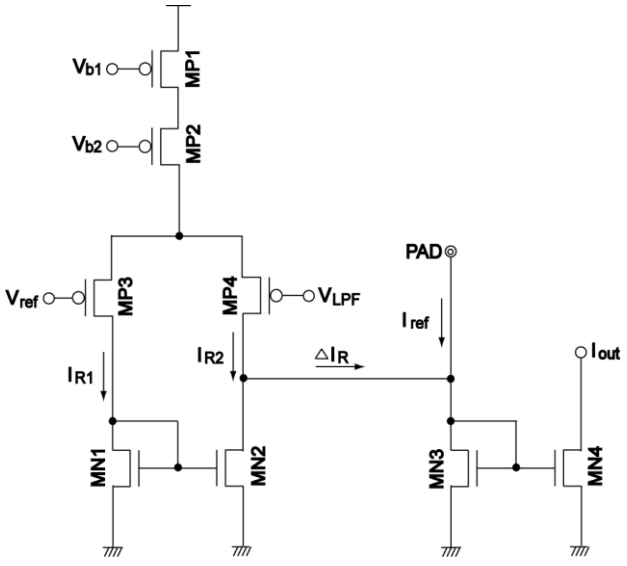


Fig.3.8. Voltage-controlled current source.

3.2.4 Current Controlled Delay Line

The current-controlled delay line (CCDL) consists of a NAND gate and a buffer as shown in Fig.3.9. The NAND gate is for generating the sampling clock in practice in the design.

The simulated delay characteristics of CCDL is shown in Fig.3.10. The x-axis stands for the tail current, and the y-axis stands for the delay. The CCDL has the simulated correction range of 140 ps.

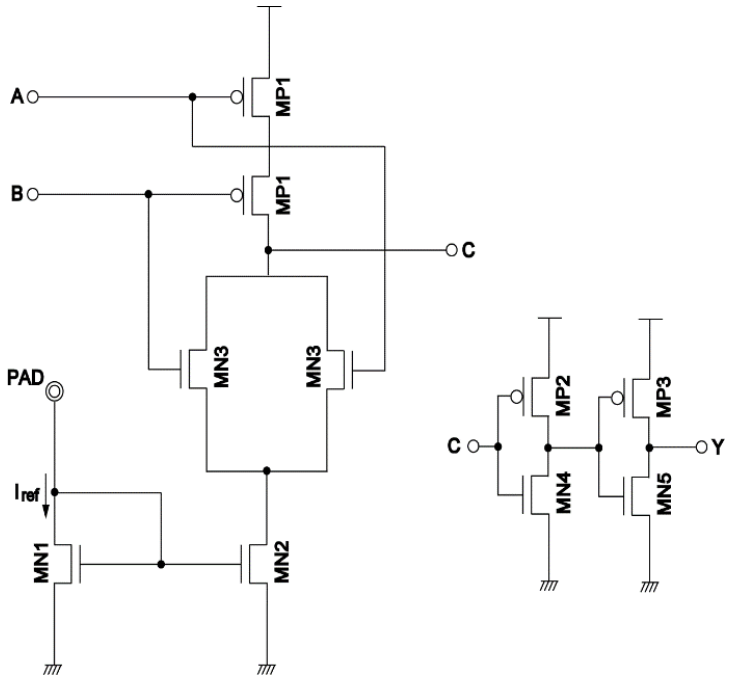


Fig.3.9. Current-controlled delay line.

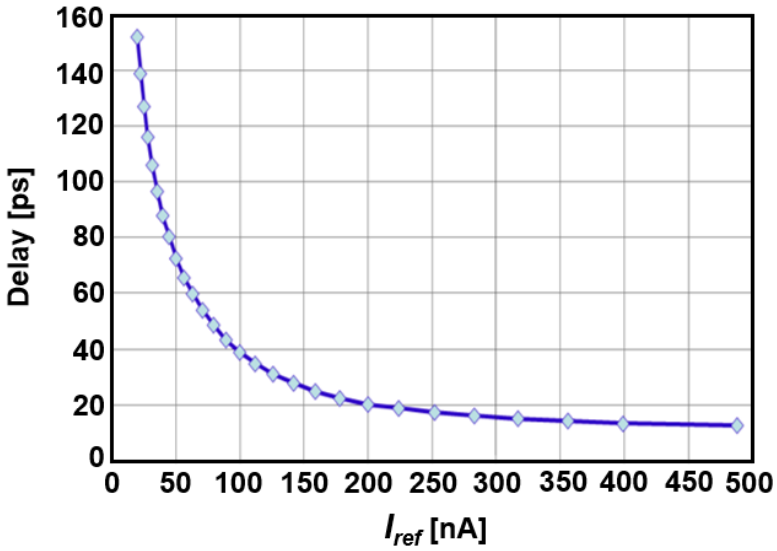


Fig.3.10. Delay characteristics of CCDL.

The output of CCDL is decided by the tail current I_{OUT} and it is given by

$$t_{dK} = t_{d0} + K_2 \times I_{OUT} \tag{3.7}$$

where t_{d0} is the initial delay, K_2 is the factor of CCDL.

3.3 Considerations in Design of Feedback Control Loop

The clock skew $\triangle t_d$ can be derived from equations (3.5-3.7). It can be expressed by:

$$\Delta t_d \approx \frac{t_{dR} - t_{d0} - K_2 \times I_{OUT}}{K_1 \times K_2 \times G_m} \tag{3.8}$$

From the equation (3.8), when the clock skew is minimized ($\triangle t_d \approx 0$), the denominator $K_1 \times K_2 \times G_m$ should be as big as possible. This means the loop-gain should be big enough in the circuit design.

On the other hand, at clock skew measurement phase, the loop circuit is working as a negative feedback circuit, and the feedback systems suffer from potential instability, they may oscillate. To avoid oscillation, careful analysis and frequency compensation are needed. For a stable feedback circuit the phase margin of loop circuit should be bigger than 45 degree and loop-gain should be larger than 1 dB or the closed-loop gain $K_1 \times K_2 \times G_m >> 1000$.

In this study, the feedback circuit has many poles, after simulation, we notice that the main pole is from the low pass filter, the second pole is from the amplifier architecture voltage controlled current source, for the stability the first pole and second pole must be separated for enough distance.

The characteristics of the feedback loop versus the resistor value in LPF is shown in Fig.3.11. The phase margin is 66.7 degree and the loop-gain is 41.2 dB when the resistor value of LPF is 50 $M\Omega$.

The response time in this feedback loop circuit is a trade-off to stability. As shown in Fig.3.12, the response time CLK is increased when the resistor value is increased as a fixed 10 ps skew is given to the CKR. The figure also proves the function of closed-loop feedback circuit for skew measurement.

From the characteristics and response time of the feedback loop circuit, the resistor value of 50 $M\Omega$ is suitable for this design.

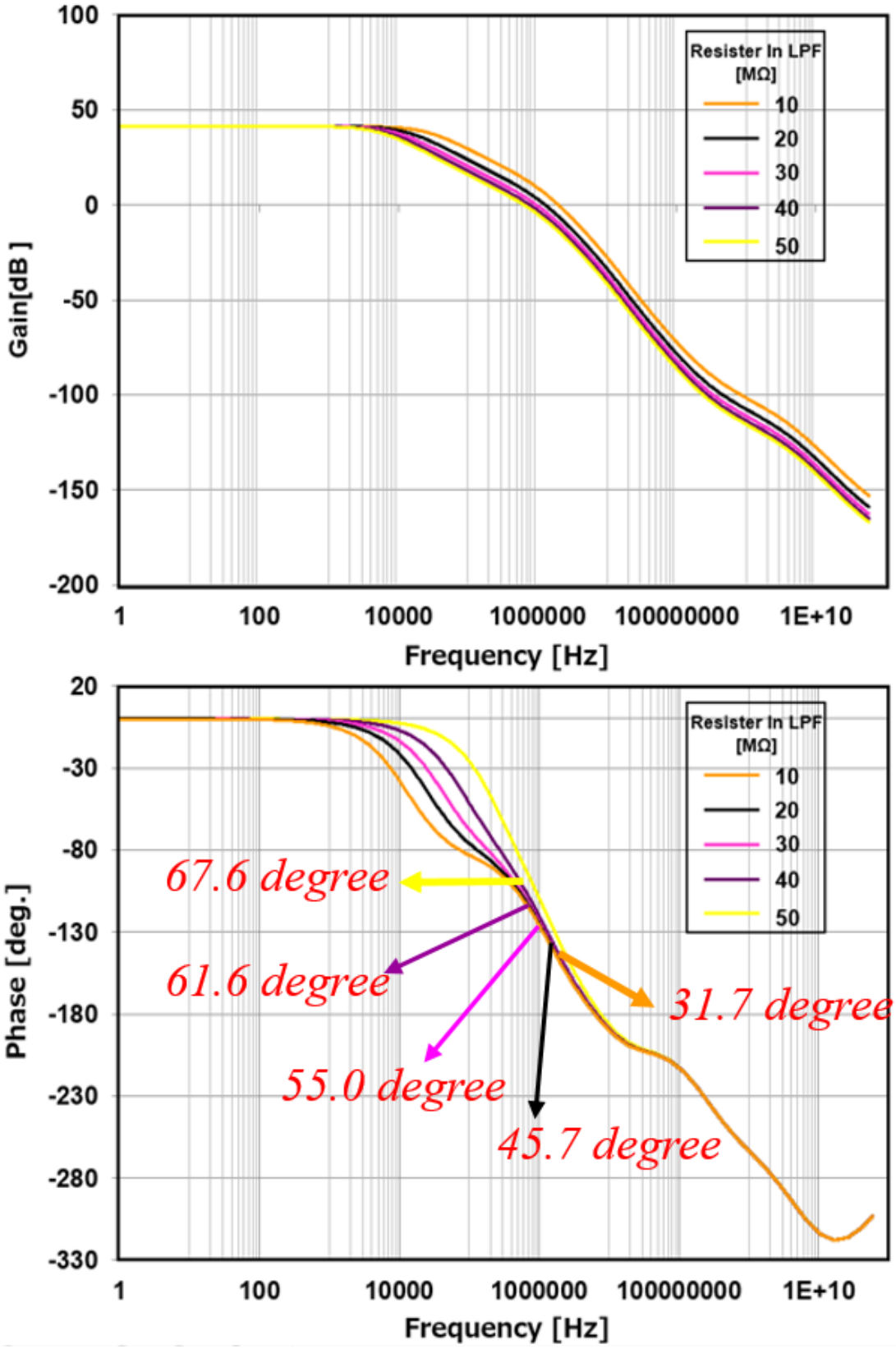


Fig.3.11. Characteristics of the feedback loop.

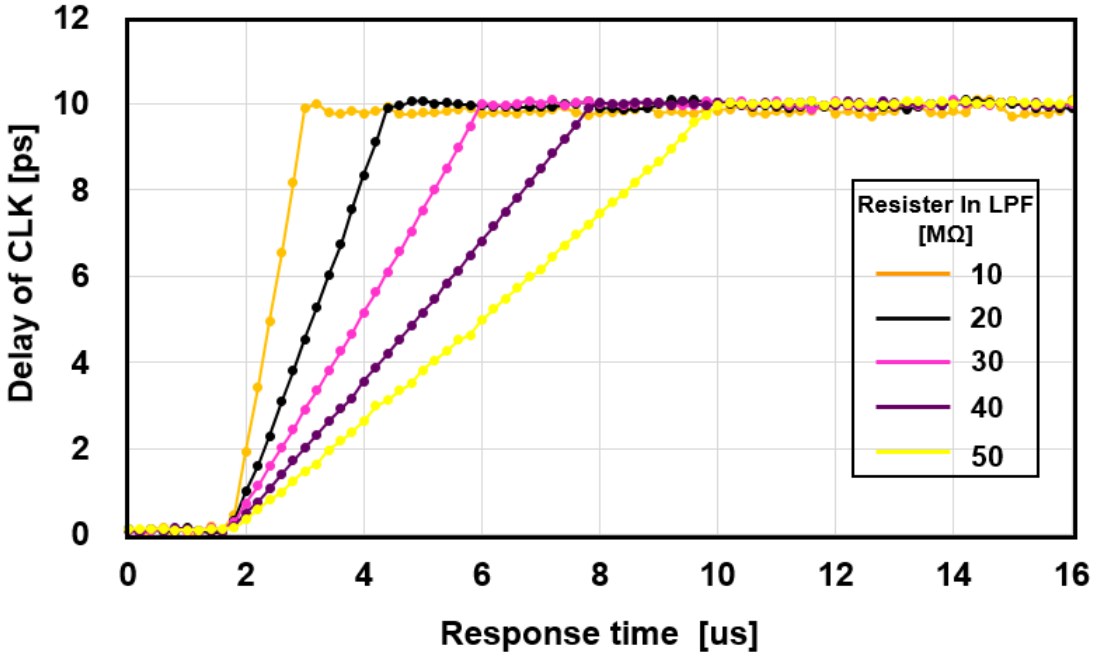


Fig.3.12. Response time of feedback loop.

3.4 Simulation Results

One property of the negative feedback circuit is that the difference of *CKR* and *CLK* tend to be zero, the time delay of *CLK* have to be changed following the time delay of *CKR*, until the *CLK* coincide with the *CKR* at the falling edge. This means if the time delay of *CKR* is setting for the variation, the time delay of *CLK*s must be a function and the function equals variation.

A simulation result of clock skew measurement circuit is shown as Fig.3.13. The x-axis is the time delay of *CKR*, the y-axis is time delay of *CLK*. The red line shows the ideal case and the blue line is the simulation result. The simulation result shows that the *CLK* delay is changed following the *CKR* delay with a small error.

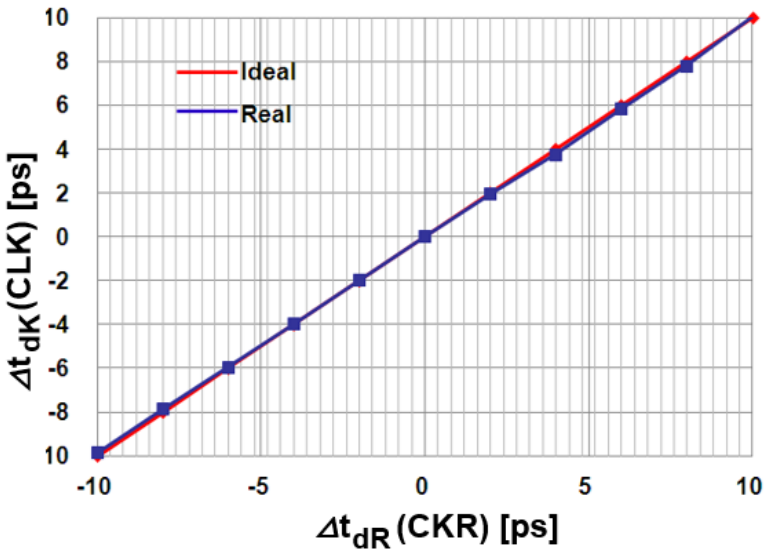


Fig.3.13. Clock skew measurement.

To investigate the effectiveness of proposed clock skew calibration, a 2-channel time-interleaved S/H circuits with skew calibration circuit for a 12-bit pipeline ADC based TiADC is designed. For the purpose of power efficient, the amplifier sharing technique is used in this design, a folded-cascode amplifier is shared in the respective stages of the two channels as shown in Fig.3.14. And the amplifier schematic and bode diagram of the

amplifier is shown in Fig.3.15 and Fig.3.16, respectively. A single tone sinusoid signal is using as input, after S/H stage, the stored output is collected. The data of output is analyzed by FFT to obtain a power spectrum, from the power spectrum the dynamic characteristics can be obtained. Using the total sampling frequency of 200 MHz, each channel is operating at 100 MHz, the *CKR* frequency is 200 MHz and the sinusoid input signals of 20 MHz and 50 MHz are used. When the 6ps skew at 20 MHz is injected to the CLKs (*Φ1A* and *Φ1B*) in S/H stages, before calibration the spur-free dynamic range (*SFDR*) is 68.4 dB, after calibration the *SFDR* is 79.6 dB, the improvement of *SFDR* is 11.2 dB. The power spectrum before calibration and after calibration at the frequency of 20 MHz and 50 MHz are shown in Fig.3.17. (a) - (b) and Fig.3.18. (a) - (b), respectively. The simulation result of *SFDR* improvement before calibration and after calibration based on input frequency scale is shown in Fig.3.19, the figure also show the sampling error (formed as *SFDR*) as a result of clock skew becomes serious when input signal frequency is much higher. At Nyquist frequency (100 MHz) the *SFDR* improvement value is 19.6 dB as shown in Table 3.2.

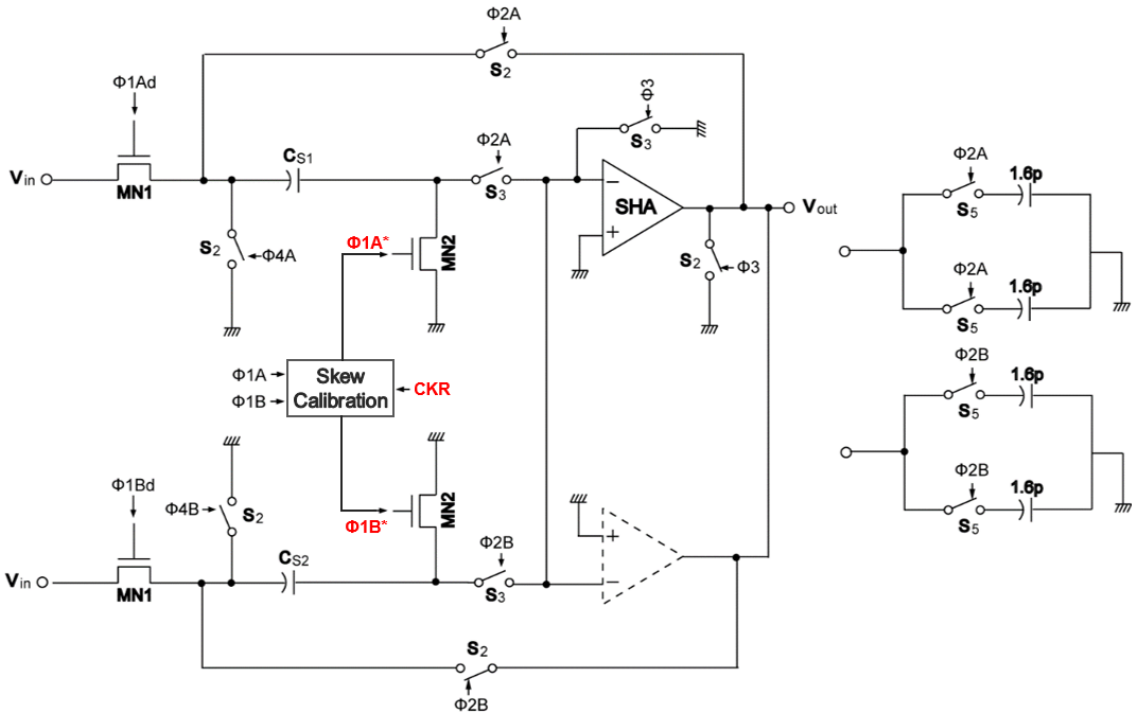


Fig.3.14. 2-chanell time-interleaved S/H circuits with skew calibration circuit and shared amplifier.

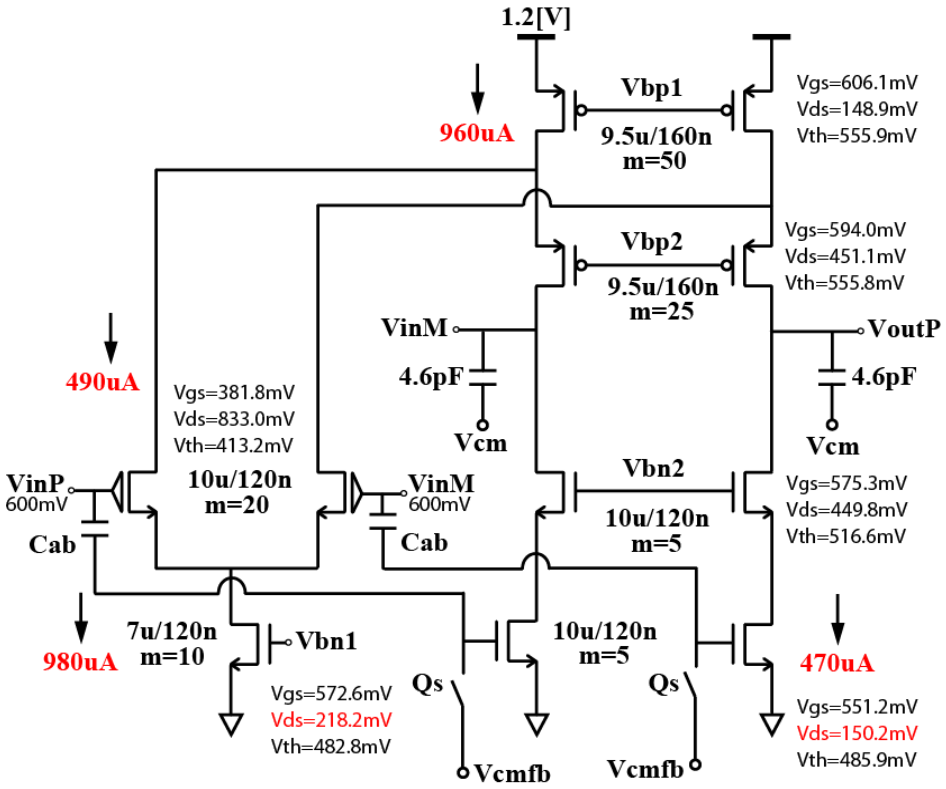


Fig.3.15. Schematic of folded-cascode amplifier.

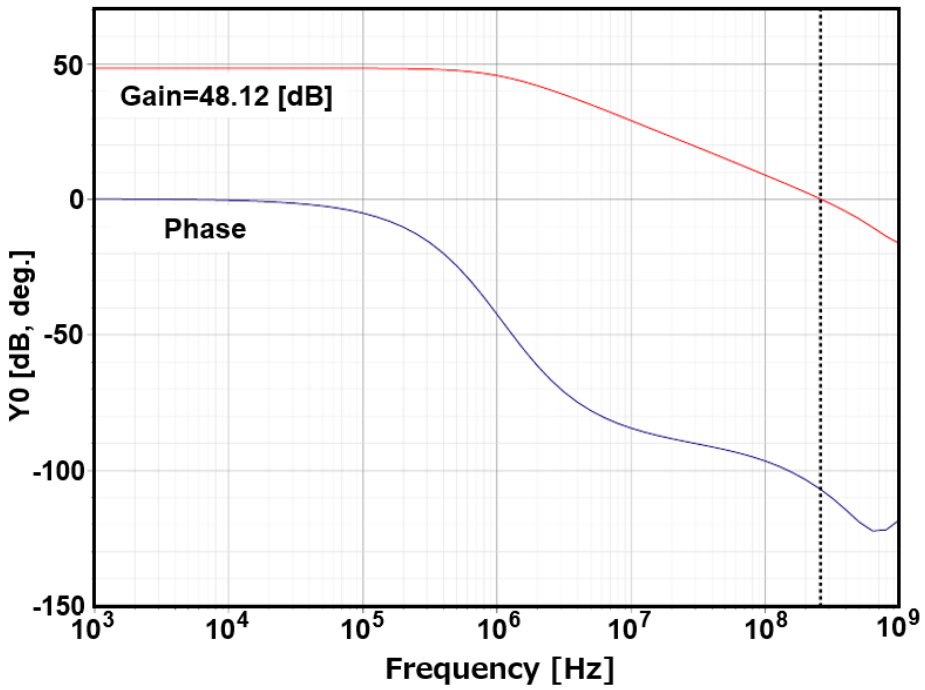
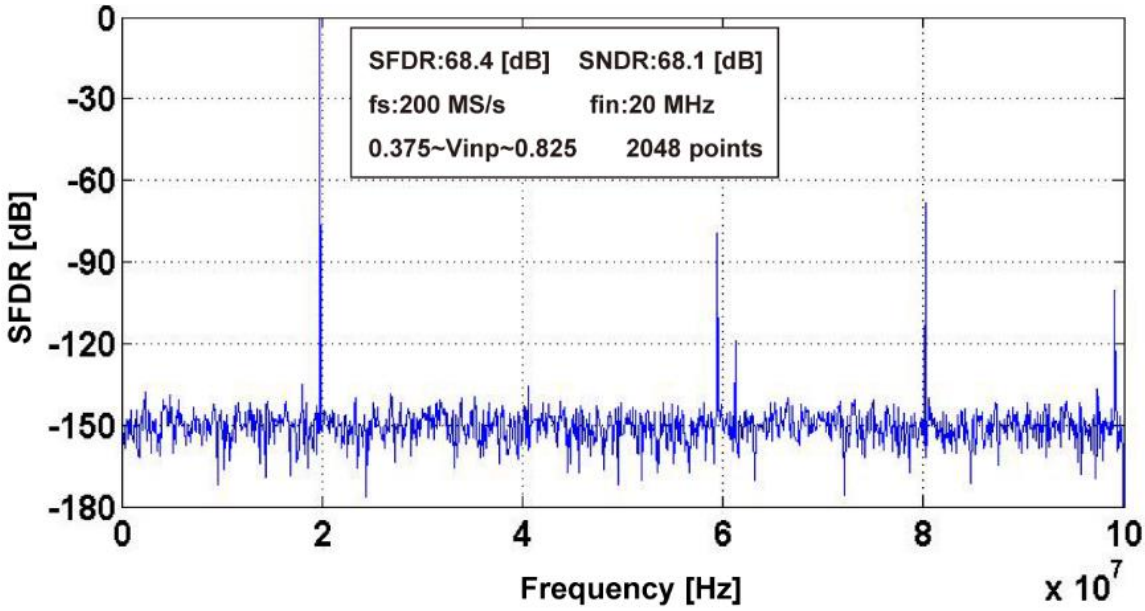
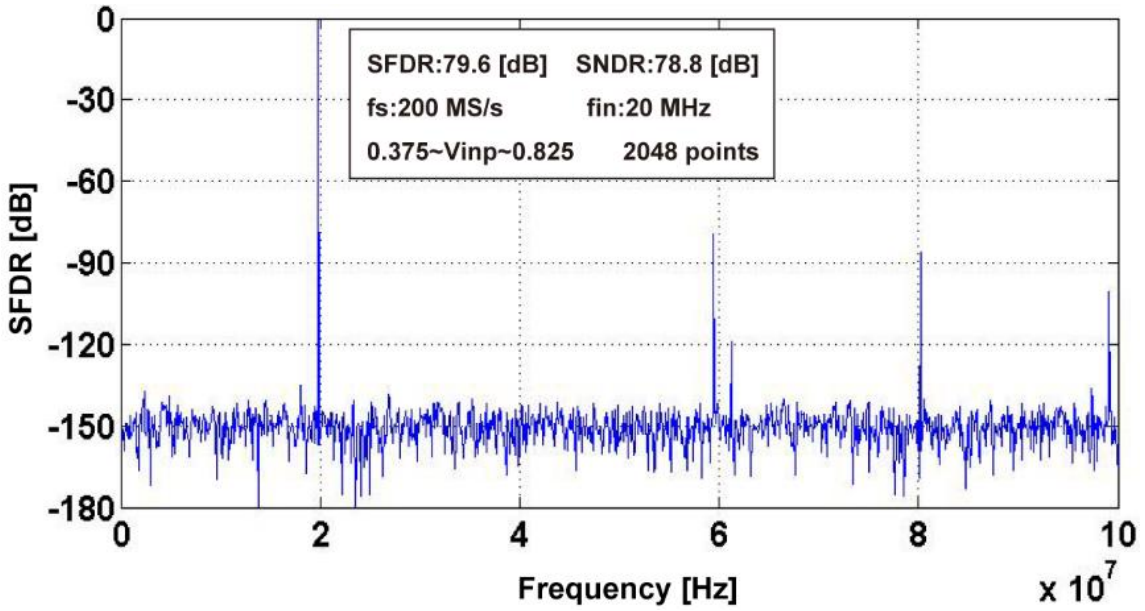


Fig.3.16. Bode diagram of the amplifier.

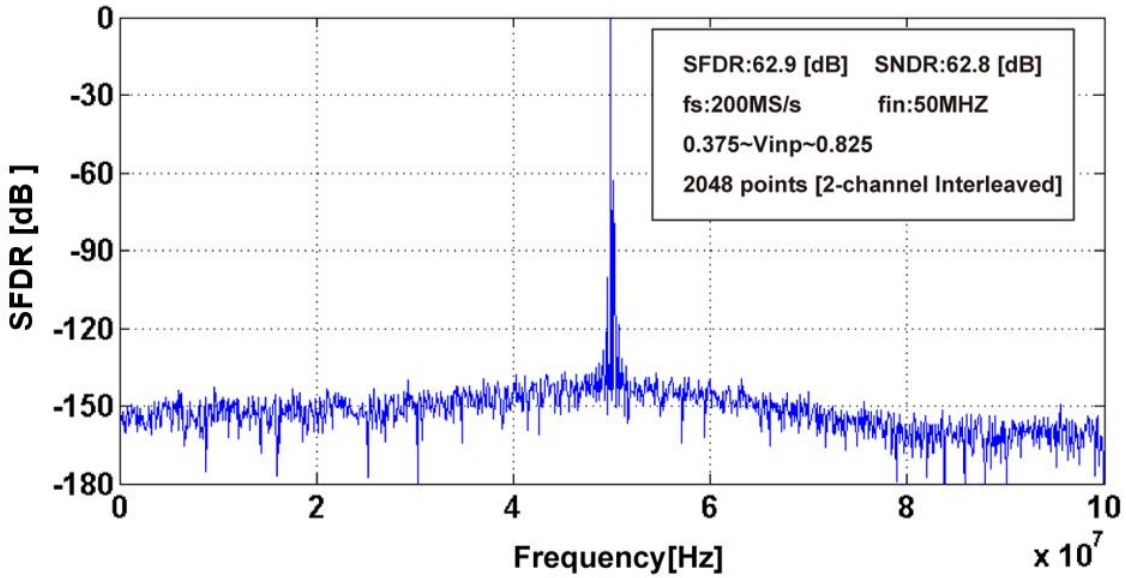


(a) Without calibration @20 MHz.

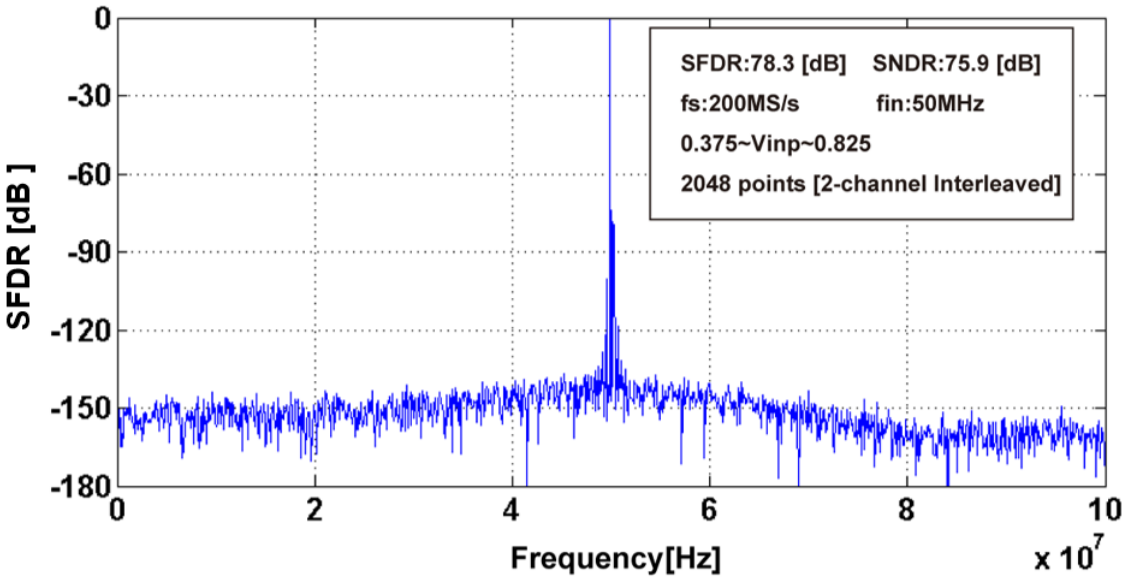


(b) With calibration@20 MHz.

Fig.3.17. FFT results for 20 MHz input with/without skew calibration.



(a) Without calibration @50 MHz.



(b) With calibration@50 MHz.

Fig.3.18. FFT results for 50 MHz input with/without skew calibration.

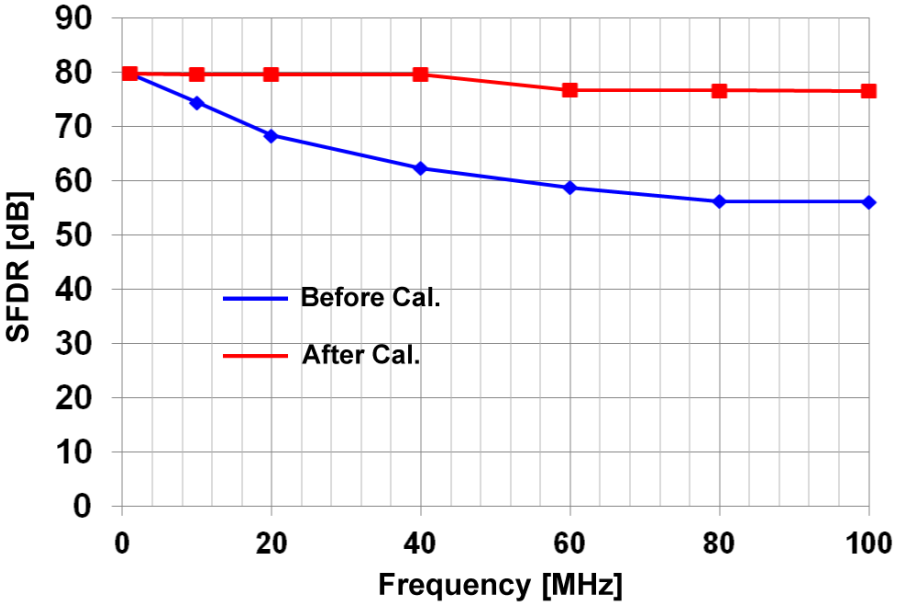


Fig.3.19. SFDR improvement before and after calibration.

TABLE 3.2

EFFECT OF CLOCK SKEW CALIBRATION (100 MHZ)

Clock Skew	SFDR (dB)
before calibration	57.1
after calibration	76.9

3.5 Conclusion

This chapter has studied clock skew calibration in sample-and-hold circuits for a time-interleaved ADCs. Clock skew in time-interleaved ADCs is caused by the mismatch due to process, voltage and temperature variations and it degrades the system performance. It becomes serious when input signal frequency is much higher. In order to calibrate the clock skew, the new approach of clock skew measurement and calibration used in sample-and-hold circuit is proposed. The proposed clock skew measurement circuit is an analog-based delay-locked loop circuit using a common SR latched based bang-bang phase detector and analog current-controlled delay lines.

The improvement result of clock skew calibration using circuit simulation base on 65-nm CMOS technology, we have found that after calibration the *SFDR* of the sample-and-hold circuit have been improved by 19.6 dB at Nyquist frequency. The simulation result shows the effectiveness of proposed clock skew measurement and calibration circuit.

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Chapter 4

A Column-Parallel Clock Skew Self-Calibration Circuit for Time-Resolved CMOS Image Sensors

This chapter reports a column-parallel clock skew self-calibration circuit for time-resolved (TR) CMOS image sensors. In TR CMOS imagers, as the time resolution increases, the skew of gating clock between pixels becomes a difficult problem because the clock skew causes the reduction of measurable maximum range in particular pixels or unmeasurable pixels. Thereby, simultaneous capturing for all the pixels cannot be achieved.

To calibrate the clock skew in short time, an electronics-only column-parallel multi-channel clock skew self-calibration circuit based on coarse-fine two-stage delay line and a dual low-skew clock tree is proposed in a time-of-flight (TOF) range imager which is a typical TR CMOS image sensor with high time resolution such as sub-millimeter range resolution. The experimental results show that the skew calibration circuit successfully reduces the clock skew from 247 ps_{rms} to 25 ps_{rms}, and the calibration time is only 12 μs, which is much faster than the previous work.

4.1 Introduction

TR CMOS image sensors have recently been paid much attention in applications of time-of-flight (TOF) range imaging [1, 2, 3, 4], biological imaging [5, 6, 7], and so on. A state-of-the-art TOF range imager[4] have been demonstrated the high range resolution of 0.3 mm, which corresponds to time resolution of 2 ps. Higher time resolution is strongly required for extending the application area of TOF imagers. As the time resolution increases, a skew of gating clock between pixels becomes a difficult problem, because the clock skew causes the reduction of measurable maximum range in particular pixels or unmeasurable pixels.

To address this problem, column-parallel skew calibration circuits have been proposed and demonstrated its effectiveness [4]. However, the calibration procedure takes a lot of time, because the delay characteristics of the skew calibration circuits are measured by using optical response and approximately 10^5 to 10^6 measurements or 1 to 9 hours are required for the skew calibration when the frame rate is 30 fps. Electronics-only self-calibration techniques are strongly desired for reducing calibration time and the cost of calibration. A lot of multi-channel skew self-calibration techniques have been reported in high-speed TiADCs [8, 9] as discussed in Chapter 1. However, the techniques used in the TiADCs targeted for relatively small number of channels are not suitable for the column-parallel multi-channel skew calibration in TR imagers which have typically more than 100 columns.

In this chapter, an electronics-only column-parallel multi-channel clock skew self-calibration circuit for highly TR imagers is proposed. The proposed self-calibration technique uses a coarse-fine two-stage delay line for each column and a dual low-skew clock tree for supplying skew-corrected gating pulses to a pixel area. This technique is effective for embedding the skew calibration circuit unit in the small pixel pitch while attaining the specified accuracy of skew calibrations. And the clock skew calibration circuit is a kind of digital-based delay-locked loop (DLL).

For a proof of concept, a typical TOF range imager with the proposed skew calibration circuitry is designed and implemented in 0.11-μm CMOS image sensor (CIS) technology, and the experimental results are shown to demonstrate its effectiveness.

The remaining sections are organized as follows. In Section 4.2, the column-parallel clock skew calibration circuit for TR imager is introduced and the key components are introduced in detail. A circuit simulation result and experimental result of clock skew calibration are given in Section 4.3 and 4.4 respectively. In final, a brief conclusion in drawn in Section 4.5.

4.2 Proposed Column-parallel Clock Skew Self-calibration Circuit for TR CMOS Image Sensors

In TR CMOS image sensor, a gating clock is supplied to pixels by column-parallel clock drivers. Because the clock driver has to drive a large capacitance due to a large number of gates in one pixel column, a large clock skew may occur between columns because of different delay from pixel to pixel. The skew includes both random and systematic components, which are mainly due to device mismatches (especially clock drivers) and a voltage drop of power supply line, respectively. The systematic skew due to the power-supply voltage drop of a clock driver is dominant according to [4]. If the skew is comparable or larger than the measurable range, each pixel has a different measureable range. Thereby, simultaneous capturing for all the pixels cannot be achieved [4].

The optical response column-parallel clock skew calibration circuit in [4] which has been proposed and demonstrated its effectiveness consists 2 stages for coarse and fine calibration respectively. Each stage has almost same design includes a voltage-controlled delay line (VCDL), a 7-bit current-steering digital-to-analog (DAC) and a 7-bit register. The value of each register can be set individually in every column. The skew calibration procedure in [4] are as follows: first, the skew before calibration is measured, when all the registers are set to an initial value that is close to the minimum delay condition. The measurement setup is shown in Fig.4.1. The skew is extracted from modulation characteristics by sweeping the delay of laser trigger as show in Fig.4.2. In the modulation characteristics, the skew is observed as a shift of the peak photocurrent. For the coarse calibration, the delay characteristics of the first stage of calibration circuits are measured in the same manner as the skew measurement. The modulation characteristics are measured while changing the register value. For these measurements, the register values of all the column are set to be identical. The delay characteristics is then extracted from them. From the delay characteristic, the register value of the first stage is chosen so that

the skew is minimized. Finally, fine calibration is performed in the same manner as of the coarse calibration [4].

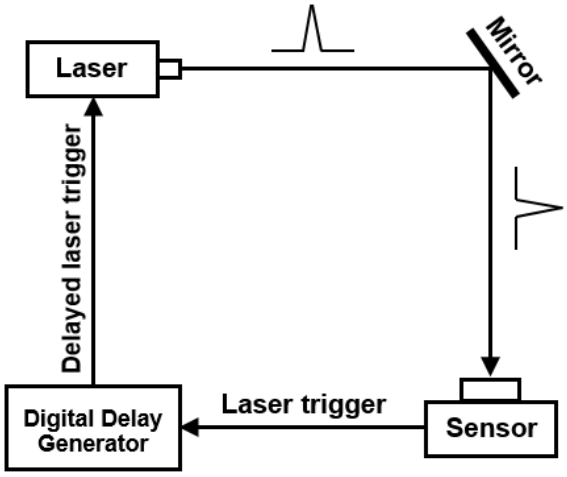


Fig. 4.1. Measurement setup.

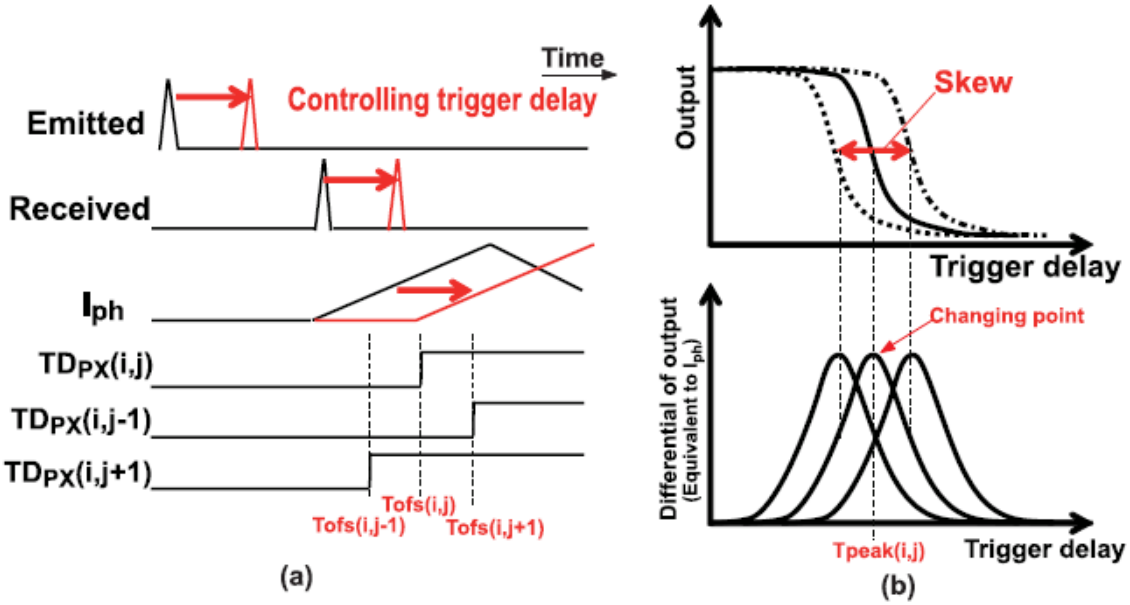


Fig.4.2. Measurement of skew from the modulation characteristic. (a) Measurement of modulation characteristic. (b) Modulation characteristic. [4]

However, this calibration procedure takes a lot of time, because the delay characteristics of the skew calibration circuits are measured by using optical response and long calibration time is required.

A new electronics-only column-parallel multi-channel clock skew self-calibration circuit as shown in Fig.4.3 is proposed. The principle of the proposed skew calibration

circuit is shown in Fig.4.4. A high-skew CLK_PIXs (w/o Cali.) is generated through a clock tree with clock driver. The high skew can be calibrated by a digital-based DLL circuit when a low-skew REF_CLKs are supplied by another clock tree without clock driver. The skew corrected CLK_PIXs (w/ Cali.) are used for the modulation pixels.

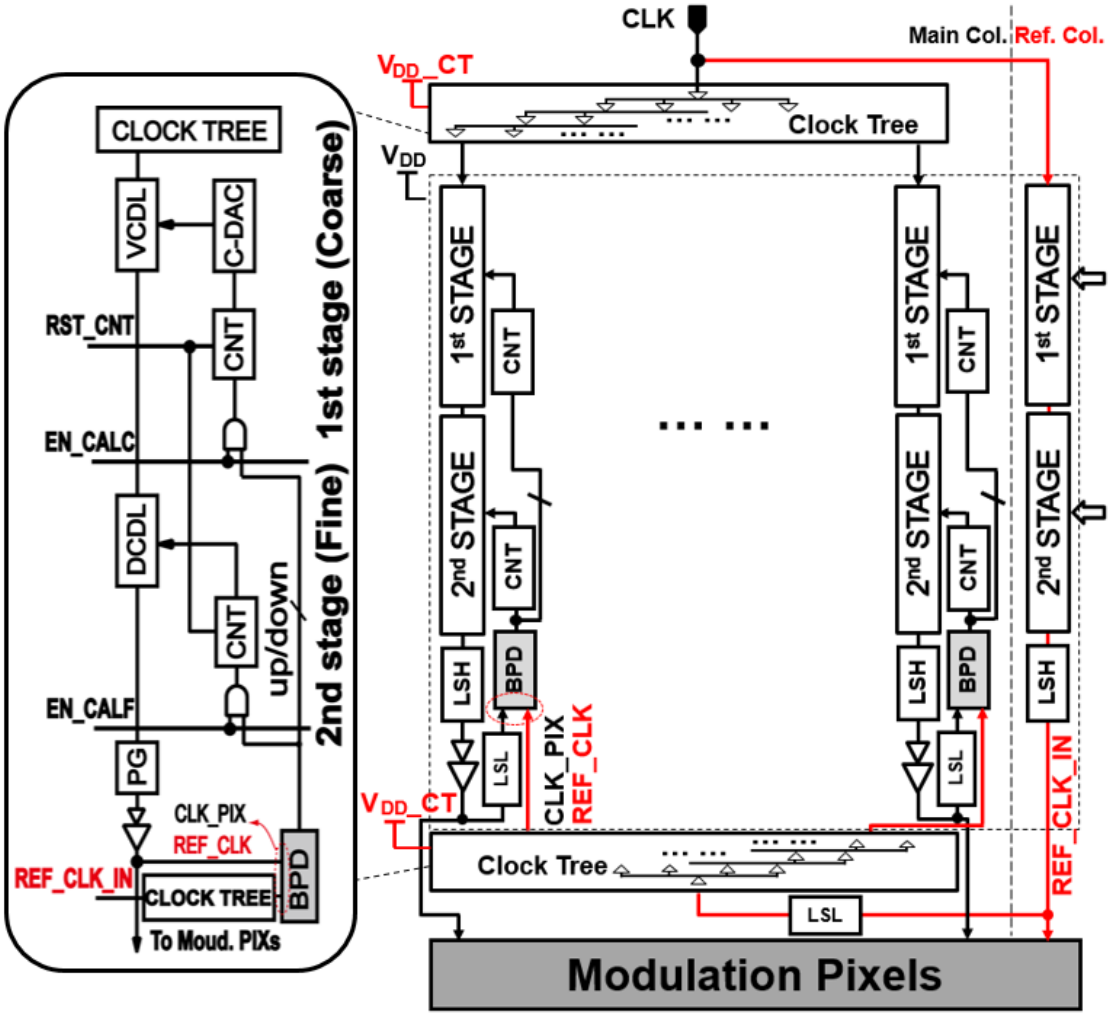


Fig. 4.3. Proposed clock skew calibration circuit.

The proposed calibration circuit consists of a bang-bang phase detector (BPD) based on a SR latch and a coarse-fine two-stage delay line. Each stage includes a 7-bit up-down binary counter (CNT). The amount of delay is controlled by the CNTs value. The first and second stages have a different calibration range and resolution, and are used for coarse and fine calibrations, respectively.

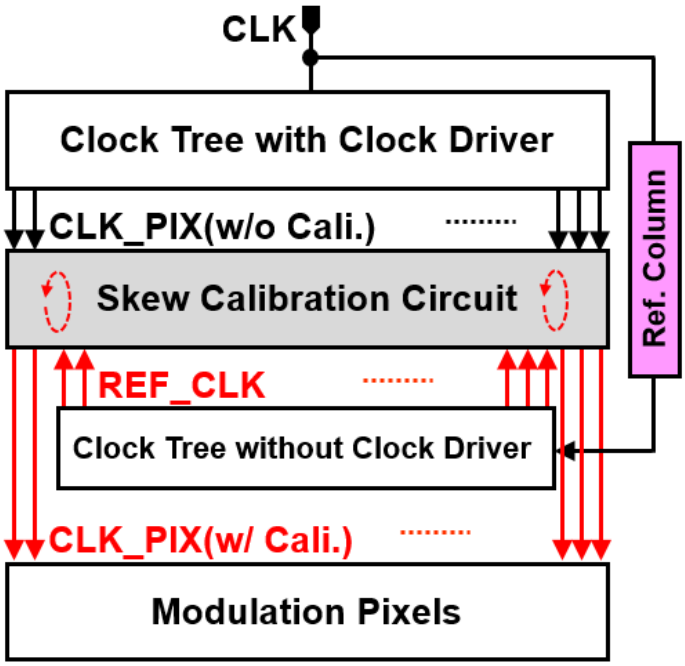


Fig. 4.4. The principle of proposed skew calibration circuit.

Besides the main column, it also includes a reference column with almost identical design to the main column. The reference column gives a reference gating clock, REF_CLK for the main column via a low-skew clock tree without clock driver. The BPD detects the phase difference between REF_CLK and a modulation clock of each column, CLK_PIX, and the results, i.e. up and down signals are counted by the CNTs only when enable signals (EN_CALC, EN_CALF) are asserted. As a result, the two-state delay line of each main column is controlled such that the skews between columns are minimized. Unlike the previous skew calibration circuit [4], the proposed circuit works as a bang-bang digital DLL, and realizes a short-time self-calibration without any optical response measurements. The level shifters to high and low levels (LSH and LSL, respectively) in the figure are necessary to meet a working voltage of gates in the pixel. A pattern generator (PG) is used for generating the gating clock as well as a CNT latch clock. The resulting frequency of the gating clock is one third of that of the input clock, CLK.

A phase diagram and timing chart of the skew calibration circuit is shown in Fig.4.5. The skew calibration is carried out only one time after power on, and then image capture begins: accumulation phase and readout phase are repeated. First, the CNTs of the first

and second stages are initialized by RST_CNT. The coarse calibration is then done when EN_CALC is asserted. After that, EN_CALF becomes high, and the fine calibration is carried out.

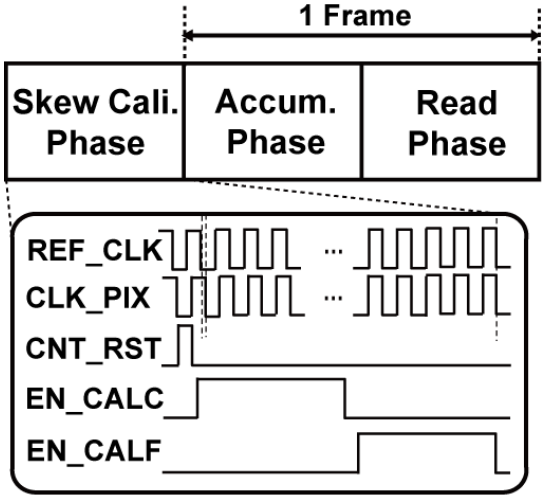


Fig. 4.5. Imager phase diagram and timing chart of skew calibration circuit.

4.2.1 Bang-bang Phase Detector

The BPD is widely used in digital phase-locked loops (PLLs) and DLLs [10]. Difference to the conventional phase detector (PD) or phase-frequency detector (PFD) which the output is linear to the phase difference of the inputs, the BPD detects the polarity of the phase difference only and lacks the magnitude of phase difference with the feature of no systematic timing offset.

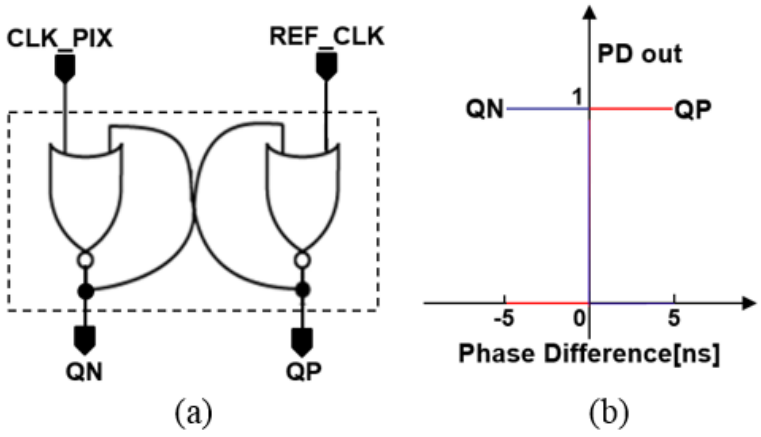


Fig. 4.6. (a) SR latch based BPD. (b) BPD phase characteristics.

In the study for the skew calibration circuit for TR imagers, the SR latch based BPD same as Chapter 3 is used as shown in Fig.4.6. (a). The detail of BPD is introduced in Chapter 3. It requires only eight transistors. The less number of transistors is suitable for the column-parallel skew calibration. The two inputs of an SR latch are assigned to CLK_PIX and REF_CLK. The outputs, QP and QN, are used for the up and down inputs of the CNT, respectively. The simulated phase characteristic of the BPD is shown in Fig.4.6. (b).

4.2.2 7-bit up-down Binary Counter

The CNT in this study is shown in Fig.4.7. The countdown counter can be constructed as follows, the inputs to the AND gates must come from the complement outputs instead of the normal outputs of the previous flip-flop. The up and down counters can be combined in one circuit to form a counter capable of counting either up or down.

For preventing the counting overflow, the counting prevention circuit is required for both up and down. For giving the initial value of the delay line in two stages, the initial code (A_0~ A_6) of the CNTs are 1111111 and 0111111 for first and second stage, respectively.

4.2.3 Voltage-controlled Delay Line

As shown in Fig.4.8, the first stage of the delay generator uses a VCDL controlled by the CNT via a 7-bit DAC. In the current-steering DAC as shown in Fig.4.9， binary-weighted current source generates an amount of current that depends on a 7-bit code (A_0~ A_6) from CNT. The total code-dependent current is copied to the current source in the VCDL, which controls the amount of delay in the falling edge of the input clock.

The unit current I_{UNIT} is 0.5 μA, the simulation results in Fig.4.10 show the delay correction range and delay correction step as a function of digital code. The VCDL has the delay correction range of 1.84 ns and the step of maximally 210 ps. The VCDL has a nonlinear and wide range characteristics suitable for coarse calibration.

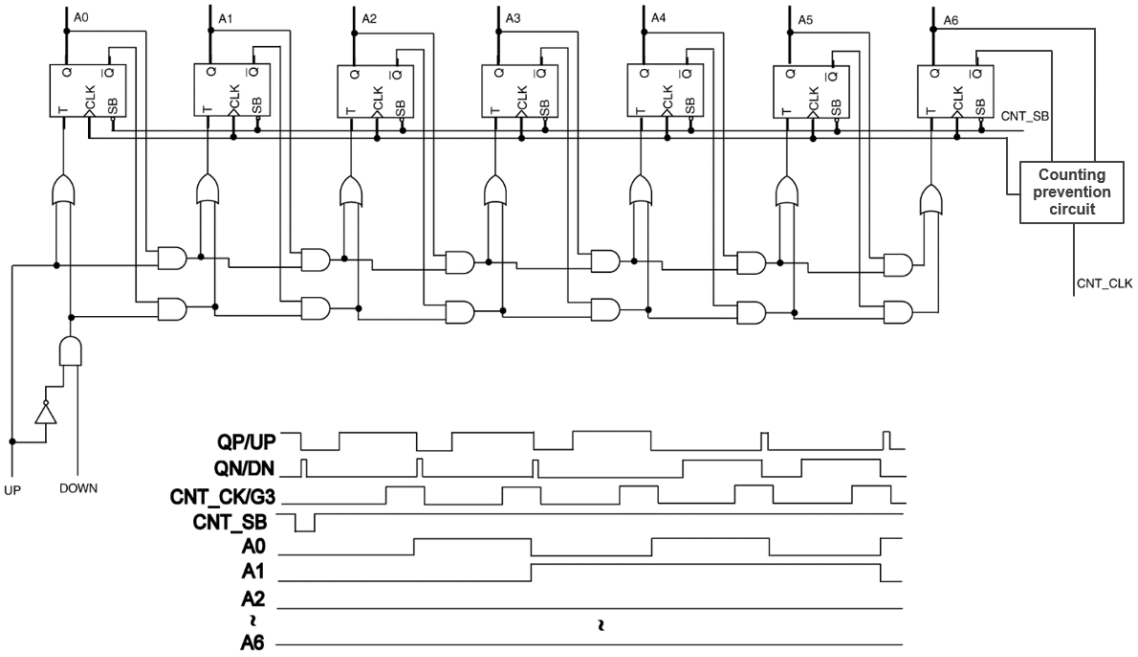


Fig.4.7. 7-bit up-down counter.

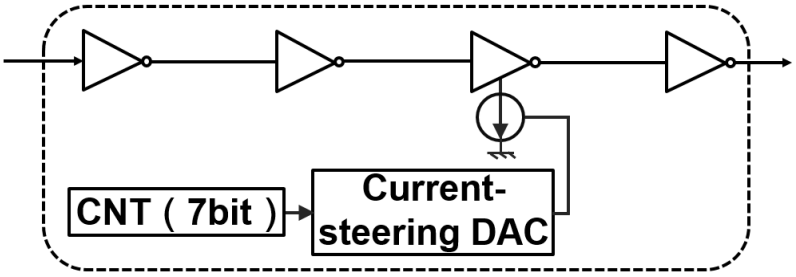


Fig.4.8. Voltage-controlled delay line (VCDL).

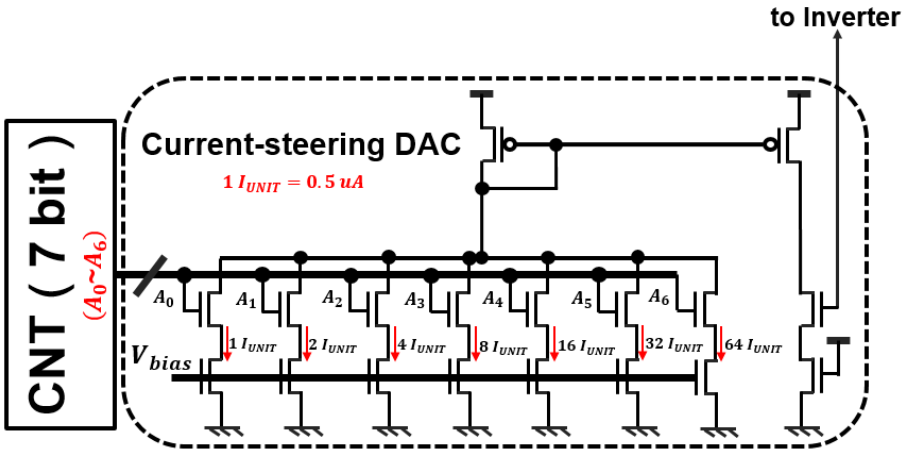


Fig.4.9. Current-steering DAC.

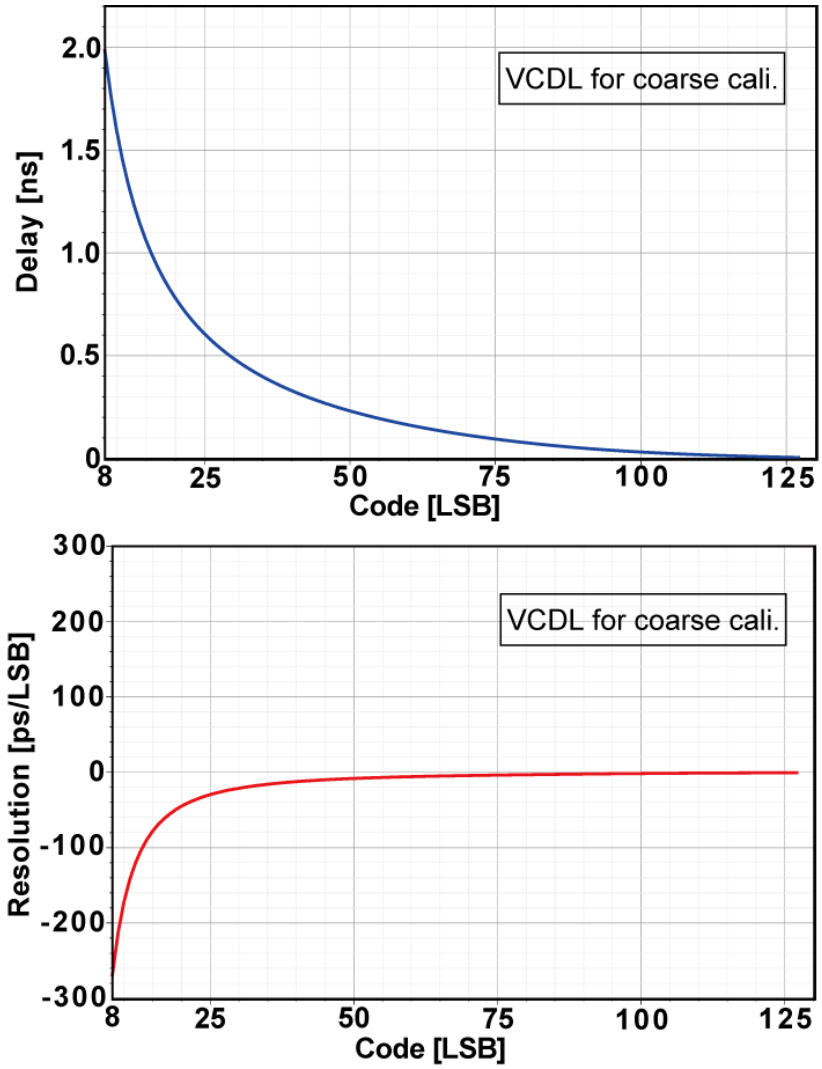


Fig.4.10. Delay characteristics of VCDL.

4.2.4 Digitally-controlled Delay Line

As shown in Fig.4.11, the second stage of the delay generator uses a digitally-controlled delay line (DCDL) in which the delay is adjusted by changing the value of variable load capacitors [11]. The variable load capacitors consists of MOS transistors, the gate capacitance of MOS transistor is a function of bias voltage. Shorting the drain and source nodes of the transistor and digitally controlling this shorted node changes the value of the gate capacitance, moreover the binary-weighted number of transistors gives binary-weighted gate capacitance. Creating an array of such digitally controlled transistors with binary-weighted number results in a digitally controlled capacitive load. A 7-bit CNT is

used for the digital controlling and the high to low order outputs (A_0~ A_6) of CNT are connected to the corresponding binary-weighted transistor. A series of 3 cascaded delay cells which are controlled by the same digitally control from same CNT are used to compensate the expected timing skew and to limit the change in delay per delay cell to a fraction of its delay.

The delay of DCDL $\triangle t_d$, assuming a switching point at half the voltage supply, is

$$\Delta t_d = \Delta C_L \frac{V_{DD}}{2 \times I_{inv}} \tag{4.1}$$

where V_{DD} is the voltage supply, $\triangle C_L$ is the changing value of the load capacitor and I_{inv} is the inverter drive current. As shown in Fig.4.12, the DCDL has the simulated correction range of 360 ps with the delay step of approximately 2.8 ps. The simulated result also show the linearity of delay versus digital code. Because of the linear code-dependent delay characteristic and high resolution, the DCDL is suitable for fine calibration for second stage.

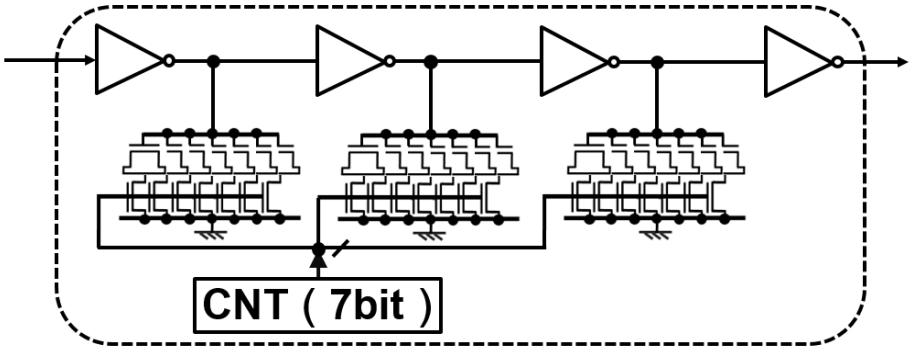


Fig.4.11. Digitally-controlled delay line (DCDL).

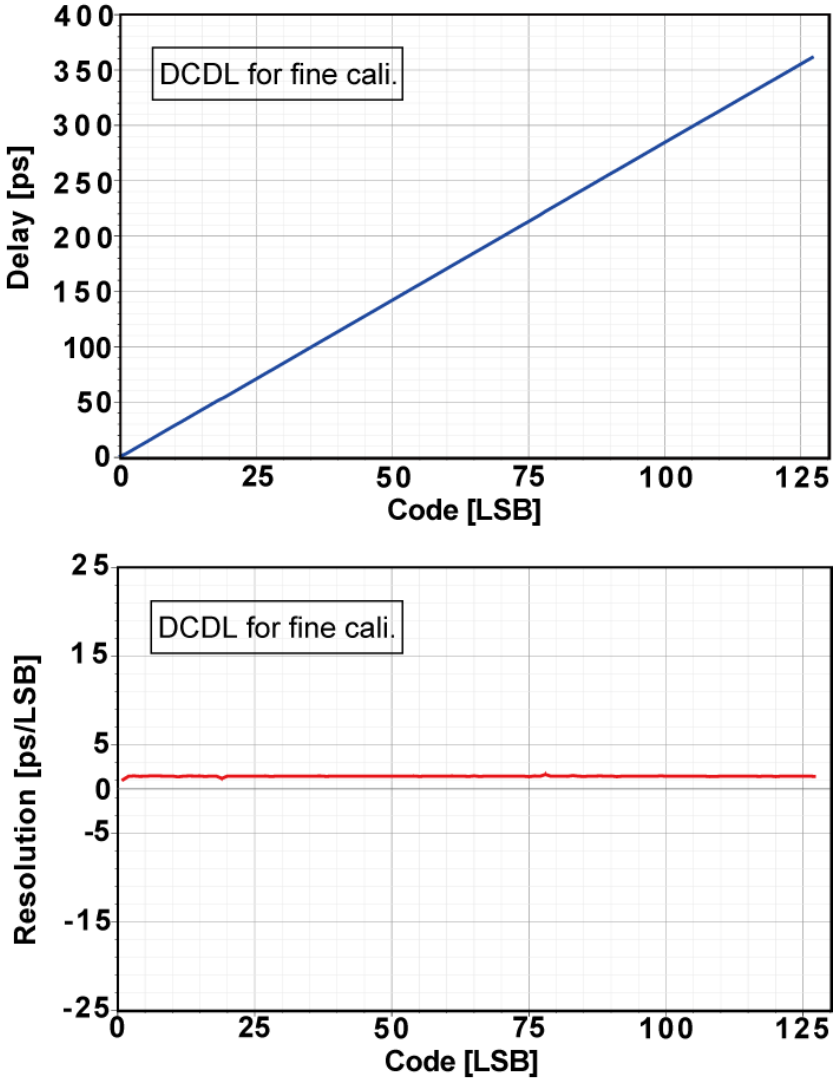


Fig.4.12. Delay characteristics of DCDL.

4.2.5 Low-skew Clock Tree

In the clock skew calibration circuit, two clock trees are used; one is for the gating clock drivers supplied to pixels and another one is without clock drivers which is for the reference clocks. The clock tree for distributing the reference clocks into all the columns is a key point of the design. Since the load capacitance of inverters in the clock tree is much smaller than that of the modulation clock drivers connected to pixels in each column, the clock skew due to the clock tree is also much smaller than that of the clock drivers. However, the skew due to the clock tree remains after skew calibration. For this reason, to minimize the clock skew in the reference clock tree, a carefully designed low-skew

clock tree is strongly required. The clock tree layout is carefully designed to meet symmetricity, and the power supply lines for the reference clock tree are separated from other parts of power supply lines in this design.

As shown in Fig.4.13, in the post-layout simulation, the estimated systematic skew is approximately 10.59 $ps_{p\text{-}p}$, which is sufficient for the application in TR imagers.

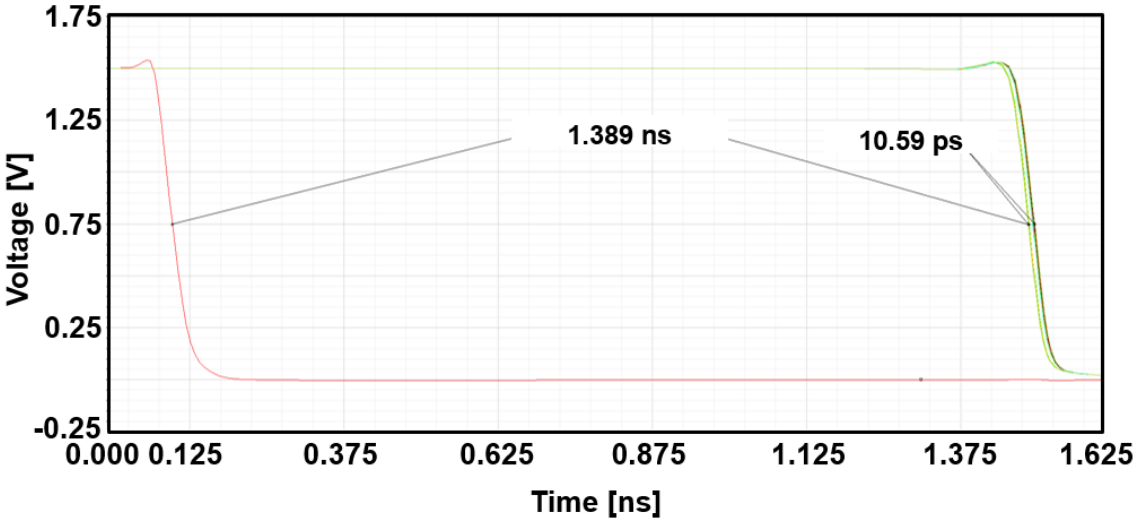


Fig.4.13. Clock skew in low-skew clock tree.

TABLE 4.1

CLOCK SKEW OF CLOCK TREE (POST-LAYOUT SIMULATION)

Layout	Skew ($ps_{p\text{-}p}$)
Asymmetric	294.41
Symmetric	10.59

4.3 Simulation Results

Simulation results for the clock skew calibration are shown in Fig.4.14. In this simulation, the different delays are given at two columns as an initial skew before calibration and the residual skews after calibration are simulated for the cases calibrated with the first stage only (VCDL only) and both the first and second stages (VCDL and DCDL). After the calibration with the first stage only, the skew of 122.8 ps_{rms} still remains. After the calibration with the first and second stages, the residual skew is reduced to 2.3 ps_{rms}.

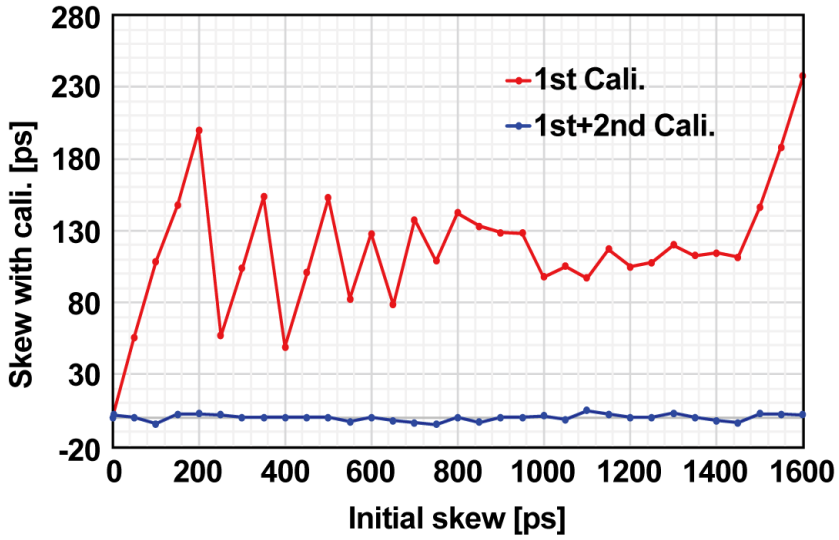


Fig.4.14. Simulated skew with calibration.

TABLE 4.2

EFFECT OF CLOCK SKEW CALIBRATION (SIMULATION)

Skew	Standard deviation (ps_{rms})
1^{st} calibration(Coarse only)	122.8
1^{st} +2^{nd} calibration(Coarse and Fine)	2.3

4.4 Experimental Results

In order to demonstrate the proposed skew calibration circuit, a typical TOF range imager is implemented using 0.11-μm CIS technology. The prototype has a pixel array of 256 (H) x 8 (V) and the column pinch is 22.4 μm. The unit pixel has 45 high-speed charge modulators based on lateral-electric-field-modulation (LEFM) [12], and those are connected in parallel. The configuration of the LEFM detectors is similar to draining-only modulation (DOM) [3], i.e. the modulator has three outputs with one drain. In this study, only main pixels (200 (H) x 4 (V)) and the output of one tap from each pixel are characterized for the purpose to prove the concept of the proposed skew calibration technique. The input clock and gating clock frequencies are set to 100 MHz, and 33 MHz, respectively. The chip micro-photograph is shown in Fig.4.15 and the specification is summarized in Table 4.3.

The skew is characterized with the same manner as the previous work [4]. The amount of delays in the pixel response waveform to a short laser pulse is measured for every columns. The measurement setup is same as Fig.4.1, the experimental setup is shown in Fig.4.16.

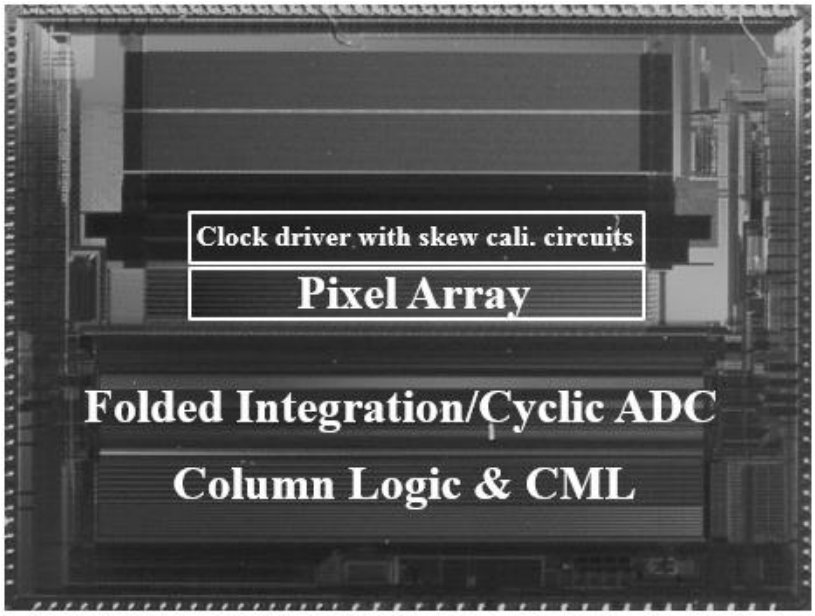


Fig.4.15. Chip micro-photograph.

TABLE 4.3

SUMMARY OF THE SPECIFICATION OF CHIP

Parameter	Value
Technology	0.11-μm CIS
Total pixels	256 (H) x 8 (V)
Main pixels	200 (H) x 4 (V)
Column pitch	22.4-μm
Input clock frequency	100 MHz
Gating clock frequency	33 MHz

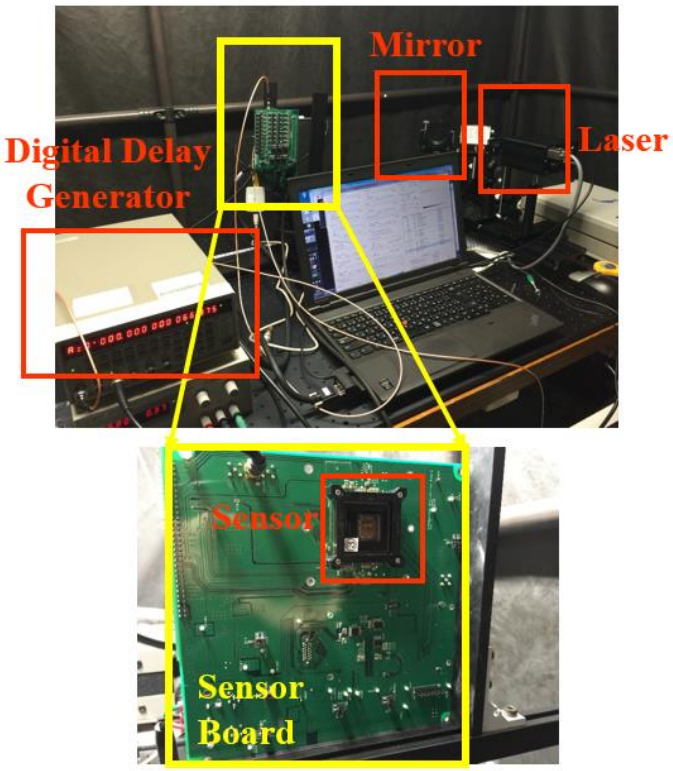


Fig.4.16. Experimental setup.

The measured skews with and without calibrations are shown in Fig.4.17, the clock skew due to the code for setting calibration step (formed as register value of EN_CAL) is shown in Fig.4.18, the distribution of clock skew in shown in Fig.4.19, with calibration, the skew is reduced from 247 ps_{rms} to 65 ps_{rms} and 25 ps_{rms} for the calibrations with the first stage only and both the first and second stages, respectively. The calibration time is only 12 μs,

which is much shorter than that of the previous work [4].

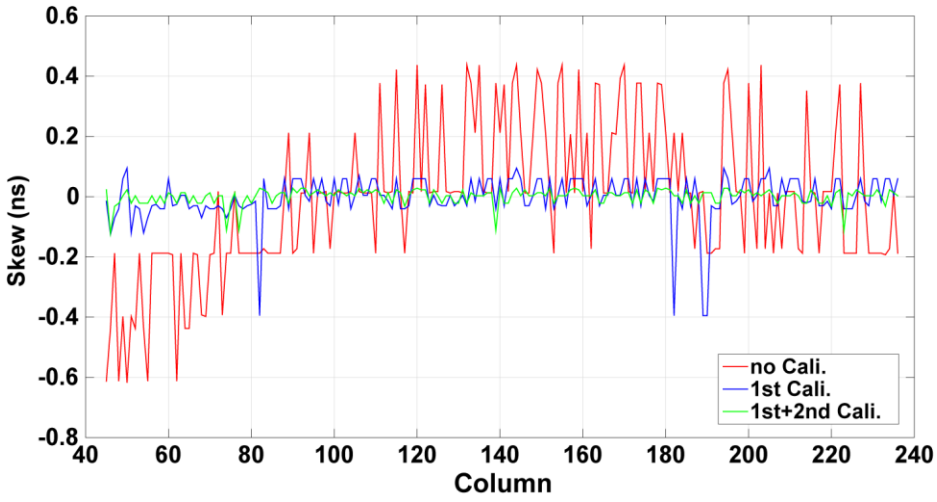


Fig.4.17. Measured skew without and with calibration.

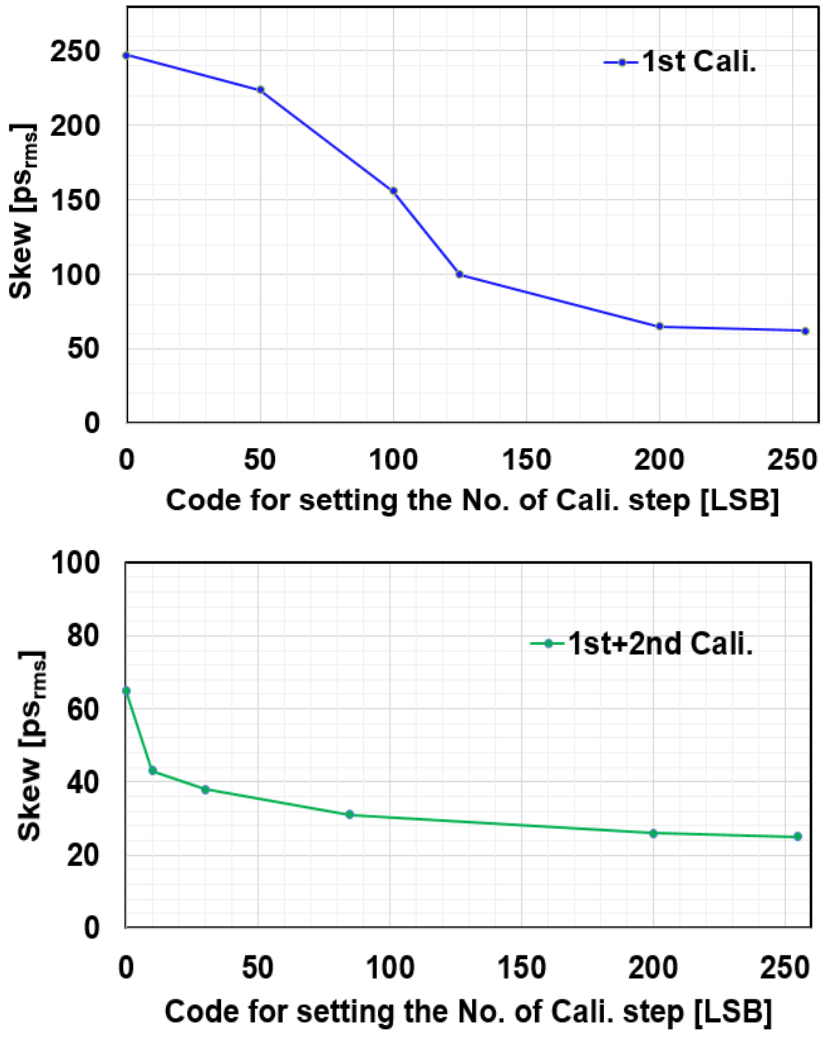
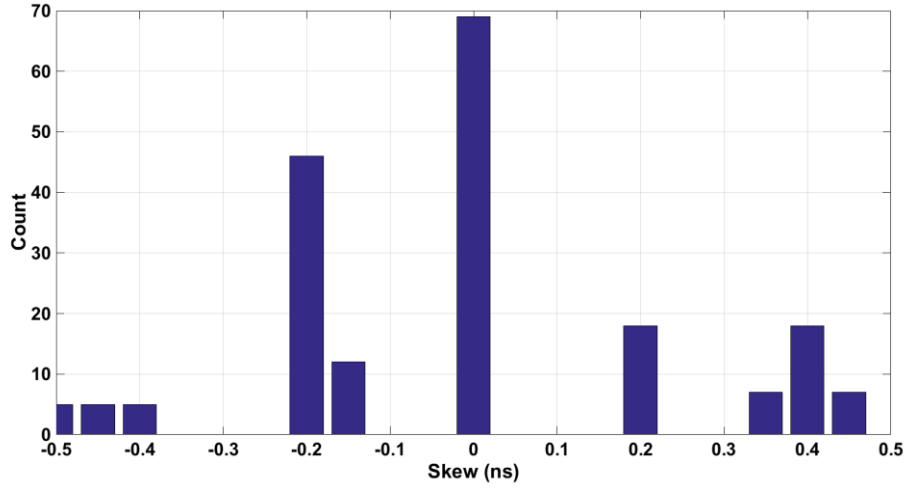
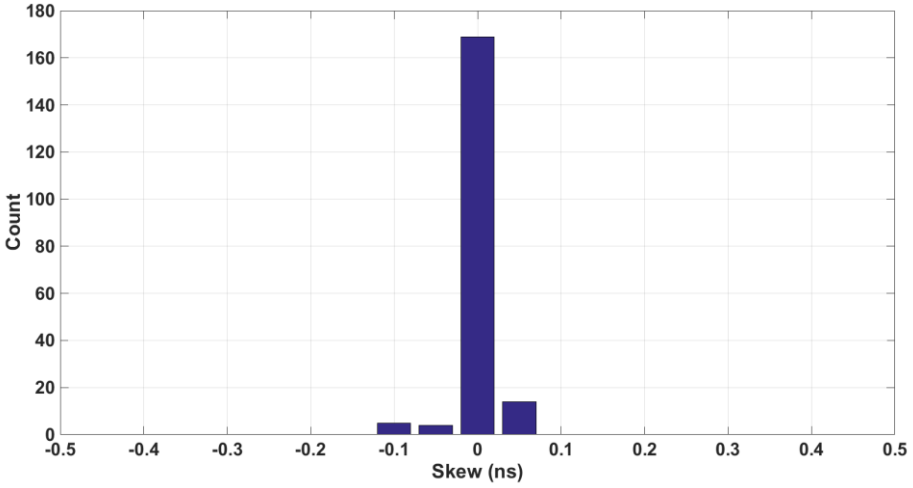


Fig.4.18. The clock skew due to calibration step (formed as EN_CAL resister value).



(a)



(b)

Fig.4.19. (a) Distribution of clock skew without calibration. (b) Distribution of clock skew with 1st and 2nd stage calibration

TABLE 4.4

EFFECT OF CLOCK SKEW CALIBRATION (MEASUREMENT)

Clock skew	Standard deviation (ps_{rms})
no calibration	247
1st Calibration(Coarse only)	65
1st +2nd Calibration(Coarse and Fine)	25

TABLE 4.5

SPEED OF CLOCK SKEW CALIBRATION

Technique	Calibration time
Optical response method in [4]	1-9 hrs
Electronic-only self-calibration method in [13]	12 μs

4.5 Conclusion

This chapter descries an electronics-only column-parallel multi-channel clock skew self-calibration circuit for a typical time-resolved CMOS image sensors. The two-stage delay line comprised with voltage-controlled delay line and digitally-controlled delay line covers a wide calibration range with high resolution and the dual low-skew clock tree technique is essential for controlling clock skews of all the pixels within a specified tolerance range of skews. The experiment results of the prototype chip shows that the clock skew has been reduced from 247 ps_{rms} to 25 ps_{rms} with short calibration time. This technique can widely be used for time-resolved CMOS image sensors.

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[13] Lianghua Miao, Keita Yasutomi, Shoma Imanishi, and Shoji Kawahito, "A Colum-Parallel Clock Skew Self-Calibration Circuit for Time-Resolved CMOS Image Sensors", IEICE Electronics Express, Vol. 12, No. 24, pp. 1-7, Dec., 2015.

Chapter 5

Conclusion

This thesis has studied the clock skew calibration for time-interleaved analog-to-digital converters (TiADCs) and time-resolved (TR) CMOS image sensors. The clock skew causes a lot of serious problems both in TiADCs and TR CMOS image sensors. In order to calibrate the clock skew in TiADCs and TR CMOS image sensors, the clock skew calibration methods are proposed and their effectiveness are demonstrated for these two devices.

TiADCs are considered to achieve high speed and high resolution data conversion by using M-channel low-speed ADCs working in parallel. However, the TiADCs are sensitive to the mismatches between the channels. The clock skew is caused different delay between channels dues to process, voltage and temperature variations and it degrades the system performance. The sampling error due to the clock skew becomes serious when input signal frequency is much higher. In order to calibrate the clock skew, a new and effective clock skew measurement and calibration technique is proposed. The proposed new clock skew measurement circuit is using analog-based delay-locked loop (DLL) and a common phase detector.

To investigate the effectiveness of proposed clock skew calibration in TiADCs, a 2-

channel 200 MHz time-interleaved sample-and-hold (S/H) circuits for a 12-bit pipeline ADC based TiADC is designed using 65-nm CMOS technology. When the 6 ps skew at Nyquist frequency (100 MHz) is injected to the channels, the spur-free dynamic range (*SFDR*) is improved from 57.1 dB before calibration to 76.9 dB after calibration, an improvement is 19.6 dB. The simulation results also show the sampling error as a result of clock skew becomes serious when input signal frequency is much higher. The simulation results investigate the effectiveness of the proposed clock skew calibration circuits for TiADCs.

On the other hand, this thesis also describes an electronics-only column-parallel multi-channel clock skew self-calibration circuits for TR CMOS image sensors. TR CMOS image sensors have recently been paid much attention in applications of time-of-flight (TOF) range imaging, biological imaging, and so on. In TR CMOS imagers, a gating clock is supplied to pixels by column-parallel clock drivers. Because the clock driver has to drive a large capacitance due to a large number of gates in one pixel column, a large clock skew may occur between columns because of different delay from pixel to pixel. The skew includes both random and systematic components, which are mainly due to device mismatches (especially clock drivers) and a voltage drop of power supply line, respectively. The systematic clock skew due to the power-supply voltage drop of a clock driver is dominant. As the time resolution of TR imagers increases, for example, TR imager with high time resolution such as sub-millimeter range, a clock skew of gating clock between pixels becomes a serious problem, because the clock skew causes the reduction of measurable maximum range in particular pixels or unmeasurable pixels. To address this problem, column-parallel skew calibration circuits have been proposed and demonstrated its effectiveness in previous work. However, the calibration procedure takes a lot of time, because the delay characteristics of the skew calibration circuits are measured by using optical response and approximately 10^5 to 10^6 measurements or 1 to 9 hours are required for the skew calibration when the frame rate is 30 fps. Electronics-only self-calibration techniques are desired for reduced calibration time and the cost of calibration. A lot of multi-channel skew self-calibration techniques have been reported in

high-speed TiADCs. However, compared to the clock skew calibration techniques in TiADCs targeted for relatively small number of channels, it is more difficult for the clock skew calibration in TR imagers which have typically more than 100 columns.

In this thesis, an electronic-only column-parallel multi-channel clock skew self-calibration circuit for highly TR imagers is proposed. The proposed clock skew calibration technique is a method of digital-based DLL. It uses a coarse-fine two-stage delay line for each column and a dual low-skew clock tree for supplying skew-corrected gating pulses to a pixel area.

The coarse-fine two-stage delay line comprised with voltage-controlled delay line (VCDL) and digitally-controlled delay line (DCDL) covers a wide calibration range with high resolution. The dual low-skew clock tree technique is essential for controlling clock skews of all the pixels within a specified tolerance range of skews. This technique is effective for embedding the skew calibration circuit unit in the small pixel pitch while attaining the specified accuracy of skew calibrations.

For a proof of concept, a typical TOF image sensor with the proposed skew calibration circuitry is designed and implemented in 0.11-μm CMOS image sensor (CIS) technology, and the experimental results are shown to demonstrate its effectiveness. The experiment results of the prototype chip shows that the clock skew has been reduced from 247 ps_{rms} to 25 ps_{rms}, an improvement is 225 ps_{rms}. The calibration time in this work is 12 μs which is much faster than the previous work. This technique can widely be used for TR CMOS image sensors.

List of Publications

Journal Papers

1. Lianghua Miao, Keita Yasutomi, Shoma Imanishi, and Shoji Kawahito, "A Colum-Parallel Clock Skew Self-Calibration Circuit for Time-Resolved CMOS Image Sensors", IEICE Electronics Express, Vol. 12, No. 24, pp. 1-7, Dec., 2015.

2. Sung-Wook JUN, Lianghua MIAO, Keita YASUTOMI, Keiichiro KAGAWA, and Shoji KAWAHITO, "Design of a Digitally Error-Corrected Pipeline ADC using Incomplete Settling of Pre-charged Residue Amplifiers," IEICE Trans. Electron., Vol.E96-C, No.6, JUNE, 2013.

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1. L.Miao, S.Kawahito, “A Study on Bandwidth Mismatch Calibration for Time-interleaved A/D Converter”, Inter-Academia 2011, iAY18, Sep. 2011.

2. L.Miao, S.Kawahito, "Skew Measurement and Calibration in Interleaved Sample-and-Hold Circuits", STARC SYMPOSIUM 2013, Jan. 2013.

National Symposia and workshops

1. Lianghua MIAO, Keita YASUTOMI, Keiichiro KAGAWA, and Shoji KAWAHITO, " Bandwidth Mismatch Calibration for a Time-interleaved A/D Converter Using Sampling Pulse Width Modification", The 2012 IEICE GENERAL CONFERENCE, C-12-38, Mar. 2012.

2. Lianghua Miao, Sung-Wook Jun, Keita Yasutomi, Keiichiro Kagawa, and Shoji Kawahito, "Clock Skew Measurement and Calibration in Time-Interleaved ADCs", Tokai-section Joint Conference on Electrical and Related Engineering2013, G2-5, Sep. 2013.

3. Lianghua MIAO, Keita YASUTOMI, Keiichiro KAGAWA, and Shoji KAWAHITO, "Clock Skew Measurement and Calibration in Time-Interleaved ADCs Using Racing Circuits", The 2014 IEICE GENERAL CONFERENCE, C-12-9, Mar. 2014.

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