A Study on High-Speed Low-Noise Readout Architectures and Column A/D Converters for CMOS Image Sensors

（課程博士・様式７）（Doctoral qualification by coursework,Form 7）

学 位 論 文 要 旨

Abstract of Doctoral Thesis

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論文題目：CMOS イメージセンサの高速低ノイズ信号読み出しアーキテクチャとカラム A/D 変換器に関する研究

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論文要旨：

Abstract：

In this thesis, the readout architectures and readout circuits of CMOS image sensors have been particularly studied for high-performance imaging systems, including: 1) high-speed readout architectures, 2) high-speed low-noise column-parallel readout circuits, 3) performance-enhanced column-parallel analog-to-digital converters (ADCs), and 4) a digital calibration technique to enhance the linearity of high-resolution folding-integration/cyclic cascaded (FICC) ADCs. These studies are conducted with two prototype chip implementations in two projects, respectively, which have been summarized as follows.

Firstly, a fully pipeline readout architecture has been proposed and implemented by using a low-power high-speed hybrid tri-stage-pipeline (TSP) column ADC with two-stage column cache structure in 65 nm CMOS technology. Time of pre-charge for source-follow (SF) driver inside of pixel is provided by pipeline readout fashion to improve the overall readout speed of large pixel array. To conduct fully pipeline readout fashion, a hybrid high-speed low-power TSP column ADC with 12-bit resolution and 1.2 V power supply has been proposed and implemented, which contains a 4-bit folding-integration (FI) ADC as the first stage to perform multiple-sampling and suppress noise, a 5-bit cyclic ADC as the second stage, and a 5-bit single-slope (SS) ADC as the third stage to increase power efficiency. A two-stage cache structure has been proposed and integrated in column circuits to handle the data generated from two column pixels by one shared column TSP ADC corresponding to two column pixels. Furthermore, to enhance the speed of the FI ADC, a pipeline sampling technique has

been proposed and implemented with the only cost of one additional capacitor and several additional switches. The prototype imager with this fully pipeline readout architecture has been fabricated in 65 nm CMOS technology. 1.767 μs of 1-horizontal readout time is achieved according to the simulation results. The function of proposed speed-enhanced FI ADC has been verified by measurement results. The basic functions of proposed TSP ADC with column cache have been confirmed by measurement results from prototype chips.

Secondly, a high-speed low-noise column-parallel readout circuits have been developed which is composed of an analog buffer and a performance-enhanced FICC ADC. Since the SF driver inside of the pixel is unable to drive the column FICC ADC in high-speed operation, a high-speed analog buffer is employed in this design to achieve requirement of high-speed readout of image sensor. Two techniques have been proposed and implemented to enhance the performance of the FICC ADC. One is the pre-charging technique to improve the sampling speed and reduce settling related error as well as error from historical code dependency during FI operation. The other is variable-threshold-voltage (VTV) technique to enhance the linearity of the FICC ADC. Moreover, a quad-horizontal parallel readout architecture of pixel array has been proposed and implemented in this design to further increase the readout speed by 4 times comparing with conventional one-side rolling-shutter readout architecture. This high-speed architecture and circuits design has been implemented in 110 nm CMOS technology with a low-noise pixel structure. The measurement results from prototype chips achieve 0.44 e$^-$ random read noise and 32 frames per second (fps) with 752 (H) × 700 (V) pixel array under 776 mW power consumption in total, which yield a figure of merit (FoM) of column ADC 0.04 pJe$^-$/conversion-step. The obtained FoM of column ADC in this low noise imager is the best one among reported state-of-the-art CMOS image sensors all over the world at this moment.

Lastly, a digital calibration technique has been proposed and simulated to enhance the linearity of the FICC ADC with 18-bit resolution. This calibration technique is done by compensation of non-ideal errors in digital domain based on the numerical modeling of the FICC ADC. The ideal model and the model with errors generated during both each converting cycle and the final effects of them are calculated according to the behaviors of the FICC ADC, respectively. The simulation results show that the maximum integral nonlinearity (INL) is improved from +69.2/-78 LSBs to +1.23/-1.1 LSBs, and the differential nonlinearity (DNL) is decreased from +19.3/-1.88 LSBs to +0.12/-0.33 LSBs for 18-bit resolution after calibration. Both high-resolution and high-linearity have been achieved by employing the proposed digital calibration technique simultaneously.