# A 2V 3.8□W Fully-Integrated Clocked AC-DC Charge Pump with 0.5V 500Ω Vibration Energy Harvester

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# A 2V 3.8μW Fully-Integrated Clocked AC-DC Charge Pump with 0.5V 500Ω Vibration Energy Harvester

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***Abstract*—This paper proposes a clocked AC-DC voltage multiplier to enable full integration of power converters into a sensor/RF chip even with low voltage micro-watt vibration energy harvesting such as electromagnetic or magnetostrictive energy transducer operating at a low resonant frequency of 10Hz-1kHz. Relationships of output voltage-output current and input current-output voltage are also formulated together with the open circuit voltage amplitude and the output impedance of the transducer. The modeling and the performance of the proposed voltage multiplier are validated by SPICE simulation and measured results of the prototype chip fabricated in a 65nm 1V CMOS process. As a result, the proposed integrated circuit can output a target power of 3.8$\mu$W at an output voltage of 2V from a magnetostrictive energy transducer with an available output power of 63μW and an output impedance of 500Ω.**

***Keywords*—AC-DC, IoT, Charge pump, Energy harvesting, Vibration, Electromagnetic, Magnetostrictive.**

## NOMENCLATURE

| | |
|---|---|
| C | Capacitance per stage |
| $f_{CLK}$ | Frequency of a clock generated by ring oscillator |
| $f_{IN}$ | Frequency of harvester's output power |
| $I_{CP}$ | Input current of the charge pump |
| $I_{OSC}$ | Current driving the oscillator |
| $I_{OUT}$ | Output current of the charge pump |
| $I_S$ | Diode saturation current |
| N | Stage number of the charge pump |
| $P_{CP}$ | Input power of the charge pump |
| $P_{EH}$ | Power generated by energy harvesting |
| $P_{LOSS}$ | Power loss in the charge pump |
| $P_{OSC}$ | Power of the oscillator |
| $P_{OUT}$ | Output power of the charge pump |
| $P_{RE}$ | Reactive power |
| $P_{TOT}$ | Power of the system |
| $R_{EH}$ | Output impedance of energy transducer |
| $R_{TOT}$ | Total output impedance of the system |
| $V_{DD}$ | AC input voltage amplitude |
| $V_{OUT}$ | Output voltage of the charge pump |
| $V_{REC}$ | Rectified voltage |
| $V_{SS}$ | Ground |
| $V_{TH}^{EFF}$ | Effective threshold voltage of diode |
| $V_T$ | Thermal voltage |
| $\beta$ | Ratio of parasitic capacitance to C |
| $\theta_S$ | Phase at which the output current begins to flow |

## I. INTRODUCTION

Internet-of Things (IoT) is being developed to realize the connected world. It is desired to operate IoT devices without batteries for cost reduction. Energy harvesting (EH) [1] [2] is a technology to harvest energy from environment. It is realized by a combination of energy transducer (ET) and power converters. Because the voltage obtained by electromagnetic and magnetostrictive vibration EH (VEH) is too low to directly drive building blocks (BBs) such as Sensor, RF and DSP, it is necessary to boost the voltage using a voltage multiplier (VM) (Fig. 1). Several types of boost schemes have been proposed for VEH [3]-[6]. In [3], AC-DC charge pump (CP), which has been used for RF energy harvesting and RFID, is used for VEH as well. Due to a low frequency operation of VEH, discrete capacitors of 1μF and diodes are required. The other types of boost schemes have a rectifier followed by a booster: a switched capacitor technique with adaptive control [4] and DC-DC CP [5]. These systems can output tens of micro-watt with VEH, but require a discrete capacitor for rectification. In [6], a switching regulator is used as booster to output 1mW with 76% power efficiency. However, it cannot be fully integrated, because a discrete capacitor and an inductor are required. As a result, full integration of the boost circuit for low voltage output VEH has not been achieved to the best of our knowledge. The authors have proposed a concept of clocked AC-DC converters which can be ideally fully integrated and reduce reactive power for micro-watt VEH in [7] and [8]. In [7], we discussed the circuit modeling of the clocked AC-DC converters under the condition that the AC power supply is ideal with zero impedance. It was theoretically shown that the power conversion efficiency could be improved and the output power could increase. In [8], simulation results of the converter system in term of the output power and input power over the clock frequency are also reported. However, modeling of the system including both the clocked AC-DC converter and the vibration energy transducer has not been done. In this paper, the modeling expands by taking the output impedance of the vibration energy transducer $R_{EH}$ into

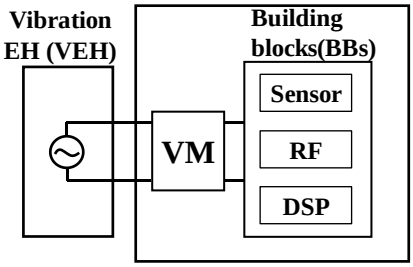



Fig. 1. Target IC for IoT/EH

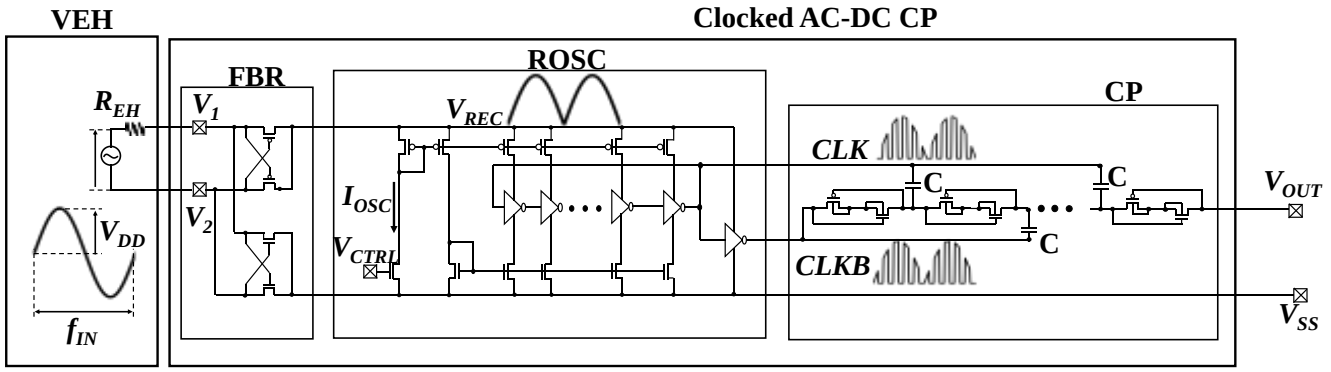



Fig. 2. System diagram of the clocked AC-DC CP
(FBR: full-bridge rectifier, ROSC: ring oscillator)

consideration. Its validation is also reported based on both SPICE simulation and measurement results of the system fabricated in 65nm 1.0V CMOS. The performance of the proposed system is compared with the existing techniques. Measured results of the output power as a function of the vibration frequency are also reported.

## II. Modeling of Clocked AC-DC CP with VEH

Fig. 2 shows a diagram of the proposed clocked AC-DC CP. The power generated by VEH is rectified by a full-bridge rectifier (FBR). A cross-coupled CMOS bridge circuit [9] is used. The clock frequency ($f_{CLK}$) is increased by a ring oscillator (ROSC). In order to measure the dependency of the output current ($I_{OUT}$) and input power ($P_{CP}$) on the clock frequency ($f_{CLK}$), the operation current of the ROSC ($I_{OSC}$) can be controlled externally by $V_{CTRL}$ in the test chip. Once the optimum $f_{CLK}$ is determined so as to have a maximum output current at a target output voltage, one can design ROSC without any control terminal for mass production. Thus, no discrete capacitor is needed for $V_{REC}$. Diode-connected CMOS transistors were used for the diode portion of CP [10]. Since $V_{OUT}$ is the power supply for the subsequent building blocks, a regulator is required at the output stage.

When the input voltage of the CP is $V_{DD}\sin\theta$, $I_{OUT}$ of the proposed circuit is expressed by (1) when $f_{CLK} >> f_{IN}$ using a model of DC-DC CP [11] where $R_{TOT}$ is the total output resistance of the system including CP and VEH (2) [12].

$$I_{OUT}(\theta)= \frac{1}{R_{TOT}}\left\{\left(\frac{N}{1+\beta}+1\right) V_{DD}\sin\theta-(N+1)V_{TH}^{EFF}-V_{OUT}\right\} \quad (1)$$

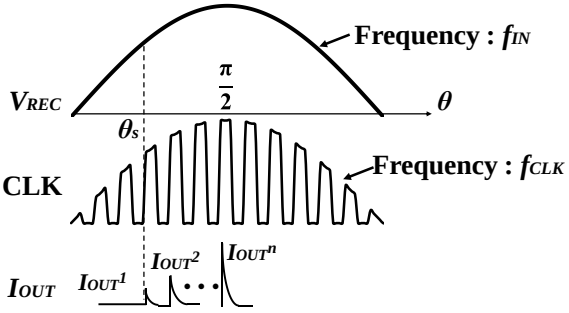



Fig. 3. Waveform of the clocked AC-DC CP

$$R_{TOT} = \frac{N}{(1+\beta)Cf_{CLK}}+R_{EH}(N+1)^2 \quad (2)$$

Let $\theta_s$ be the phase at which the current begins flowing, i.e., $I_{OUT}(\theta_s) = 0$

$$\theta_s = \sin^{-1}\left[\frac{1+\beta}{V_{DD}(1+\beta+N)}\left\{V_{OUT}+(N+1)V_{TH}^{EFF}\right\}\right] \quad (3)$$

where $V_{TH}^{EFF}$ is the effective threshold voltage of the diode given by (4) [11].

$$V_{TH}^{EFF} = V_T \ln\left(\frac{\sqrt[1]{4^{N+1}}(1+\beta)f_{CLK}CV_T}{I_s}\right) \quad (4)$$

In the proposed circuit, the amplitude of the clock and $I_{OUT}$ vary with $\theta$. $I_{OUT}{}^k$, an average $I_{OUT}$ over a k-th period, is given by (5) as illustrated in Fig. 3. It is assumed that ROSC is designed to have $f_{CLK}$ with negligibly small voltage dependency. $\overline{I_{OUT}}$, an

$$I_{OUT}{}^k = \frac{1}{R_{TOT}}\left\{\left(\frac{N}{1+\beta}+1\right) V_{DD}\sin\left(\theta_s+k\times\frac{2\pi f_{IN}}{f_{CLK}}\right)-(N+1)V_{TH}^{EFF}-V_{OUT}\right\} \quad (5)$$

$$\overline{I_{OUT}} = \frac{2}{\pi}\times\sum_{k=1}^{n} I_{OUT}{}^k = \frac{2}{\pi}\left(\frac{1}{R_{TOT}}\right)\left[\left(\frac{N}{1+\beta}+1\right)\cos\theta_s-\left(\frac{\pi}{2}-\theta_s\right)\left\{(N+1)V_{TH}^{EFF}+V_{OUT}\right\}\right] \quad (6)$$

$$P_{CP} = \frac{2}{\pi}\times\int_{\theta_s}^{\frac{\pi}{2}} I_{CP}(\theta)V_{DD}\sin\theta\,d\theta = \frac{2}{\pi}\left[\frac{1}{4}\left(\frac{1}{R_{TOT}}\right)\left\{\left(\frac{N}{1+\beta}+1\right)^2 V_{DD}^2\left\{2\left(\frac{\pi}{2}-\theta_s\right)+\sin 2\theta_s\right\}-\left(\frac{N}{1+\beta}+1\right)V_{DD}\left((N+1)V_{TH}^{EFF}+V_{OUT}\right)\cos\theta_s\right\}+\frac{1}{4}\left(\frac{\beta}{1+\beta}\right)f_{CLK}NCV_{DD}^2\left\{2\left(\frac{\pi}{2}-\theta_s\right)+\sin 2\theta_s\right\}\right] \quad (7)$$

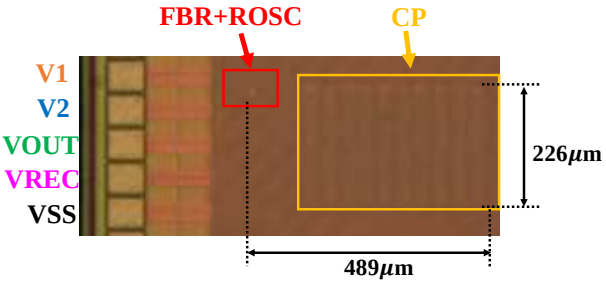



Fig. 4. Die photo of the proposed system with N=9, and C=10pF

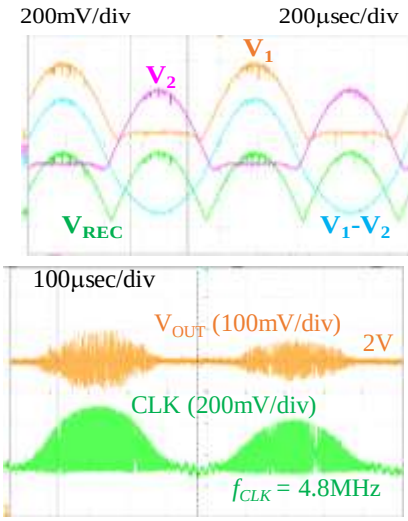



Fig. 5. Measured waveform

average $I_{OUT(\theta)}$ over $1/f_{IN}$, is calculated to be (6). One can calculate the power efficiency of the proposed circuit ($\eta_{CP}$) as follows. The input power of the CP ($P_{CP}$) is calculated by an average of the product of the input current of CP ($I_{CP}$) and the input voltage over a cycle time, given by (7) as in [13]. The input power of the proposed circuit ($P_{TOT}$) contains the input power of OSC ($P_{OSC}$).

$$P_{TOT} = P_{CP} + P_{OSC} \tag{8}$$

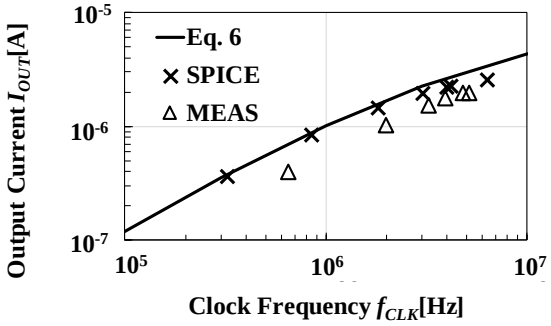
$P_{OUT}$ is obtained by the product of $\overline{I_{OUT}}$ and $V_{OUT}$. Therefore, $\eta_{CP}$ is defined by (9).

$$\eta_{CP} = \frac{\overline{I_{OUT}} \times V_{OUT}}{P_{TOT}} \tag{9}$$

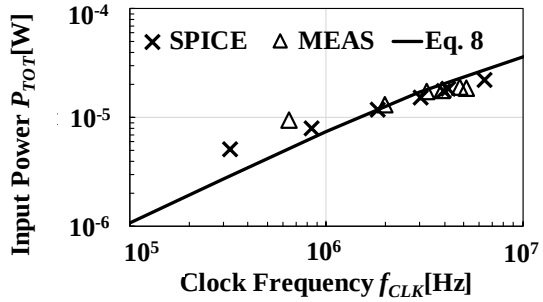
As a result, it is expected from (6) that $I_{OUT}$ increases in proportion to $f_{CLK}$ as far as it is not too high. When $f_{CLK}$ is as high as an inverse of a time constant of $R_{TOT}$ × NC, CLK and CLKB couldn't have full amplitude. As shown in (7), it is also expected that $P_{CP}$ increases as well as $I_{OUT}$, which would degrade power efficiency. However, the largest $I_{OUT}$ must be prioritized rather than the highest power efficiency when VEH outputs a specific power.

## III. Measurement and Discussion

In order to validate the proposed circuit system, it was fabricated in 65nm 1V CMOS as shown in Fig. 4. AC-DC CP was designed with N = 9 and C = 10pF for a target of $I_{OUT}$ > 1μA at $V_{OUT}$ = 2V. A CMOS diode was well modeled with a




(a) $\overline{I_{OUT}}$ as a function of $f_{CLK}$




(b) $P_{TOT}$ as a function of $f_{CLK}$

Fig. 6. Comparisons of $\overline{I_{OUT}}$ and $P_{TOT}$ ($R_{EH}$=500Ω)

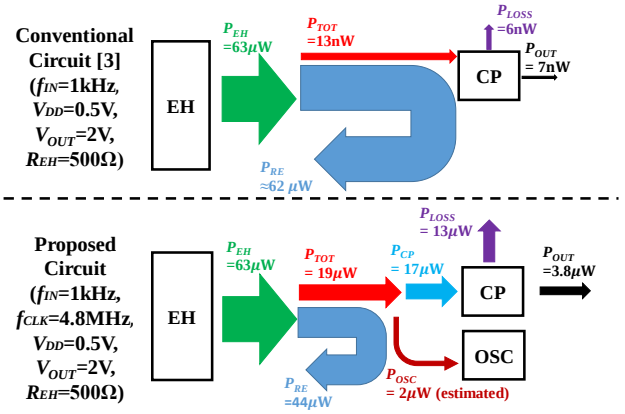



Fig. 7. Power distribution chart (C=10pF, N=9)

saturation current of 39nA based on the I - V model of a PN diode. VEH was modeled with an ideal AC source whose voltage amplitude is 0.5V, $R_{EH}$ of 500Ω [14], and $f_{IN}$ of 1kHz unless otherwise stated. The area of the circuit system was 0.11mm$^2$. Even with $V_{OUT}$ = 2V, any two terminals of any 1V transistor does not go beyond 1V. Only isolated P-well to N-well and N-well to P-sub receive > 1V. Fig. 5 shows a measured waveform of the proposed circuit in case of $f_{CLK}$ = 4.8MHz. Fig. 6 (a) shows $\overline{I_{OUT}}$ as a function of $f_{CLK}$. The model (6) is in good agreement with SPICE simulation results within an error of 5% at $f_{CLK} \leq$ 1MHz. When $f_{CLK}$ is excessively high, the model (6) and measured value deviates the simulated curve. This is because the clock drivers' output resistance is not considered in (6). The measured value agreed with SPICE simulation results with an error of 10 ~ 40%. It was not possible to measure at $f_{CLK}$ > 5MHz because the frequency was saturated. $P_{OUT}$ reached its maximum of 3.8μW at $f_{CLK}$ = 4.8MHz. Fig. 6 (b) shows $P_{TOT}$ as a function of $f_{CLK}$. $\eta_{CP}$ was 21% at $f_{CLK}$ = 4.8MHz. Fig. 7

Table I. Comparison on the characteristics (C: capacitor, D: diode, L: coil, *1: $P_{OUT}$ to $P_{TOT}$, *2: $P_{OUT}$ to $P_{EH}$)

| | Boosting Method | Discrete Element | Circuit Area | Power Efficiency | | | | Technology |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ | $V_{OUT}$ | $P_{OUT}$ | $R_{EH}$ | |
| [3] | AC-DC CP | 3C + 4D | Discrete | 25% (*1) | | | | - |
| | | | | N.A. | 2V | 30μW | N.A. | |
| [4] | Rectifier + Switched capacitor | 1C | 0.58mm$^2$+4.84mm$^2$ | 37% (*2) | | | | 0.35$\mu$m CMOS |
| | | | | 1.2V | 2V | 33μW | 2kΩ | |
| [5] | Rectifier + DC-DC CP | 1C | N.A. | 13% (*2) | | | | 90nm CMOS |
| | | | | 0.5V | 1.8V | 3.2μW | 180Ω | |
| [6] | Rectifier + Switching regulator | 1C + 1L | 1.6×1.6 mm$^2$ | 76% (*2) | | | | 0.18$\mu$m CMOS |
| | | | | 0.6V | 1V | 1mW | 120Ω | |
| **This work** | Rectifier + Clocked AC-DC CP | None | 0.11mm$^2$ | 21% (*1), 6% (*2) | | | | 65nm CMOS |
| | | | | 0.5V | 2V | 3.8μW | 500Ω | |

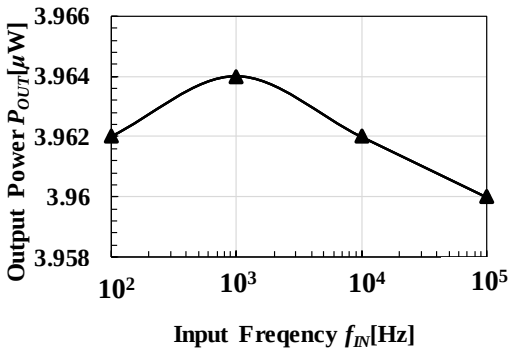



Fig. 8. Measured $P_{OUT}$ as a function of $f_{IN}$ ($f_{CLK}$=4.8MHz, $R_{EH}$=500Ω)

compares the power distribution for the conventional AC-DC CP and the proposed circuit. When a conventional circuit [3] was measured under the same condition as the proposed circuit, the simulation result and the measured value had negative $P_{OUT}$ due to a leakage current as high as an expected output current of about 10nA. Therefore, the ideal value of the conventional circuit estimated by the formula [15] and the measured value of the proposed circuit were compared in Fig. 7. 542X higher $P_{OUT}$ is achieved with a trade-off against a reduction in $\eta_{CP}$ by a factor of 2.5. The proposed circuit generated $P_{OUT}$ of 3.8μW whereas the conventional circuit with the same circuit area does $P_{OUT}$ of 36nW. $P_{OSC}$ is estimated to be about 10% of $P_{CP}$ at $f_{CLK}$ = 4.8MHz. The proposed circuit requires more $P_{TOT}$ than the conventional one due to the addition of the ROSC. However, system power efficiency, $\eta_{SYS} \equiv P_{OUT}/P_{EH}$, is improved over the conventional one because the increase in $P_{TOT}$ can be obtained from the reactive power $P_{RE}$. In other words, $\eta_{SYS}$ can be increased by a factor of 542 as far as $P_{TOT} < P_{EH}$. In the conventional AC-DC CP, $P_{OUT}$ varies in proportion to $f_{IN}$. Therefore, a dedicated circuit design is needed for every VEHs with a different resonant frequency. On the other hand, as shown in Fig. 8, $P_{OUT}$ of the proposed circuit has negligibly small dependency on $f_{IN}$. Therefore, a universal design can be applied to various VEHs with different resonant frequencies, which can significantly decrease design cost. Table. I compares the prior art and the proposed circuit. Although this work is the worst in power conversion efficiency (note that power efficiency is defined by $P_{OUT}$ / $P_{TOT}$ or $P_{OUT}$ / $P_{EH}$ as respectively shown by *1 or *2 by paper), full integration is realized as far as the subsequent building blocks require μW power.

## IV. Summary

In this paper, modeling of the clocked AC-DC voltage multiplier system is proposed for low output voltage micro-watt electromagnetic and magnetostrictive VEHs. Even when the VEH has $R_{EH}$ of 500Ω, one can obtain 3.8μW power with a minimal area overhead of 0.11mm$^2$ without using large discrete capacitors when the input frequency of 1kHz is increased to 4.8MHz by the on-chip oscillator at an open circuit voltage of 0.5V. As a results, it is possible to integrate the voltage multipliers for the VEHs in IoT chips. Also, the proposed circuit has negligibly small dependency of $P_{OUT}$ on $f_{IN}$. This means that a universal design can be applied to various VEHs with different resonant frequencies. One may have an opportunity to further increase $P_{OUT}$ by improving oscillators in such a way that a faster clock can be generated at an extremely low voltage.

## Acknowledgment

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