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An Interface Circuit for Capacitive Sensors

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SUMMARY An active circuit for detecting a small capacitance change accurately with a minimum number of components is presented for interfacing a capacitive sensor with a digital system. No component trimming is required and the sensitivity to circuit constants is minimum. Thus, it meets all the requirements for the on-chip interface.

1. Introduction

Many sensors are now being developed which detect such physical quantities as pressure, displacement, humidity, touch, and acceleration in the form of the capacitance change. The capacitance change of such sensors is usually very small compared with their offset capacitance, and thus the ultimate sensitivity depends largely on the signal processing circuit. Besides the signal-to-noise ratio, the on-chip integralability and the microprocessor compatible output are prerequisite to the interface of a "smart" sensor[1],[2]. One of such candidates is the switched-capacitor capacitance bridge[3]-[5]. This bridge meets the requirement of the on-chip integralability, but suffers from the clock feedthrough accompanied with the analog switch.

Another candidate is the AC operated charge amplifier[6]. The circuit configuration is simple enough, but the sensitivity adjustment by means of the phase difference between the two sinusoidal sources plagues the practical design. To alleviate this difficulty, a charge amplifier is developed which allows the easy adjustment of the sensitivity by means of the amplitude of the quadrature sinusoidal source. This letter describes the interface based on this improved charge amplifier. The experimental results confirming its principles of operation are also given.

2. Circuit Description

Figure 1 shows the circuit diagram of the interface. Here, C_x represents a capacitive sensor. C_c and C_s are reference capacitors for cancelling the offset capacitance C_0 of the sensor and for adjusting the sensitivity, respectively. These capacitors are driven by three sinusoidal sources with the following phase relations ; v_0 and v_c are 180° out-of-phase, and v_0 and v_s are in phase quadrature. The op-amp A_1 forms the charge amplifier to take the weighted sum of the charges stored in C_x, C_c, and C_s. The resistor R_f provides the bias current path of op-amp A_1, and is chosen such that $\omega C_f R_f \gg 1$. If the amplitude of v_c is adjusted such that $\alpha_c C_c = C_0$ hold, then the output voltage v_1 of op-amp A_1 is given by

$$v_1 = -V\frac{\sqrt{(\Delta C)^2+(\alpha_s C_s)^2}}{C_f}\cos(\omega t-\theta) \qquad (1)$$

where θ is the phase difference between v_1 and v_s given by

$$\theta = \tan^{-1}\frac{\Delta C}{\alpha_s C_s}. \qquad (2)$$

The phasor diagram of v_1, normalized to $-V/C_f$, is depicted in Fig. 2. It is clear from Eqs. (1) and (2) and Fig. 2 that if $\Delta C \ll \alpha_s C_s$, then ΔC changes θ linearly while keeping the amplitude of v_1 almost constant. The sensitivity, defined as $\partial\theta/\partial(\Delta C/C_s)$, is then given by $1/\alpha_s$, and thus can be adjusted by the amplitude of v_s.

Two comparators A_2 and A_3 operates as the zero-cross detectors. Comparing the symmetrical rectangular outputs of A_2 and A_3, the EXOR gate converts the phase difference into the pulse width T. The digital output is finally obtained by counting the high frequency clock

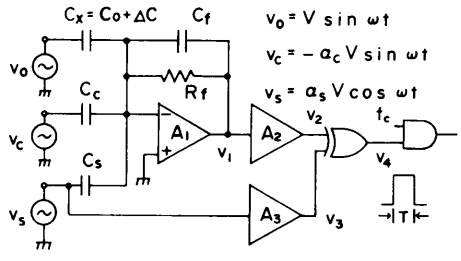

Fig. 1 The circuit diagram of the charge amplifier based interface.

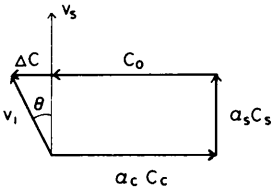

Fig. 2 The phasor representation of the output voltage of the charge amplifier.

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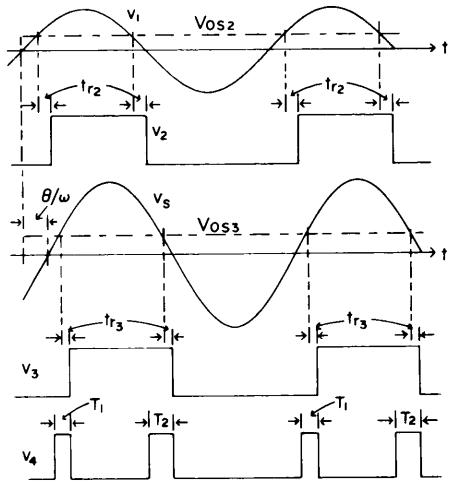

Fig. 3 The erroneous phase-to-pulse width conversion due to the offset voltages and the response time of comparators.

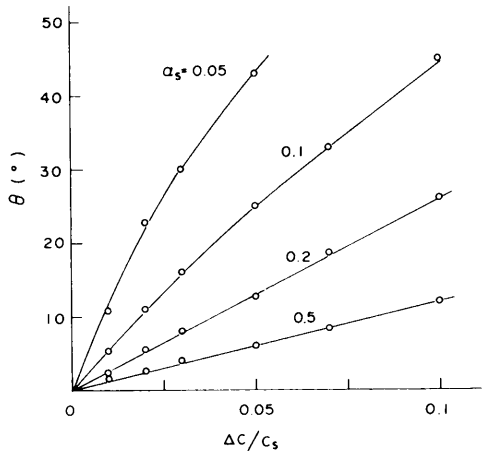

Fig. 4 The phase θ versus the relative capacitance change obtained by a prototype interface.

during T.

Detailed error analysis has shown that parasitic capacitances and nonideal op-amp parameters have no effect upon the interface operation. The offset voltages, V_{os2} and V_{os3}, and the response time, t_{r2} and t_{r3} of the comparators A_2 and A_3, respectively, are possible error sources in the phase-to-pulse width conversion. Their effects are illustrated in Fig. 3. Referring to Fig. 3, one can obtain the following expressions for the output pulse width;

$$T_1=\frac{\theta}{\omega}+\frac{V_{os3}}{\alpha_s V\omega}+t_{r3}-\frac{V_{os2}}{V_1\omega}-t_{r2}, \quad (3)$$

$$T_2=\frac{\theta}{\omega}-\frac{V_{os3}}{\alpha_s V\omega}+t_{r3}+\frac{V_{os2}}{V_1\omega}-t_{r2}, \quad (4)$$

where V_1 is the amplitude of v_1. It is clear from Eqs. (4) and (5) that the effect of the offset voltages can be eliminated by averaging T_1 and T_2. Therefore, the difference in the response time, $\Delta t_r=t_{r2}-t_{r3}$, is only the error source in this interface. Assuming Δt_r less than 20 ns, and the clock frequency f_c of the order of a few tens of MHz, the error due to Δt_r is estimated to be 1 count at most.

3. Experimental Results

The circuit shown in Fig. 1 was breadboarded to confirm its principles of operation. The op-amp and comparators used were LF347 and LM306, respectively. A variable capacitor in parallel with a 10,310 pF capacitor was used for a capacitive sensor. Ceramic capacitors of 10,810 pF and 1,051 pF were used for C_c and C_s, respectively. These capacitors were driven by the 10 kHz quadrature oscillator built using op-amps. The clock frequency f_c used for sensing the pulse width was 10 MHz. No special attention was paid to the response time of the comparator. The experimental results thus obtained are plotted in Fig. 4 with α_s as a parameter. The results are in good agreement with the theoretical values calculated by Eq. (2), showing that the capacitance change smaller than 0.1% can be detected accurately and that the linearity over the wide dynamic range is possible by compromising with the sensitivity.

4. Conclusions

An interface circuit was presented which allows the accurate detection of the capacitance change of a capacitive sensor with a minimum number of components. No trimming of components is required because the cancellation of the offset capacitance of the sensor and the sensitivity adjustment can be made independently by means of the amplitude of sinusoidal sources. The effect of parasitic elements accompanied with the monolithic implementation is also minimum. Therefore, the circuit presented herein is believed to be best suited for the on-chip interface. Its application to practical capacitive sensors is now under way.

References

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