Resonant tunneling characteristics in SiO$_2$/Si double-barrier structures in a wide range of applied voltage

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We have found that current–voltage characteristics of resonant tunneling diodes (RTDs) with a structure of Al/upper-SiO$_2$/p^--Si-well/lower-SiO$_2$/n^+-Si substrate are distinctly categorized by the kinetic energy of electrons in the Si well injected from the n^+-Si substrate. For RTDs with a lower-SiO$_2$-layer thickness below 4 nm, negative differential conductance is observed in accordance with our previous work [Y. Ishikawa, T. Ishihara, M. Iwasaki, and M. Tabe, Electron. Lett. **37**, 1200 (2001)], where electrons have relatively low kinetic energies below 2.7 eV in the Si well. On the other hand, RTDs with a lower-SiO$_2$ layer thicker than 5 nm have specific characteristics of a large current peak and a large hysteresis at higher kinetic energies above 2.9 eV, indicating that hot electrons are readily stored in the Si well, probably due to enhanced impact ionization scattering. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1603352]

Since the first report of resonant tunneling diodes (RTDs), RTDs have been demonstrated mostly in heteroepitaxial systems such as GaAs/AlGaAs,[1–3] GaAs/AlAs,[4] CaF$_2$/CdF$_2$,[5] CaF$_2$/Si,[6] and SiGe/Si systems.[7,8] In contrast, until recently there had been only a few reports on RTDs of the Si/SiO$_2$ system[9,10] and besides they did not show negative differential conductance (NDC), which is the most prominent feature of resonant tunneling. Most recently, we have fabricated Si/SiO$_2$ RTDs by a wafer-bonding method and observed clear NDC, in the Si/SiO$_2$ system.[11] In the present letter, we further investigated $I-V$ characteristics for RTDs with varied thicknesses of the lower oxide in a wide range of applied voltage. As a result, we have found that the diode characteristics strongly depend on the kinetic energies of injected electrons in the Si well.

In this work, we fabricated RTDs with a structure of Al/upper-SiO$_2$-barrier/p^--Si-well/lower-SiO$_2$-barrier/n^+-Si substrate in the same way as in Ref. 11, which is briefly described later. First, Si-on-insulator wafers with an ultrathin (3–7 nm) buried oxide (BOX) layer were prepared. Then, the SiO$_2$/Si double barrier structure was fabricated by thinning of the top Si layer and oxidation for the formation of an upper tunneling barrier (2-nm-thick SiO$_2$). The resultant Si well was about 2 nm in thickness. The Al-electrode area was about 150 μm^2 and the measurement temperature was 15 K. In the $I-V$ measurement, positive voltages were applied to the top Al electrode so that electrons flow from the n^+-Si substrate to the top Al electrode.

Figure 1 shows a typical $I-V$ curve which is observed in RTDs with a BOX thickness below 4 nm. The applied voltage range in Fig. 1 corresponds to injected-electron kinetic energies in the Si well of 2.7 eV or less. The broken lines in the figure indicate the calculated resonance voltages, assuming the longitudinal and transverse effective masses for electrons as $m_l^* = 0.98 m_0$ and $m_t^* = 0.19 m_0$ (m_0: electron rest mass), the Si/SiO$_2$ barrier height $\phi_B = 2.9$ eV,[12] and the Si

well width, only one fitting parameter, $t_{Si} = 2.4$ nm. The NDC peak and inflections are in good agreement with the theoretical resonance voltages. Hence, electrical characteristics of RTDs with a BOX layer thickness below 4 nm are dominated by the ordinary resonant tunneling mechanism, where the kinetic energy of injected electrons in the Si well is relatively low (<2.7 eV) in comparison with the Si/SiO$_2$ barrier height (2.9 eV).

Diode properties for RTDs with a BOX layer of 5 and 7 nm in thickness are shown in Figs. 2(a) and 2(b). The measurement duration time in these figures is defined by the sum of holding and sampling time of a current at each voltage step ($\Delta V = 10$ mV). Some specific characteristics, which are greatly different from Fig. 1, are observed: (i) a large current peak in upward voltage ramping with the duration-time-dependent peak height, (ii) large hysteresis, and (iii) an opposite (negative) current in downward ramping. As for hysteresis in RTDs, a parasitic series resistance causes a hysteresis, as previously reported in AlAs/GaAs RTDs,[4] but this kind of hysteresis is independent of ramping rate (or duration time). Another origin of a hysteresis is reported in CaF$_2$/Si RTDs,[6] i.e., electron storage effect in the Si well is
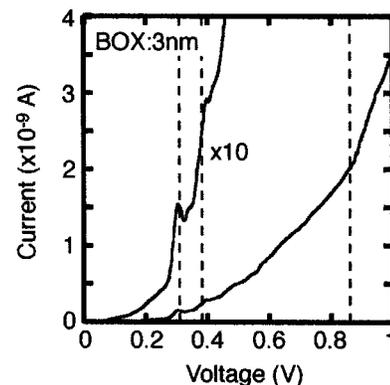

FIG. 1. $I-V$ characteristics of a RTD with a BOX thickness of 3 nm, measured at 15 K. Broken lines indicate the voltages calculated from discrete energy levels for a Si-well model with finite barrier potentials.

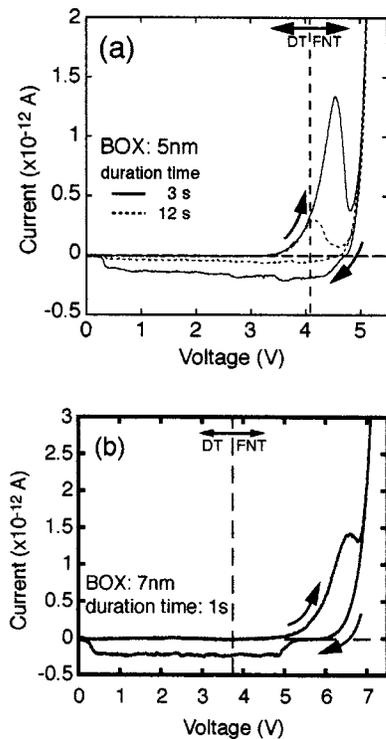[a]Electronic mail: ikeda@rie.shizuoka.ac.jp

FIG. 2. Diode properties (a) for a sample with a 5 nm BOX layer for a measurement duration time of 3 and 12 s and (b) for a 7 nm BOX layer for a duration time of 1 s, at 15 K. Arrows indicate the voltage ramping directions.

FIG. 3. Calculated tunnel current of a SiO_2/Si/SiO_2 diode with a BOX thickness of 5 nm, taking account of the reduction in the BOX layer voltage drop due to the electron storage. In the calculation, it is assumed that the effective mass $m^* = 0.5m_0$, the band offset $\phi_B = 2.9$ eV (see Ref. 12), and the electrode area $A = 150$ μm^2.

responsible for the hysteresis. The latter may be partly effective in explanation of our work. However, both reports deal with the direct tunneling mode, while it should be noted that our results in Fig. 2 were obtained in the Fowler–Nordheim (F–N) tunneling mode involving high-kinetic energies of electrons in the Si well.

The specific characteristics for thick-BOX diodes shown in Fig. 2 can be explained by the electron storage due to the hot electron injection in the Si well. Under the F–N tunneling condition, the injected electrons in the Si well have relatively high kinetic energies above 2.9 eV. The injected electrons with high kinetic energies easily experience impact ionization scattering and lose their energies, as described later. Once the injected electrons are rapidly stored during upward ramping, the Si-well potential will also be rapidly raised and the voltage-drop across the BOX layer (emitter-side barrier) will be reduced. This leads to the reduction in the tunneling current in upward voltage ramping. Figure 3 is a calculated $I–V$ curve of a 5 nm BOX diode for a ramping rate (duration time) of 3 s, taking into account the electron storage effect reflecting impact ionization scattering, under the assumption that the stored electrons are fixed in the well (not released). The hysteresis in downward voltage ramping is also reproduced in Fig. 3. From this agreement between Figs. 2 and 3, it is convincing that the result in Fig. 2 is due to electron storage. However, there is a slight difference between these figures, that is, the opposite (negative) current in downward voltage ramping cannot be reproduced in the calculated curve. Since the opposite current is inversely proportional to the duration time in the whole voltage range as shown in Fig. 2(a), we believe that the opposite current is primarily a transient current which should have been influ-
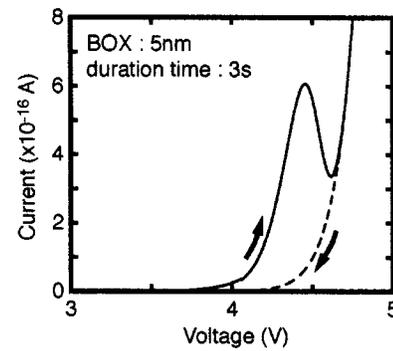
enced by parasitic capacitance and resistance, but further study is necessary.

As the scattering process, electron–electron, electron-phonon, and electron-impurity collisions may be possible, but impact ionization scattering[13–16] should be the most relevant scattering process, as is usually considered in hot electron issues in metal–oxide–semiconductor field effect transistors,[14–16] because the injected electrons must efficiently lose their kinetic energy as large as ~3 eV during the short transit time (subpicoseconds) in the Si well. The electron storage rate caused by the impact ionization scattering can be proportional to the product of the injected electron flux (cm^{-2} s^{-1}), the ionization rate (s^{-1}), and the transit time in the Si well t_{well} (s). Figure 4 shows the ionization rate of an electron in Si after Ref. 13 and the calculated tunneling current through a single barrier of the 5-nm-thick SiO_2 film, as a function of applied voltage to a RTD. The tunneling current is calculated using the direct and F–N tunneling equations, assuming the effective mass $m^* = 0.5m_0$ and the band offset $\phi_B = 2.9$ eV.[12] Both ionization rate and tunneling current increase exponentially with increasing the applied voltage,[13–16] while t_{well} is inversely proportional to square root of the voltage across the BOX layer. Thus, the electron storage rate should exponentially increase with increasing voltage, and hence, the electron storage in the well becomes prominent only at high voltages.

We have investigated the $I–V$ characteristics of RTDs with a Si/SiO_2 double barrier. It is found that the diode char-
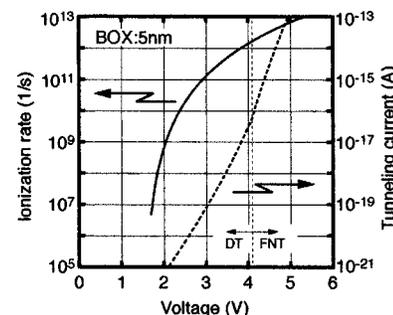

FIG. 4. Impact ionization rate of an electron in Si after Ref. 13 and the tunneling current through a 5-nm-thick SiO_2 film, as a function of applied voltage to the RTD. The tunneling current is calculated using the direct and F–N tunneling equations, assuming the effective mass $m^* = 0.5m_0$, the band offset $\phi_B = 2.9$ eV (see Ref. 12) and the electrode area $A = 150$ μm^2.

acteristics are strongly dependent on the kinetic energy of injected electrons in the Si well. In high-energy electrons as in the F–N tunneling mode, the electron storage in the Si well occurs due to the impact ionization scattering of injected electrons.

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