Single-electron tunneling in a silicon-on-insulator layer embedding an artificial dislocation network

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A two-dimensional dislocation network artificially embedded in a silicon-on-insulator (SOI) layer was examined as the source of lattice strain to generate a periodic potential. A screw dislocation network with the period of 20 nm was formed in an SOI layer using a twist bonding of two SOI wafers. *n*-channel metal-oxide-semiconductor field-effect transistors using the dislocation-embedded SOI layer showed an oscillation of drain current with the gate voltage at the temperatures below 40 K. This oscillation is ascribed to the single-electron tunneling through the spatially modulated potential. The results suggest that the dislocation network works as the strain source to form the potential array. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2176849]

Formation of an alternate structure of potential well and tunnel barrier in a silicon-on-insulator (SOI) layer is the key issue to realize Si-based nanodevices, such as single-electron transistors. From the viewpoint of self-organized formation of a potential array, we have recently reported a two-dimensional network of screw dislocations buried in a thin SOI layer, which is formed using a twist bonding of two SOI wafers.[1] Such an artificial dislocation network is known to be formed at the bonding interface between the bare surfaces of Si (Refs. 2 and 3) as well as other semiconductors, such as GaAs,[4] when the in-plane crystalline direction is slightly misaligned to cause a lattice mismatch.[5,6] It is noted that the period of dislocations can be controlled on the nanometer scale by the twist angle.[2,5,6] In the previous study by Leroy *et al.*,[7,8] the dislocation network, embedded near the bulk Si surface, was used as the template for the ordered growth of Ge quantum dots with the help of the two-dimensionally modulated strain field due to the dislocations. However, as widely used in the III-V and Si/SiGe heteroepitaxial systems, the lattice strain causes the changes in the band edge energies,[10] suggesting that the dislocations can directly work as the periodic stressors to modulate the electronic potential.

In this letter, an artificial dislocation network embedded near the SOI surface was examined as the strain source to generate the periodic potential, as schematically shown in Fig. 1. For the screw dislocation network, a shear strain is accumulated around the dislocations, particularly around the crossing of the dislocation lines.[8,9] Such a shear strain should split six equivalent minima of conduction bands along the ⟨100⟩ directions in Si, and the larger change in the conduction-band minimum is expected at the locations where the larger strain is accumulated.[10] Taking into account the tendency of band gap narrowing for Si under the stress,[10,11] the potential well may be formed around the crossing. The potential profile in the dislocation-embedded SOI layer was investigated using the transport characteristics of metal-oxide-semiconductor field-effect transistors (MOSFETs). As a result, the drain current oscillated with the gate voltage probably due to the single-electron tunneling. This suggests that the spatially modulated potential is induced by the strain due to the dislocation network.

Figure 2 shows the fabrication process of the SOI layer embedding the dislocation network. In order to form the dislocation network in the thin SOI layer, two commercially available SOI (UNIBOND) wafers were directly bonded. The starting SOI wafers had a top *p*-Si (001) layer (10 Ω cm) of 205 nm, a buried SiO_2 (BOX) layer of 400 nm and a thick *p*-Si (001) base substrate (10 Ω cm). Prior to the bonding, the thicknesses of top Si layers were reduced to 20 nm by the thermal oxidation. After removing the grown oxide in a diluted HF solution, the wafers were bonded at room temperature in air, as in the left of Fig. 2. It is noted that the in-plane crystalline direction was intentionally misaligned (twist angle $\psi \sim 1°$) to induce the screw dislocation network at the bonding interface. Then, the sample was annealed in N_2 at 1000 °C for 2 h to stabilize the bonding. Next, as in the center of Fig. 2, the Si substrate and BOX layer (front side) were etched in a KOH solution and a diluted HF solution, respectively.[12] The dislocation network should be formed at the bonding interface in the thin SOI layer, as in the right of Fig. 2. In fact, the plan-view transmission electron microscope (TEM) image of Fig. 3(a) showed a periodic array of screw dislocations in the ⟨110⟩ directions, although the dislocations are not perfectly uniform due to the mixture with the edge dislocations induced by the surface steps before the bonding.[2] The period between the dislocations d_d is ~20 nm on average, being in good

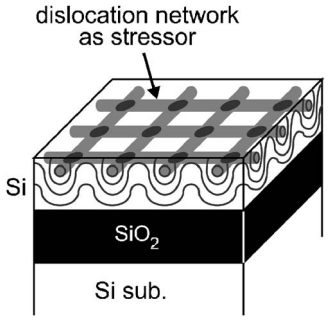

FIG. 1. Schematic illustration of thin SOI layer embedding an artificial dislocation network as the strain source.

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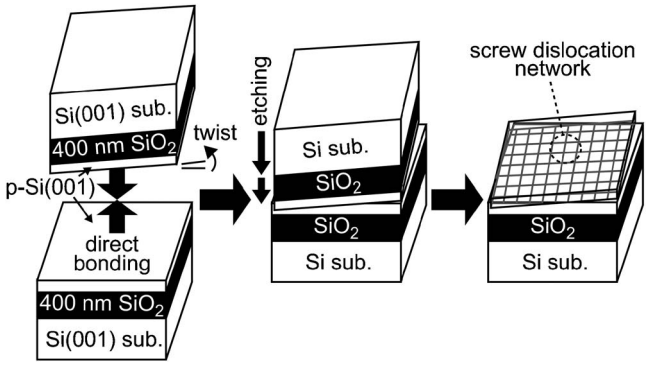

FIG. 2. Fabrication procedure of artificial dislocation network embedded in a thin SOI layer.

agreement with the theoretical value of 22 nm for $\psi=1°$, which is determined by $d_d=|\mathbf{b}|/[2\sin(\psi/2)]$ ($\mathbf{b}=(a/2)\langle 110\rangle$: Burger's vector, a: Lattice constant of Si).[2,6] Additionally, in the cross-sectional image of Fig. 3(b), bright and dark regions are alternately seen in the lower half of the SOI layer, although such a behavior is not clearly seen in the upper half probably due to the structural nonuniformity observed in the plan-view image. These bright and dark regions may reflect the strain distribution in the SOI layer, since the period almost agrees with the dislocation period. Our concept is to use such a strain distribution for the formation of the potential array.

In order to investigate the potential profile, current-voltage (I-V) characteristics were measured for n-channel MOSFETs using the dislocation-embedded SOI layer, whose TEM images were shown in Fig. 3. Figure 4 shows the schematic device structure. Electron-beam lithography was used to pattern the SOI layer into the $\langle 110\rangle$ wire connected to the large source and drain contacts. A selective n-type doping was performed for the source and drain regions with phosphorous diffused from a spin-coated silica film containing P_2O_3. The channel width and length were typically 0.5 μm. The device surface was covered with a thermally grown SiO_2 layer (10 nm) and an Al top gate, which are not indicated in Fig. 4. The final thickness of SOI layer was ~25 nm; the dislocation network was located ~5 nm below the top SiO_2/Si interface and ~20 nm above the bottom interface. Although the top gate was prepared, the Si substrate was used as the backgate in the present experiments. In this case, electrons should preferentially flow below the dislocations. The I-V measurements were carried out at low temperatures (mainly 15 K). As the reference, MOSFETs without the dislocations were also prepared.

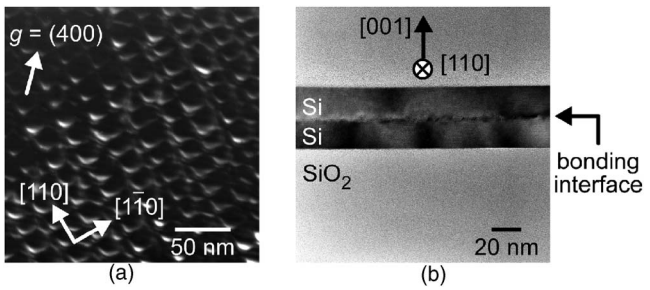

FIG. 3. Typical TEM images for a sample with twist angle ψ of ~1°. (a) Plan-view image [g-2g weak beam image: $g=(400)$] and (b) cross-sectional image.

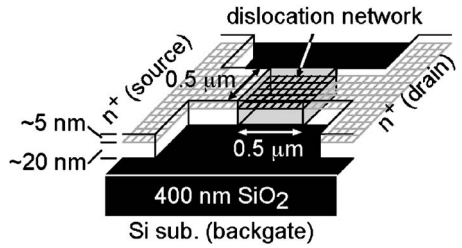

FIG. 4. Schematic structure of fabricated MOSFET.

Typical drain current-gate voltage (I_d-V_g) characteristics at 15 K are shown in Fig. 5(a) for two different MOSFETs with the dislocations as well as the one without the dislocations. A small drain voltage V_d of 5 mV was used. For the MOSFETs with the dislocations, oscillatory, and step-wise current changes are commonly seen near the threshold voltage, as indicated by the arrows, although the peak positions and amplitudes are slightly different between the MOSFETs probably due to the structural nonuniformity seen in the TEM image. Such an oscillatory behavior can be observed up to ~40 K, as in Fig. 5(b). On the other hand, the oscillations could not be observed for the reference MOSFETs without the dislocations. Thus, the observed oscillations are ascribed to the presence of dislocations.

The oscillations are most likely to be due to the single-electron tunneling (Coulomb blockade oscillation). In order to examine the validity of such an interpretation, the lateral size of Coulomb island d_c was estimated from the observed spacing between the current oscillations, ΔV_g (e.g., in Fig. 5), and compared with the dislocation period d_d. Assuming the circular island, d_c is roughly determined using ΔV_g by $d_c=\sqrt{4et_{ox}/\pi\varepsilon_{ox}\Delta V_g}$, where t_{ox} is the thickness of buried

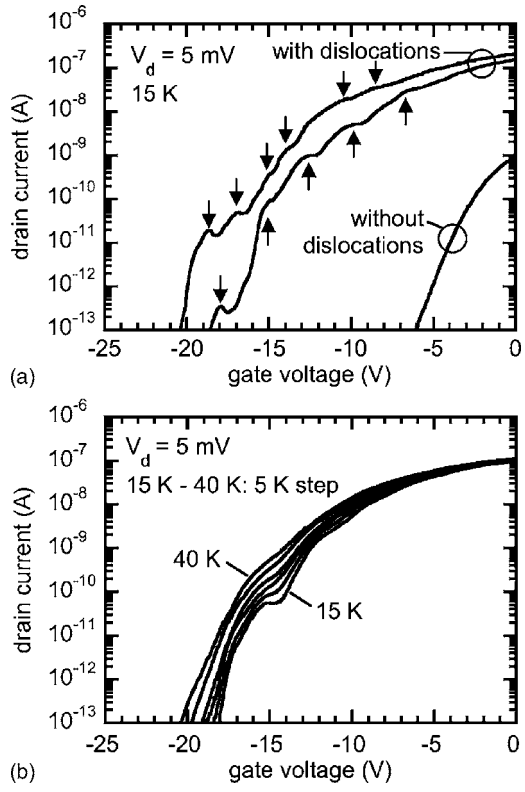

FIG. 5. (a) I_d-V_g curves at 15 K for two different MOSFETs with dislocations and a MOSFET without dislocations and (b) typical temperature dependence of I_d-V_g property.

SiO_2 layer (400 nm) and ε_{ox} is the permittivity of SiO_2 ($3.9\varepsilon_0$). Substituting a typical ΔV_g value of 3 V, d_c is obtained to be 28 nm. This value is in good agreement with the dislocation period d_d of ~20 nm by TEM, supporting that the single-electron tunneling occurs due to the potential modulation induced by the dislocations. The multiple tunnel junctions should be formed when the dislocation network is responsible for the potential modulation. The nonuniform voltage spacings between the current oscillations, seen in Fig. 5(a) particularly for one of the samples showing the higher current level, is probably ascribed to the formation of multiple tunnel junctions. The lower measurement temperatures would be required for the present devices to clearly observe the multiple-junction behaviors such as the peak splitting and the nonuniform peak amplitude.[13]

The vertical size of Coulomb island is also estimated. As in Fig. 5(b), the maximum temperature to observe the oscillations T_{max} is ~40 K. Assuming that one of the Coulomb islands in the multiple tunnel junctions survives from the temperature increase, i.e., one Coulomb island dominates the characteristics at the raised temperature, the charging energy E_c of the island is estimated to be $E_c \sim k_B T_{max} = 3.4$ meV. This leads to the total capacitance $C_\Sigma (= e^2/2E_c)$ of 23 aF, indicating that the source and drain capacitances (C_s and C_d) mainly contribute to $C_\Sigma (= C_g + C_s + C_d)$, because the gate capacitance $C_g = e/\Delta V_g$ is only ~0.05 aF. In order to explain C_s and C_d of ~10 aF, the height of Coulomb island as large as 10 nm is necessary, taking into account that the width of tunnel barrier is as large as the dislocation period d_d of ~20 nm or below. The obtained height of Coulomb island is comparable to the SOI thickness used in this study, and therefore, the dislocation-induced potential modulation extends almost throughout the thin SOI layer in the vertical direction.

As mentioned already, for the screw dislocation network, a shear strain is accumulated around the dislocations, particularly around the crossing of the dislocation lines.[8,9] Such a shear strain should cause the change in the energy of conduction-band minimum,[10] and it is most likely that this leads to the formation of the Coulomb islands underneath the crossing points. The strain field due to the edge dislocations, which are induced by the surface steps and lead to the degradation of structural uniformity, might also influence the potential modulation. The additional effect of Coulomb potential due to the charged defects may be superimposed, which is partly seen in Fig. 5(a) as the negative shift in the threshold voltage (~15 V, corresponding to the positive charge density of $\sim 1 \times 10^{12}$ cm^{-2} at the bonding interface). Further studies are necessary to clarify these points.

In summary, an artificial dislocation network embedded near the SOI surface was examined as the strain source to generate the periodic potential. The drain current oscillated with the gate voltage probably due to the single-electron tunneling, resulting from the formation of spatially modulated potential. This result suggests that the dislocation network works as the strain source to form the potential array.

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[1] Y. Ishikawa, K. Yamauchi, C. Yamamoto, and M. Tabe, Mater. Res. Soc. Symp. Proc. **864**, E6.5.1 (2005).
[2] K. Rousseau, J. L. Rouviere, F. Fournel, and H. Moriceau, Appl. Phys. Lett. **80**, 4121 (2002), and references therein.
[3] R. A. Wind, M. J. Murtagh, F. Mei, Y. Wang, M. A. Hines, and S. L. Sass, Appl. Phys. Lett. **78**, 2205 (2001).
[4] F. E. Ejeckam, Y. H. Lo, S. Subramanian, H. Q. Hou, and B. E. Hammons, Appl. Phys. Lett. **70**, 1685 (1997).
[5] D. Hull and D. J. Bacon, *Introduction to Dislocations*, 4th ed. (Butterworth–Heinemann, Oxford, UK, 2001), Chap. 9.
[6] J. P. Hirth and J. Lothe, *Theory of Dislocations*, 2nd ed. (Wiley, New York, 1982), Chap. 19.
[7] F. Leroy, J. Eymery, P. Gentile, and F. Fournel, Appl. Phys. Lett. **80**, 3078 (2002).
[8] F. Leroy, J. Eymery, P. Gentile, and F. Fournel, Surf. Sci. **545**, 211 (2003).
[9] A. Bourret, Surf. Sci. **432**, 37 (1999).
[10] C. G. Van de Walle, Phys. Rev. B **39**, 1871 (1989).
[11] K. Shiraishi, M. Nagase, S. Horiguchi, H. Kageshima, M. Uematsu, Y. Takahashi, and K. Murase, Physica E (Amsterdam) **7**, 337 (2000).
[12] Y. Ishikawa, S. Makita, J. Zhang, T. Tsuchiya, and M. Tabe, Jpn. J. Appl. Phys., Part 2 **38**, L789 (1999).
[13] See, for example, F. R. Waugh, M. J. Berry, C. H. Crouch, C. Livermore, D. J. Mar, R. M. Westervelt, K. L. Campman, and A. C. Gossard, Phys. Rev. B **53**, 1413 (1996).