Foreword

THIS Special Issue of IEEE TRANSACTIONS ON NANOTECHNOLOGY is devoted to papers from the 2003 Silicon Nanoelectronics Workshop, the eighth workshop in the series, which was held on June 8–9, 2003, at the Rihga Royal Hotel, Kyoto, Japan.

The workshop shed light on all aspects of silicon-based nanoelectronics, including MOSFET scaling and ballistic transport effects, novel structures for Si FETs, nanoscale memories, quantum and single-electron effects in Si devices, novel circuit architectures in nanodevices, and nano-heterostructure devices. This workshop was the largest so far, with 145 in attendance from all over the world. There were five invited talks, which covered a wide area from advanced FETs to Si quantum computers, 20 contributed talks, and 30 poster presentations. There was also the Rump Session, "Prospect of the future (2020) silicon nanodevices," moderated by Asen Asenov, from the University of Glasgow, Glasgow, U.K., Yukinori Ono, from Nippon Telegraph and Telephone (NTT) Corporation Laboratories, Atsugi, Japan, and Ken Uchida, from Toshiba, Research and Development Center, Kawasaki-shi, Japan.

We would like to thank the Technical Program Committee Members, Asen Asenov, from the University of Glasgow; Simon Deleonibus, from LETI Genoble, France; Kristin De Meyer (IMEC), David K. Ferry, from Arizona State University, Tempe, David J. Frank, from IBM; Yorktown Heights, NY, Hiroya Ikeda, from Shizuoka University, Hamamatsu, Japan; Seiichi Miyazaki, from Hiroshima University, Hiroshima, Japan; Hiroshi Mizuta, from Hitachi Cambridge, Research Laboratory, Cambridge, U.K.; Shunri Oda, from the Tokyo Institute of Technology, Meguro-ku, Tokyo, Japan; Yukinori Ono, from NTT; Byung-G. Park, from Seoul National University, Kwanak-gu, Seoul; Wolfgang Porod, from Notre Dame University, Notre Dame, IN; Nobuyuki Sano, from Tsukuba University, Ibaraki, Japan; Hyungcheol Shin from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea; Thomas Skotnicki, from STMicroelectronics; Crolle, France; Eiichi Suzuki, from AIST, Japan; Sandip Tiwari, from Cornell University, Ithaca, NY; Akira Toriumi, from the University of Tokyo, Toyko, Japan; Ken Uchida, with Toshiba, Research and Development, Kawasaki-shi; Tatsuya Usuki, from Fujitsu Labs, Atsugi, Japan; Hitoshi Wakabayashi, from NEC, Kanagawa, Japan; and Bin Yu from AMD, Sunnyvale, CA, for their effort in making the workshop an attractive and successful event. We would also like to thank the many reviewers who ensured the quality of this Special Issue. Finally, we would like to thank the Japan Society of Applied Physics for its support of the workshop. The next Silicon Nanoelectronics Workshop will be held in Hawaii, on June 13–14, 2004.

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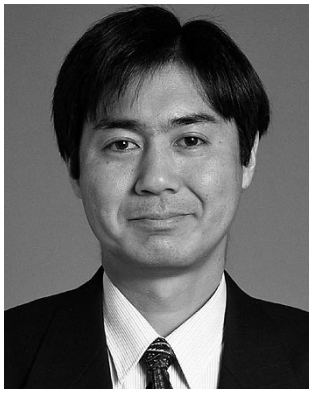

Toshiro Hiramoto received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Japan, in 1984, 1986, and 1989, respectively.

In 1989, he joined the Device Development Center, Hitachi Ltd., Ome, Japan, where he was engaged in the device and circuit design of ultra-fast BiCMOS SRAMs. In 1994, he joined the Institute of Industrial Science, University of Tokyo, as an Associate Professor. He was also an Associate Professor with the VLSI Design and Education Center, University of Tokyo, from 1996 to 2002. He has been a Professor with the Institute of Industrial Science, University of Tokyo, since 2002. His research interests include low-power, low-voltage design of advanced CMOS devices, SOI MOSFETs, device/circuit cooperation scheme for low-power VLSI, quantum effects in nano-scale MOSFETs, and silicon single electron transistors.

Dr. Hiramoto is a Member of IEICE and the Japan Society of Applied Physics. Since 2001, he has been an Elected AdCom Member of IEEE Electron Devices Society. He served as the General Chair of Silicon Nanoelectronics Workshop in 2003, and the Program Chair in 1997, 1999, and 2001. He also served on the Program Subcommittee on Integrated Circuits of IEEE International Electron Devices Meeting (IEDM) in 1993 and 1994, and on the Program Subcommittee on CMOS Devices of IEDM in 2003, and has served on Program Committee of Symposium on VLSI Technology since 2001.

Michiharu Tabe received the B.S., M.S. and Dr. Eng. degrees from Keio University, Keio, Japan, in 1973, 1975, and 1984, respectively.

From 1975 to 1994, he was with Nippon Telegraph and Telephone (NTT) Corporation Laboratories, Atsugi, Japan, where he was involved in the research of surface-related Si processes for advanced MOS and bipolar transistors, and also in Si nanodevices such as single-electron devices. From 1984 to 1985, while on leave from NTT, he was a Visiting Researcher with Stanford University, Palo Alto, CA, where he worked on Synchrotron Radiation for the characterization of ultra-thin gate oxides. In 1994, he joined the Research Institute of Electronics, Shizuoka University, Japan, as a Professor. He is currently engaged in Si single-electron devices, Si resonant tunneling devices, self-organization phenomena and their application to photonic devices.