Ambipolar Coulomb Blockade Characteristics in a Two-Dimensional Si Multidot Device

Ratno Nuryadi, Hiroya Ikeda, Yasuhiko Ishikawa, and Michiharu Tabe

***Abstract*—A two-dimensional Si multidot channel field-effect transistor is fabricated from a silicon-on-insulator material and the electrical characteristics are studied. The multidots are formed using a nanometer-scale local oxidation of Si process developed in our laboratory. The device shows ambipolar characteristics because of Schottky source and drain, i.e., the carriers are electrons for positive gate voltage and holes for the negative one. It is shown that Coulomb blockade (CB) oscillations are clearly observed for both of the electrons and holes at measurement temperatures up to 60 K. Both CB characteristics show nonperiodic oscillation and an open Coulomb diamond. These features are ascribed to the single electron/hole tunneling in the Si multidot channel.**

***Index Terms*—Ambipolar Coulomb blockade, Schottky contact, Si multidot, single electron tunneling, single hole tunneling.**

I. Introduction

SINGLE-ELECTRON/HOLE Tunneling (SET/SHT) devices have attracted much attention as a candidate for future nanodevices in terms of ultra-high density integration and low-power consumption. The SET/SHT devices have been fabricated using various material systems such as Si/SiO_2 [1]–[3], GaAs [4], [5] and carbon nanotube [6], [7] systems. Particularly, Si-based-SET devices have been demonstrated to operate at or near room temperature [1]–[3]. In applying Si SET devices to new functional devices such as quantum cellular automata (QCA) [8], [9] and photoimaging devices [10], it is necessary to develop the SET/SHT devices composed of a two-dimensional (2-D) array of Si dots. So far, most of the Si-based SET devices utilize single dot or one-dimensional (1-D) dot array [1], [11], [12], while only one paper has been reported [13] on the transport properties in the 2-D Si dots, to our knowledge. In [13], 2-D multidots composed of an undulated ultrathin silicon-on-insulator layer were formed using anisotropic wet etching in an alkaline-based solution. Such a method using wet chemical etching is simple, but difficult to precisely control the structure.

In this article, we present a new fabrication method of Si SET devices with a 2-D multidot channel and study their electrical characteristics. The multidots are formed using a nanometer-scale local oxidation of Si (nano-LOCOS) process developed by the authors [14]. The nano-LOCOS process is effective to control the size of Si dots. It will be shown that Coulomb blockade (CB) oscillations for electrons and holes are clearly observed in the same device. In CB characteristics, spacing between current peaks in the CB oscillations is not constant and current contour plots for the drain voltage and gate voltage plane show an open Coulomb diamond. These features are ascribed to SET/SHT through the Si multidot structure.

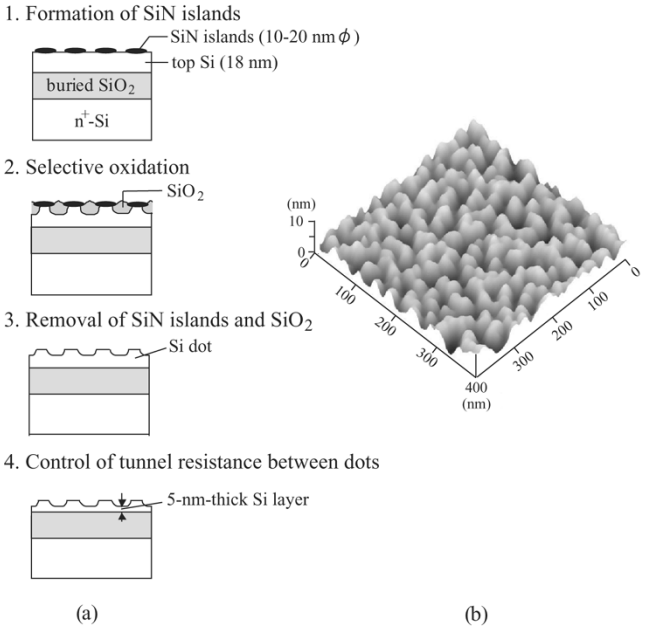

Fig. 1. (a) Fabrication steps of Si multidots. (b) AFM image of the fabricated dots.

II. Device Fabrication

As the starting substrate, a silicon-on-insulator (SOI) wafer composed of a 150-nm-thick lightly doped p-type top Si layer, a 90-nm-thick buried SiO_2 layer and an n^+-type Si substrate, was used. This SOI substrate was fabricated in our laboratory by a wafer-bonding technique [15]. In this work, we use heavily-doped base Si substrates as a backgate (see Fig. 2), because a voltage drop can be neglected.

In the first step of fabrication, the thickness of the top Si layer of the SOI wafer was reduced to about 18 nm by repetitive cycles of thermal oxidation and subsequent chemical etching of the SiO_2. The top Si thickness of 18 nm is thick enough to prevent the agglomeration of the Si layer [16], [17] during high temperature cleaning used in the nano-LOCOS process, as described below.

Fig. 1(a) shows a schematic process flow of the fabrication procedure of Si multidots by the nano-LOCOS process. The process consists of four steps, i.e.: 1) formation of ultrasmall

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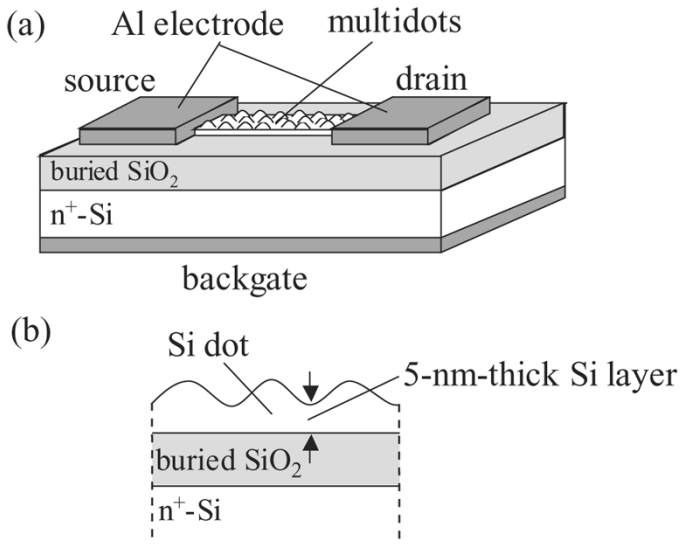

Fig. 2. Schematic view of Si SET device. (b) Cross-sectional view of the Si channel.

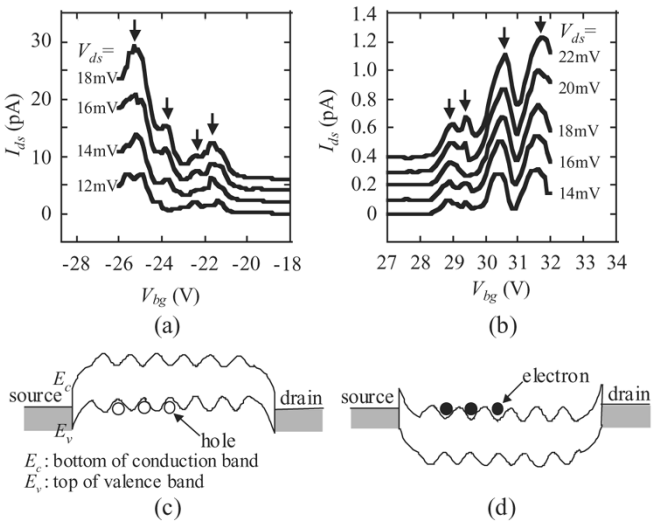

Fig. 3. Drain-source current (I_{ds}) versus backgate voltage (V_{bg}) of the (a) SHD and (b) SED characteristics at 15 K. The curves are shifted vertically by (a) 2 pA and (b) 0.1 pA, respectively, for clarity.

SiN islands; 2) selective oxidation with SiN masks; 3) removal of SiN islands and SiO_2; and 4) control of tunnel resistance between dots. Details of the process are as follows. Prior to loading into an ultra-high vacuum (UHV) chamber, the SOI substrate is chemically cleaned in a H_2SO_4/H_2O_2 mixture and then rinsed in a deionized water. After high-temperature cleaning (about 930 °C) in UHV for removing the surface oxide, ultrasmall SiN islands were naturally formed on the Si surface by supplying N_2 gas (partial pressure of 1×10^{-5} torr) for 100 s at the substrate temperature of 750 °C. Here, as pointed out by Janzen and Monch [18], nitrogen radicals automatically excited by a nude ionization gauge, are responsible for the SiN formation. In this condition, the SiN islands with a lateral size of 10–20 nm, a thickness of only 0.5 nm, and a density of about 3×10^{11} cm^{-2}, are formed [19], [20].

Next, the surface was selectively oxidized with the SiN masks by a conventional furnace oxidation. It is noted that the SiN islands work as oxidation masks despite their thickness of only 0.5 nm [19], [20]. The oxidation was carried out at 800 °C (1 atm dry O_2) for 150 min, immediately after the nitrided sample was removed from the UHV chamber. Since this oxidation produces a 12-nm-thick SiO_2 layer on the Si surface, Si multidots with a height of about 18 nm are formed, which are connected with the 13-nm-thick Si layer. (It is noted that the height of the dot is measured from Si/buried SiO_2 interface.) Then, the sample was dipped in an H_2SO_4/H_2O_2 mixture and subsequently in a diluted HF solution. By this treatment, the SiN masks as well as SiO_2 were removed. Next, the thickness of the Si layer connecting the dots was reduced to be about 5 nm by further oxidizing the whole surface. Simultaneously, the height of the dots are reduced to be about 9 nm. Here, the ultrathin Si layer connecting the Si dots plays an essential role in this device because it works as a tunnel barrier (or tunnel resistance) between the dots.

Fig. 1(b) shows a typical atomic force microscope (AFM) image taken for the multidots. From the AFM image, the lateral size, height and density of the Si dots are about 20 nm, 4 nm and 2×10^{11} cm^{-2}, respectively. The values of the lateral size and the density of the dots are in good agreement with those of SiN islands. The observed dots height of 4 nm is also in good agreement with the expected height of the dots measured from the surface of the connecting Si layer (about 5 nm).

Then, the Si layer with multidots was patterned by a conventional electron beam lithography and a selective etching with a KOH solution to form a Si channel. Finally, Al electrodes were deposited as Schottky source and drain. Fig. 2(a) and (b) show the schematic view of the final structure and the cross-sectional view of the channel. The base n^+-Si substrate works as the backgate and no top gate is prepared. The channel width and the distance between source and drain are about 0.3 and 0.8 μm, respectively. As mentioned above, the Si layer connecting the Si dots is important for the tunneling transport. Comparing the lowest energy level of the 5-nm-thick Si layer and the 9-nm dot height resulted from the quantum confinement effects, the tunnel barrier heights are estimated to be 50 meV for holes and 20 meV for electrons, respectively. (Details will be shown later.)

The other important feature of this device is that ambipolar characteristics are expected due to the Schottky source and drain. For positive backgate voltage (V_{bg}), electrons are induced in the channel and the device acts as a single-electron device (SED). On the other hand, for negative V_{bg}, holes are induced and the device acts as a single-hole device (SHD).

III. Device Characteristics

Fig. 3 shows the drain-source current (I_{ds}) versus V_{bg} characteristics for (a) SHD and (b) SED conditions at 15 K as a parameter of drain-source voltage (V_{ds}). The current oscillations due to CB phenomena are clearly observed for both conditions. This result means that the device has an ambipolar property and that the tunnel barriers are certainly formed in both of the conduction and valence bands of the channel, as schematically shown in Fig. 3(c) and (d). Such an ambipolar and CB characteristics has been reported in FETs with a carbon nanotube as a channel [6], [7]. In the Si/SiO_2 system, ambipolar CB characteristics have

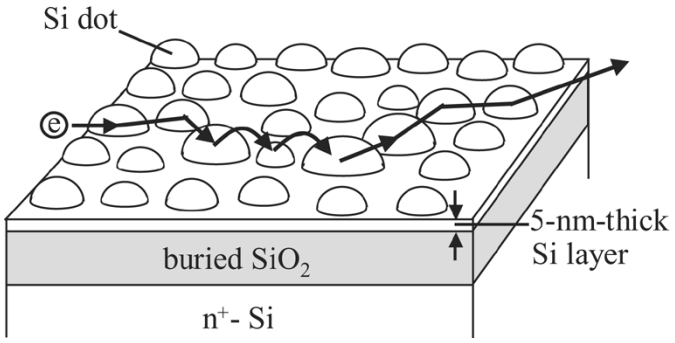

Fig. 4. Single-hole (electron) percolation path.

been observed for a point contact channel FET which has the n^+-Si source/drain contacts for electrons separately from p^+-Si source/drain for holes [21]. In the present experiment, on the other hand, we observe ambipolar CB characteristics for FET with the 2-D Si multidot channel connected to source/drain contacts common to electrons and holes, for the first time.

In an ordinary single-electron transistor that consists of a Coulomb island connected to two ultrasmall tunnel junctions and a gate capacitor (C_g), the current-voltage (*I–V*) characteristics are periodic with the gate voltage (V_g). The period δV_g is equal to e/C_g, where e is the electron charge. However, the spacing between the current peaks in Fig. 3 is not constant. This strongly suggests that several single electron (hole) transistors with different C_g are working in the channel. Actually, the dot size and the interspacing are not uniform, as seen in Fig. 1(b). In such a case, the dot capacitance as well as the tunnel resistance between the dots are different each other. Therefore, we believe that an electron (hole) percolation path, which has the largest total conductance, is formed in the channel and then a few tunnel junctions with highest resistance in the path dominate the carrier transport, as shown in Fig. 4. The number of such effective percolation paths is expected to be small, because current peaks in *I–V* characteristics would disappear due to averaging effect by the peak superimposition if many parallel percolation paths are present.

Here, we focus on the current-peak intensity in the CB characteristics. It seems that irregularity in the current-peak intensity is noticeable for the SHD condition. That is, with negatively increasing the V_{bg}, the peak intensity does not increase successively, in contrast with the SED condition. This fact is guessed to reflect difference in the number of dots contributing to the *I–V* characteristics, which originates from the tunnel barrier heights for holes and electrons, concerning the same dot. Based on the quantum confinement effects, the energy level in the Si layer is inversely proportional to the effective mass (m^*) and t_{Si}^2, where t_{Si}^2 is the thickness of the Si film. The tunnel barrier height results from the difference of the lowest energy levels at the top of dot and the valley between dots. Although both holes and electrons have two effective masses, the minimum energy level is mainly determined by the larger effective mass. Therefore, we use the heavy hole effective mass $m_{hh}^* = 0.49\, m_o$ and longitudinal electron effective mass $m_{le}^* = 0.98\, m_o$ (m_o is electron rest mass) for estimation. As a result, the barrier height for holes (50 meV) is 2.5 times higher than that for electrons (20 meV),

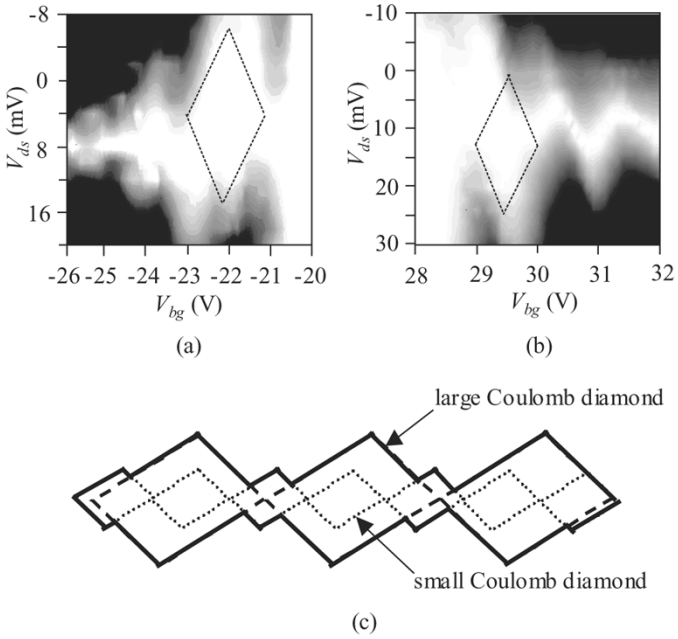

Fig. 5. Contour plot of the $|I_{ds}|$ versus V_{bg} and drain-source voltage (V_{ds}) for (a) SHD and (b) SED conditions. (c) Coulomb diamond diagram of two single-hole (electron) transistors connected in series.

and it can be expected that the number of barriers effectively working as a junction for holes is larger than that for electrons. This may be the origin why the regularity in the current-peak intensity is different between SHD and SED conditions.

It is also seen in Fig. 3, that the current level observed for the SHD condition is two orders of magnitude larger than that for the SED condition. This fact is not ascribed to the difference of the tunneling resistance between holes and electrons, because the tunnel barrier height for holes is larger than that for electrons as mentioned earlier. Therefore, the number of carriers injected at the source contact or emitted to drain contact is guessed to determine the current level. At the measurement of 15 K, thermionic emission of carriers beyond the Schottky barriers is negligible. In stead, tunneling of carriers from/to Al electrodes through the Schottky barrier would dominate the current flow. In such a case, the difference of the Schottky barrier height (SBH) between electrons and holes causes the difference of the current level, i.e., if the SHB for electrons is larger than holes, electron current is smaller. We have not yet measured barrier height directly, but the typical SHB seems to be 0.58 eV for holes and 0.72 eV for electrons at 300 K in Al/Si contacts [22].

Fig. 5(a) and (b) show the contour plots of the $|I_{ds}|$ in the $V_{ds} - V_{bg}$ plane for SHD and SED conditions, respectively. For both conditions, rhombus-shaped structures are seen, which is the direct evidence of the CB effect. However, various sizes and shapes of the rhombus structures are present. Furthermore, they are not completely closed at current peak positions for very low-drain voltages. Theoretically, such open and deformed Coulomb diamonds are ascribed to serially connected single-hole (electron) transistors having different values of dot capacitance [23], as schematically shown in Fig. 5(c). Such Coulomb diamonds were experimentally observed for multiple tunnel junctions in Si/SiO_2 [2], [24] and GaAs [25] systems. The other mechanism

to explain the open Coulomb diamonds is the effect of the resistive environmental impedance, as reported by Ingold *et al.* [26] and Wakaya *et al.* [27], since our FET has large resistances at the Schottky source and drain. This resistance may be another reason for the open diamonds, although serially connected FETs with different dot capacitances are necessary to explain the various sizes and shapes of the diamonds.

It should be noted that the Coulomb diamonds are shifted toward to the positive V_{ds} direction by about 8 mV. The origin of this offset has not been clarified yet. The actual voltage applied to the 2-D multidot channel might be different due to the fixed charges related to the effects such as the floating body effect in the SOI-based FET and the interface states. We confirmed that the error of the V_{ds} supplied between source and drain is within 1 mV, but small high-frequency noise in the V_{ds} signal may be the another possible reason. Further investigation is necessary to clarify this point.

In the Si/SiO_2 system, recently, multijunction transistors with a doped Si channel have been studied [28], [29], in which it was demonstrated that CB oscillations are induced by the additional dots originating from the dopant pileup, rather than the geometrical structure of the channel itself. In our case, we believe that the geometrical structure is responsible, because the lighly doped Si channel was used. In order to confirm this, the size of the smallest dot, which mainly determines the *I–V* characteristics, is estimated from the backgate capacitance (C_{bg}). From the CB oscillations in Fig. 3, C_{bg} is calculated to be about 0.15 aF for SHD and 0.18 aF for the SED, respectively, using the relation $C_{bg} = e/\delta V_{bg}$. Here, the average period δV_{bg} of 0.9 V for SHD and 1.1 V for SED, are used (δV_{bg} is roughly determined from the current peaks indicated by arrows in Fig. 3). Assuming that the dot has a semi-spherical shape with a radius r, the backgate capacitance is expressed as $C_{bg} = \epsilon_o \epsilon_{SiO_2} \pi r^2 / t_{BOX}$, where ϵ_o is the permittivity in vacuum, ϵ_{SiO_2} the relative dielectric constant of SiO_2 and t_{BOX} the buried SiO_2 (BOX) thickness. For $C_{bg} = 0.1 - 0.2$ aF and $t_{BOX} = 90$ nm, the radius r is estimated to be about 9–13 nm. This value is in good agreement with the dot size obtained from AFM image. Therefore, the observed CB oscillations are due to the geometrical structures of the dot formed by the nano-LOCOS process.

Next, we estimate the charging energy E_c of the smallest dot which dominates the *I–V* characteristics. From the contour plots of Fig. 5, the total capacitance C_Σ is obtained to be about 16 aF and 14 aF for SHD and SED, respectively. These values lead to the charging energy E_c of 5 and 5.7 meV for SHD and SED, respectively. The charging energy can be estimated also from the temperature dependence of the CB oscillation peaks, as shown in Fig. 6. In this measurement, the V_{ds} was kept at -15 mV with a V_{bg} interval of 0.1 V. It can be seen that as the temperature increases, the peaks broaden because of thermal broadening of the electron energy distribution. However, some oscillation peaks remain up to about 60 K for both devices. Since the CB effect becomes prominent if the charging energy E_c exceeds the thermal energy kT, there is a relation between E_c and T_{max}, $E_c = kT_{max}$, where k is the Boltzmann constant and T_{max} is the maximum temperature for the CB operation [30]. From this relationship, the charging energy is calculated to be 5.2 meV. This value agrees with E_c obtained from the contour plots.

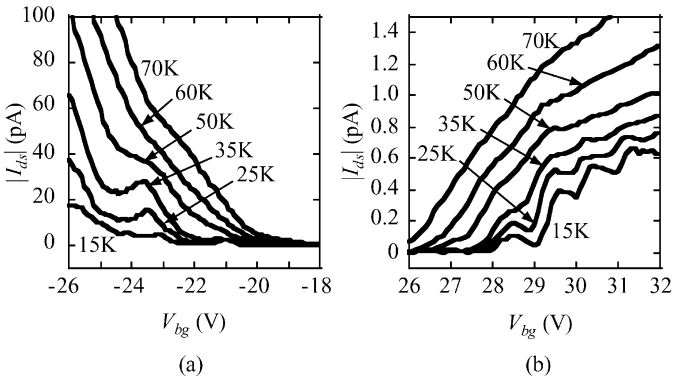

Fig. 6. Temperature dependence of I_{ds} at fixed $V_{ds} = -15$ mV for (a) SHD and (b) SED conditions.

Finally, we make a brief discussion on another temperature effect. It is known that CB peaks split into some sharp peaks with decreasing temperature in the multidot system [2], [31]. However, in Fig. 6, prominent splitting is hardly observed in our measurements. We believe that this is because of the measurement conditions, i.e., the V_{bg} interval is not short enough for the observation of peak splitting.

IV. Conclusion

We have presented the fabrication method and carrier transport characteristics of a 2-D Si multidot SET device in SOI substrate. The multidots are formed by using nano-LOCOS process developed by the authors. It was demonstrated that our device has ambipolar CB characteristics, in which the single-electron and single-hole transport phenomena were clearly observed at temperatures up to 60 K. In both CB characteristics, the spacing between the current peaks in the CB oscillations is not constant and the rhombus-shaped structures in the current contour plot for $V_{ds} - V_{bg}$ show open diamond. These features are associated with the electron/hole transport through Si multidot structure. Moreover, it was confirmed that the single-charge transport are induced from the geometrical structures of the dots, indicating that the characteristics can be tuned up by nano-LOCOS process.

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References

[1] Y. Takahashi, M. Nagase, H. Namatsu, K. Kurihara, K. Iwadate, Y. Nakajima, S. Horiguchi, K. Murase, and M. Tabe, "Fabrication technique for Si single-electron transistor operating at room temperature," *Elect. Lett.*, vol. 31, pp. 136–137, 1995.

[2] H. Ishikuro, T. Fujii, T. Saraya, G. Hashiguchi, T. Hiramoto, and T. Ikoma, "Coulomb blockade oscillations at room temperature in a Si quantum wire metal-oxide-semiconductor field-effect-transistor fabricated by anisotropic etching on a silicon-on-insulator substrate," *Appl. Phys. Lett.*, vol. 68, pp. 3585–3587, 1996.

[3] K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai, and K. Seki, "Transport characteristics of polycrystalline-silicon wire influenced by single-electron charging at room temperature," *Appl. Phys. Lett.*, vol. 67, pp. 828–830, 1995.

[4] K. Nakazato, T. J. Thornton, J. White, and H. Ahmed, "Single-electron effects in a point contact using side-gate in delta-doped layers," *Appl. Phys. Lett.*, vol. 61, pp. 3145–3147, 1992.
[5] A. A. M. Staring, H. Van Houten, C. W. J. Beenakker, and C. T. Foxon, "Coulomb-blockade oscillations in disordered quantum wires," *Phys. Rev. B.*, vol. 45, pp. 9222–9236, 1992.
[6] J. Park and P. L. McEuen, "Formation of a p-type quantum dot at the end of an n-type carbon nanotube," *Appl. Phys. Lett.*, vol. 79, pp. 1363–1365, 2001.
[7] B. Babic, M. Iqbal, and C. Schonenberger, "Ambipolar field-effect transistor on as-grown single-wall carbon nanotubes," *Nanotechnology*, vol. 14, pp. 327–331, 2003.
[8] C. S. Lent, P. D. Tougaw, W. Porod, and G. H. Berstein, "Quantum cellular automata," *Nanotechnology*, vol. 4, pp. 49–57, 1993.
[9] C. S. Lent and P. D. Tougaw, "A device architecture for computing with quantum dots," *Proc. IEEE*, vol. 85, pp. 541–557, Apr. 1997.
[10] M. Tabe, Y. Terao, R. Nuryadi, Y. Ishikawa, N. Asahi, and Y. Amemiya, "Simulation of visible light induced effects in a tunnel junction array for photonic device applications," *Jpn. J. Appl. Phys.*, pt. 1, vol. 38, no. 1B, pp. 593–596, 1999.
[11] H. Matsuoka, T. Ichiguchi, T. Yoshimura, and E. Takeda, "Coulomb blockade in the inversion layer of a Si metal-oxide-semiconductor field-effect transistor with a dual-gate structure," *Appl. Phys. Lett.*, vol. 64, pp. 584–588, 1994.
[12] J. W. Park, K. S. Park, B. T. Lee, C. H. Lee, S. D. Lee, J. B. Choi, K. H. Yoo, J. Kim, S. C. Oh, S. I. Park, K. T. Kim, and J. J. Kim, "Enhancement of Coulomb blockade and tenability by multidot coupling in a silicon-on-insulator-based single-electron transistor," *Appl. Phys. Lett.*, vol. 75, pp. 566–568, 1999.
[13] K. Uchida, J. Koga, R. Ohba, S. Takagi, and A. Toriumi, "Silicon single-electron tunneling device fabricated in an undulated ultrathin silicon-on-insulator," *J. Appl. Phys.*, vol. 90, no. 7, pp. 3551–3557, 2001.
[14] M. Tabe, M. Kumezawa, T. Yamamoto, S. Makita, T. Yamaguchi, and Y. Ishikawa, "Formation of high-density silicon dots on a silicon-on-insulator substrate," *Appl. Surf. Sci.*, vol. 142, pp. 553–557, 1999.
[15] Y. Ishikawa, S. Makita, J. Zhang, T. Tsuchiya, and M. Tabe, "Capacitance-voltage study of silicon-on-insulator structure with an ultrathin buried SiO_2 layer fabricated by wafer bonding," *Jpn. J. Appl. Phys.*, vol. 38, pp. L789–L791, 1999.
[16] R. Nuryadi, Y. Ishikawa, and M. Tabe, "Formation and ordering of self-assembled Si islands by ultrahigh vacuum annealing of ultrathin bonded silicon-on-insulator," *Appl. Surf. Sci.*, vol. 159/160, pp. 121–125, 2000.
[17] R. Nuryadi, Y. Ishikawa, Y. Ono, and M. Tabe, "Thermal agglomeration of single-crystalline Si layer on buried SiO_2 in ultrahigh vacuum," *J. Vac. Technol. B*, vol. 20, pp. 167–172, 2002.
[18] O. Janzen and W. Monch, "Comment on 'initial stages of nitridation od Si(111) surface: x-ray photoelectron spectroscopy and scanning tunneling microscopy studies' by M. Tabe and T. Yamamoto," *Surf. Sci.*, vol. 431, pp. 278–280, 1999.
[19] M. Tabe and T. Yamamoto, "Initial stages of nitridation od Si(111) surface: x-ray photoelectron spectroscopy and scanning tunneling microscopy studies," *Surf. Sci.*, vol. 376, pp. 99–112, 1997.
[20] ——, "Nanometer-scale local oxidation of silicon nitride islands formed in the early stages of nitridation," *Appl. Phys. Lett.*, vol. 69, pp. 2222–2224, 1996.
[21] H. Ishikuro and T. Hiramoto, "On the origin of tunneling barriers in silicon single electron and single hole transistors," *Appl. Phys. Lett.*, vol. 74, pp. 1126–1128, 1999.
[22] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley, 1981, ch. 5, p. 291.
[23] M. B. A. Jalil, H. Ahmed, and M. Wagner, "Analysis of multiple-tunnel junctions and their application to bidirectional electron pumps," *J. Appl. Phys.*, vol. 84, pp. 4617–4624, 1998.
[24] R. A. Smith and H. Ahmed, "Gate controlled Coulomb blockade effects in the conduction of a silicon quantum wire," *J. Appl. Phys.*, vol. 81, pp. 2699–2703, 1997.
[25] K. Nakazato and H. Ahmed, "The multiple-tunnel junction and its application to a single-electron memory and logic circuits," *Jpn. J. Appl. Phys.*, vol. 34, pp. 700–706, 1995.
[26] G.-L. Ingold and Y. V.Yu V. Nazarov, *Single Charge Tunneling*, H. Grabert and M. H. Deverot, Eds. New York: Plenum, 1992.
[27] F. Wakaya, F. Yoshioka, H. Higurashi, S. Iwabuchi, Y. Nagaoka, and K. Gamo, "Control of single-electron device using environmental impedance modulation," *Jpn. J. Appl. Phys.*, pt. 1, vol. 38, no. 5A, pp. 2812–2815, 1999.
[28] A. Tilke, R. H. Blick, H. Lorenz, J. P. Kotthaus, and D. A. Wharam, "Coulomb blockade in quasimetallic silicon-on-insulator nanowires," *Appl. Phys. Lett.*, vol. 75, pp. 3704–3706, 1999.
[29] R. Augke, W. Eberhardt, C. Single, F. E. Prins, D. A. Wharam, and D. P. Kern, "Doped silicon single electron transistors with single island characteristics," *Appl. Phys. Lett.*, vol. 76, pp. 2065–2067, 2000.
[30] T. Koester, F. Goldschmidtboeing, B. Hadam, J. Stein, A. Altmeyer, B. Spangenberg, H. Kurz, R. Neumann, K. Brunner, and G. Abstreiter, "Direct patterning of single electron tunneling transistors by high resolution electron beam lithography on highly doped molecular beam epitaxy grown silicon films," *J. Vac. Technol. B*, vol. 16, pp. 3804–3807, 1998.
[31] F. R. Waugh, M. J. Berry, D. J. Mar, R. M. Westervelt, K. L. Champman, and A. C. Gossard, "Single-electron charging in double and triple quantum dots with tunable coupling," *Phys. Rev. Lett.*, vol. 75, pp. 705–708, 1995.

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