Quantized electron transfer through random multiple tunnel junctions in phosphorus-doped silicon nanowires

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(Received 25 July 2007; published 17 August 2007)

We have demonstrated numerically and experimentally that quantized electron transfer can be achieved in single-gated random multiple tunnel junctions. Extensive Monte Carlo simulations based on Coulomb blockade orthodox theory show that nonhomogeneous distributions of capacitances energetically favor one-by-one electron shuttling between the electrodes during each cycle of a gate voltage. This numerical prediction is supported by our experimental results on Si nanowire field-effect transistors with the channel moderately doped with phosphorus. Ionized dopants within the device channel locally modulate the potential, creating a naturally random one-dimensional multiple-tunnel-junction array. Under ac-gate operation, small current plateaus or inflections aligned at $\pm nef$ appear in the I_d-V_d characteristics, suggesting that quantized electron transfer is achievable in such naturally disordered systems.

DOI: 10.1103/PhysRevB.76.075332 PACS number(s): 73.23.Hk, 73.63.Kv, 73.63.Nm

I. INTRODUCTION

Ordered quantized electron transport has been intensively investigated in metal-based quantum-dot arrays with basically uniform distribution of parameters[1–3] and recently in semiconductor single-electron devices.[4–7] As an alternative way to fabricating quantum dots by lithographic means, in doped silicon nanowire field-effect transistors (FETs), randomly distributed ionized impurities in the channel modulate the potential, creating a multiple-tunnel-junction (MTJ) array with naturally nonuniform parameters.[8–11] Only a few studies have treated similar nonhomogeneous systems from the viewpoint of ordered electron transfer, numerically showing that it could be achieved in one-dimensional (1D) arrays with specific parameter arrangements[12] or, in some cases, in two-dimensional multidot arrays.[13]

In this work, we demonstrate that quantized electron transfer is promoted in single-gated field-effect transistor structures containing random 1D MTJ arrays. Our numerical results are supported by the experimental observation of plateaus or inflections aligned around *nef* levels in the drain current (I_d)–drain voltage (V_d) characteristics measured under ac operation for Si nanowire FETs with the channel moderately doped with phosphorus.

II. NUMERICAL DEMONSTRATION OF QUANTIZED ELECTRON TRANSFER IN NONHOMOGENEOUS MULTIPLE-TUNNEL-JUNCTION ARRAYS

The numerical analysis was performed with a Monte Carlo algorithm based on the orthodox theory of Coulomb blockade[14] for 1D arrays of interacting quantum dots coupled to a common gate. During each period of ac-gate bias, the system is allowed to reach its equilibrium configuration by setting the pulse period sufficiently larger than characteristic tunneling times through any of the junctions connecting the quantum dots. Electron transport is monitored for 1000 ac-gate cycles. We purposely incorporated randomness of dot size and interdot coupling as dispersion of gate capacitances and junction capacitances, respectively. Parameter dispersion is chosen in a range reflecting practical device conditions for dopant-induced quantum dots, presented as an experiment in the latter half of this paper. The temperature was set to $T=0$ K in all simulations shown in this paper, which allows a comprehensive description of the way the system energy changes during a cycle of ac-gate bias in the absence of thermal effects.

Figure 1 shows the equivalent circuit and numerical results for 1D arrays with four quantum dots coupled to a common gate through gate capacitors (C_{gi}, $i=1-4$). As illustrated in Fig. 1(a), uniform junction capacitances ($C_j=0.5$ aF) and junction resistances ($R_j=100$ kΩ) have been considered. Periodic bias is applied with a frequency $f=1$ MHz to the gate between 0 and 100 mV ($=0.75\ e/C_g$), where C_g is the average gate capacitance, 1.2 aF. Prior to this simulation, we estimated the gate capacitance for single-dopant-induced quantum dots embedded in SiO_2 assuming a model of a spherical capacitor with the inner shell with a radius equal to the Bohr radius for phosphorus in Si (≈ 2.5 nm) and the outer shell with a radius equal to the gate oxide thickness (≈ 50 nm, as in our experimental devices). This estimated value is approximately 1.2 aF. However, since some dopant-induced quantum dots may have smaller or larger gate capacitances depending on the dopant location and position relative to neighboring dopants, gate capacitances have been varied around this average value in the numerical simulations (for instance, from 0.1 to 10 aF in the case illustrated in Fig. 3). The choice of junction capacitances around 0.5 aF was justified by an estimation based on average interdopant distance in the experimentally investigated Si:P nanowire FETs. Junction resistances are not an essential parameter in the frame of the model that will be described below and we assumed them to be 100 kΩ ($>R_Q \approx 26$ kΩ), which allows us to use the orthodox theory of Coulomb blockade.

Figure 1(b) shows an example of I_d-V_d characteristics simulated for a four-quantum-dot system with uniform junction parameters ($C_j=0.5$ aF and $R_j=100$ kΩ) but with a non-

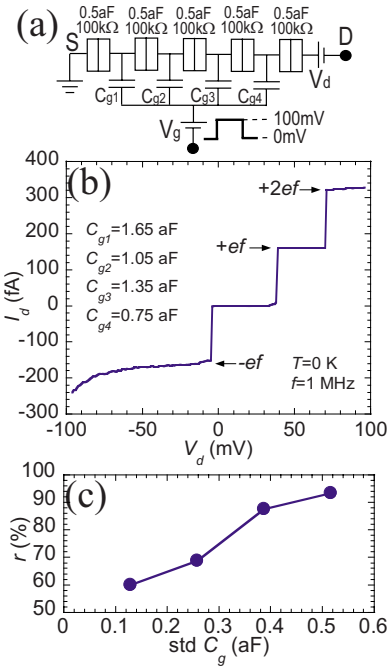

FIG. 1. (Color online) (a) Equivalent circuit of typically investigated 1D arrays. (b) Example of ac I_d-V_d characteristics for uniform junction capacitances and resistances. Current plateaus can be observed at *nef* levels. (c) Effect of gate capacitance dispersion on quantized electron transfer. Rate r is defined as the number ratio of gate capacitance arrangements exhibiting quantized electron-transfer plateaus to all 16 investigated configurations.

homogeneous arrangement of gate capacitances $\{C_g\}$, i.e., $C_{g1}=1.65$ aF, $C_{g2}=1.05$ aF, $C_{g3}=1.35$ aF, and $C_{g4}=0.75$ aF. Clear current plateaus can be observed aligned at *nef* levels, with $n=-1$, 1, and 2, indicating that during every gate voltage cycle, a quantized number of electrons can be transferred from one electrode to the other. Figure 1(c) shows the statistical analysis of such quantized electron transfer in one-dimensional MTJ arrays with different degrees of disorder (indicated by different values of the standard deviation in $\{C_g\}$ distribution). For each degree of dispersion (standard deviation) in gate capacitance distribution, 16 different $\{C_g\}$ configurations have been calculated. The rate r represented on the vertical axis is defined as the number ratio of $\{C_g\}$ configurations that exhibit *nef* plateaus in the simulated I_d-V_d characteristics to all calculated configurations. It can be observed that by increasing the dispersion in $\{C_g\}$, ordered quantized electron transfer is achieved with a surprisingly higher rate, i.e., up to about 95% for the maximum standard deviation of 0.52 aF taken into consideration in this study. This suggests that quantized electron transfer is promoted by larger variations in the gate capacitance distribution. The energetic considerations for this result are addressed in Fig. 2.

As another example, shown in Fig. 2(a), we have considered another $\{C_g\}$ arrangement with the same uniform junction capacitances and resistances. For this specific $\{C_g\}$ arrangement ($C_{g1}=1.1$ aF, $C_{g2}=0.8$ aF, $C_{g3}=1.1$ aF, and $C_{g4}=1.8$ aF), the device exhibits a pump-like single-electron transfer [Fig. 2(b)] as an *ef* current plateau extended around

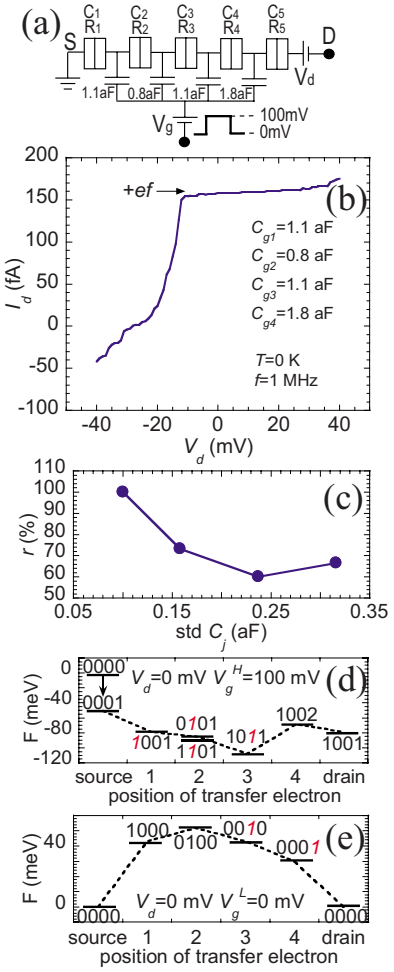

FIG. 2. (Color online) (a) Equivalent circuit of 1D arrays for investigating the effects of junction parameter randomness. (b) ac I_d-V_d characteristics simulated for uniform junction capacitances and resistances. An *ef* current plateau appears aligned around $V_d=0$ V. (c) Effect of junction capacitance dispersion on quantized electron transfer. Rate r is defined as the number ratio of junction capacitance arrangements that exhibit the *ef* current plateau to all 16 investigated configurations. [(d) and (e)] System free energy profiles calculated at $V_d=0$ V for the system shown in (a) as a function of electron position during one gate voltage pulse, i.e., at $V_g^H=100$ mV and at $V_g^L=0$ mV, respectively.

$V_d=0$ V. Thus, it can be seen from a number of simulations for different $\{C_g\}$ configurations that a variety of electron-transfer phenomena are found. As a next question arises regarding the effect of dispersion of junction capacitances C_j on this single-electron-transfer operation, we have simulated the I_d-V_d characteristics for 16 different junction capacitance arrangements $\{C_j\}$ for different standard deviations in the $\{C_j\}$ distribution. In Fig. 2(c), the rate r represented on the vertical axis is again defined as the number ratio of configurations that exhibit the *ef* current plateaus to all investigated configurations. Higher dispersion in junction capacitances $\{C_j\}$ tends to distort the favorable free energy profile and thus shrinks the parameter space available for the quantized electron transfer. It should be noted, however, that even for the highest standard deviation investigated (0.32 aF for an aver-

age junction capacitance of 0.5 aF), there are still more than 60% of configurations which still allow for the single-electron transfer to be observed as an *ef* current plateau in the I_d-V_d characteristics. This suggests that the mechanism behind this operation is mainly governed by the gate capacitance arrangement, at least for systems with short screening lengths ($C_j/C_g<1$), as we have investigated in this study. This mechanism can be understood from Figs. 2(d) and 2(e), which show the system free energy (F) when electrons occupy different dots between the source and drain at $V_d=0$ V [where $I_d \approx 160$ fA$=ef$ in Fig. 2(b)] during one period of the ac bias. At the high level of the gate voltage pulse ($V_g^H=100$ mV), one electron coming from the source is "trapped" at a certain dot (dot 3 in this case) due to the formation of Coulomb blockade in the adjacent junctions, as illustrated in Fig. 2(d). It is worth noting that two other electrons that enter the system at dots 1 and 4 contribute to the shaping up of the free energy profile so that the transfer electron can be trapped inside the array. When the gate voltage is lowered (to $V_g^L=0$ mV), the electrons present in the end quantum dots return to their original electrodes without participating in the current. Due to these two initial events [not shown in Fig. 2(e)], the trapped electron, prevented from tunneling back to the source by the Coulomb blockade, is transferred forward toward the drain, as indicated by the free energy profile shown in Fig. 2(e). This ratchet-like free energy profile can be readily formed in systems with larger variations of gate capacitances which may favor one-directional charge transfer with the assistance of several additional electrons. These *assistant electrons* naturally shape up the ratchetlike energy profile in many cases, leading to the net transfer of one electron per cycle of gate voltage.

For further study of the mechanism behind quantized electron-transfer operation, the effects of varying one of the gate capacitances in nonhomogeneous MTJ systems are also examined. The equivalent circuits of the investigated structures are shown in Fig. 3(a) (for four-quantum-dot systems) and in Fig. 3(b) (for five-quantum-dot systems). The mesh plots in Figs. 3(c) and 3(d) show the average number of electrons transferred per gate voltage cycle (N_e/cycle) as a function of source-drain bias V_d and source-side gate capacitance C_{g1}. Plateaus at N_e/cycle$=1$ appear for a wide range of V_d and C_{g1} in both circuits, while quasiperiodical features are also found for changing C_{g1}. The periodicity observed in both circuits corresponds to the addition of a single electron on the source-side dot. These additional electrons, present in the source-side larger quantum dot, work as assistant electrons necessary for quantized electron transfer to be achieved. Although the rate of undesired events is expected to increase with increasing the number of junctions, it is found from the above numerical results that a large percentage of random quantum-dot arrays are useful for ordered quantized electron transfer in simple single-gated structures.

III. EXPERIMENTAL OBSERVATION OF QUANTIZED ELECTRON TRANSFER IN Si:P NANOWIRE FIELD-EFFECT TRANSISTORS

In order to support these numerical findings, we have experimentally studied random MTJ arrays formed in Si nanowire FETs having the channel moderately doped with phosphorus. Quantum-dot arrays in Si can be formed by thickness modulation of ultrathin Si layers,[15,16] or by the discrete distribution of dopant ions in FET structures.[8–11] In this work, we took the latter approach motivated by the recent study of Si:P systems,[17] as well as by the importance of phosphorus dopants for applications such as quantum computing.[18] The nanowire channels, patterned by electron-beam lithography followed by oxidation of silicon-on-insulator substrates, have typical length, width, and thickness of approximately 100, 10, and 10 nm, respectively. Only one top gate completely covers the channel through a 50 nm SiO_2 layer. Taking into account the channel dimensions and the estimated doping concentration ($N_d \sim 1\times10^{18}$ cm^{-3}), only several impurity atoms (fewer than ten) are expected to be present between the source and drain in the Si nanowire. The ionized dopants can modulate the potential within the channel, effectively creating a MTJ array with naturally random parameters due to randomness in the position of the impurities. The mean distance between phosphorus donors ($N_d^{-1/3} \sim 10$ nm) is of the same order with both width and height of the nanowire, so it can be assumed that the resultant array of quantum dots is 1D. The effects of the ionized dopants can be observed in Fig. 4, which shows the dc drain current–gate voltage (I_d-V_g) characteristics measured at $T=5.5$ K and $V_d=10$ mV for a reference undoped-channel FET (dotted curve) and for a phosphorus-doped-channel FET (solid curve) with essentially the same dimensions. The undoped-channel FET exhibits weak but quasiperiodic Coulomb oscillations with a period in the range of 300–400 mV. This suggests that the undoped Si nanowire acts as a single Coulomb island in the FET structure. On the other hand, the doped-channel FET exhibits an irregular pattern of sharp Coulomb oscillations with voltage spacings between consecutive peaks varying from 30 to 150 mV. These observed irregularities are a clear evidence of the formation of a MTJ array with nonhomogeneous parameters in the channel due to the ionized donors.[19]

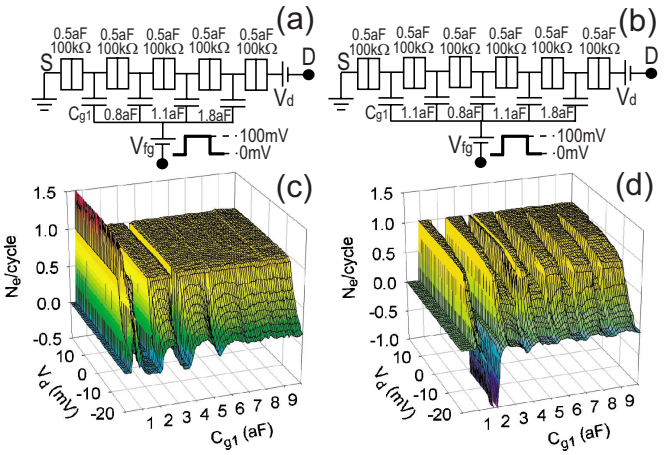

FIG. 3. (Color online) [(a) and (b)] Equivalent circuits for 1D arrays with four and five quantum dots, respectively, and parameters chosen for analysis. [(c) and (d)] Mesh plots of average number of electrons transferred between the electrodes per cycle (N_e/cycle) as a function of source-drain bias V_d and source-side gate capacitance C_{g1} for the cases of (a) and (b), respectively.

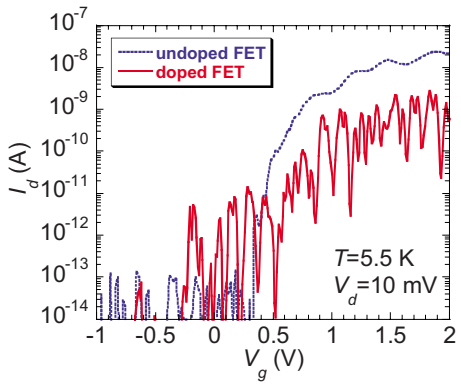

FIG. 4. (Color online) Experimental dc I_d-V_g characteristics for a reference undoped-channel FET (dotted curve) and for a FET having the same dimensions but the channel moderately doped with phosphorus (solid curve).

Thus, it can be understood that dopant-induced potential fluctuations are acting as 1D MTJ arrays with natural parameter dispersion, similarly to the systems treated in our numerical simulations.

Therefore, we have studied the ac operation of the phosphorus-doped-channel FETs. For the ac measurements, a quasisinusoidal pulse was applied to the gate with a peak-to-peak amplitude $V_{\mathrm{ampl}}=100$ mV and a frequency $f=1$ MHz, while the temperature was set to 5.5 K. Figures 5(a) and 5(b) show two examples of ac I_d-V_d characteristics (solid curves) measured for the same device at two different gate offset voltages of $V_{g0}=-0.39$ and -0.6 V, respectively. The gate voltage offset V_{g0} is defined here as the mean value between the minimum and maximum gate voltages during one pulse cycle. The dc I_d-V_d characteristics (dashed curves) measured at the same gate voltages $V_g=-0.39$ and -0.6 V, respectively, are also shown and clear Coulomb gaps can be seen around $V_d=0$ V. However, most interesting features can be noticed under ac operation, when quantized electron transfer is observed as small current plateaus or inflections aligned at $\pm nef$ current levels. These results indicate the validity of our numerical prediction, although incompleteness of the current plateaus such as insufficient flatness may be due to undesirable phosphorus atom distribution within the channel and/or to thermally activated events. Furthermore, as shown in Fig. 5(c), the current measured at $V_d=0$ V under ac operation exhibits peaks ($-ef<I_d<+ef$) for certain gate voltage offsets V_{g0}. This also indicates that nonhomogeneous parameter distribution, as naturally found in the investigated Si:P nanowire FETs, provides the Coulomb blockade ratchet mechanism[20] which favors one-directional transport even in the absence of source-drain bias.

Concerning the yield of this single-electron-transfer operation, it is worth mentioning that in this work, we have measured only two devices because only two devices were available with the same size and the same doping concentration in the sample. The other device with essentially the same dimensions showed a similar behavior under ac-gate operation, i.e., quantized electron transfer. Even though the number of investigated devices is small, the fact that we have not performed any specific selection procedure suggests that ordered charge transfer is achievable with high probability in such naturally disordered systems.

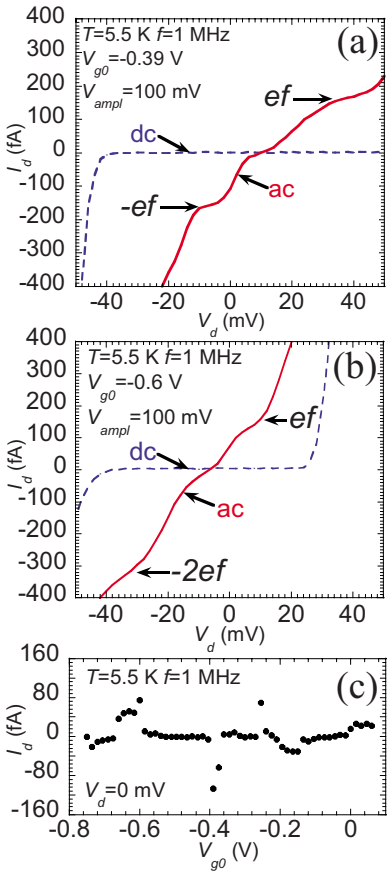

FIG. 5. (Color online) [(a) and (b)] I_d-V_d characteristics measured under dc operation (dashed curves) and ac operation (solid curves) for the doped-channel FET for offset gate voltages of -0.39 and -0.6 V, respectively. Small plateaus aligned around $\pm nef$ current levels can be noticed in both cases. (c) I_d at $V_d=0$ V under ac operation as a function of gate offset voltage V_{g0}.

IV. CONCLUSIONS

We have shown in this work that electrons can be transferred one by one through random 1D MTJ arrays during each cycle of one ac-gate bias commonly applied to the entire array. Numerical simulations suggest that dispersion in gate capacitances provides the ratchet-like free energy profile necessary for quantized electron transfer, while assistant electrons within the channel also contribute to the shaping up of this profile. We have also experimentally studied the ac behavior of 1D MTJ arrays formed by ionized dopants in phosphorus-doped Si-nanowire FETs and we have observed quantized electron transfer under ac-gate operation. This supports our numerical findings since Si:P systems are expected to contain natural parameter dispersion due to the uncon-

trolled conventional doping process. Because of the full compatibility with complementary metal oxide semiconductor technologies and relatively simple design, such devices may become a basic element for future memory and logic circuits. Inaccuracy of the single-electron transfer in such random MTJ devices is, however, the trade-off factor in application.

ACKNOWLEDGMENTS

The authors would like to thank H. Ikeda, R. Nuryadi, and K. Yokoi of the Research Institute of Electronics, Shizuoka University, for helpful discussions and suggestions. This work was partially supported by MEXT KAKENHI (No. 16106006, No. 18063010, and No. 16206038).

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[1] L. J. Geerligs, V. F. Anderegg, P. A. M. Holweg, J. E. Mooij, H. Pothier, D. Esteve, C. Urbina, and M. H. Devoret, Phys. Rev. Lett. **64**, 2691 (1990).

[2] H. Pothier, P. Lafarge, P. F. Orfila, C. Urbina, D. Esteve, and M. H. Devoret, Physica B **169**, 573 (1991).

[3] X. Jehl, M. W. Keller, R. L. Kautz, J. Aumentado, and J. M. Martinis, Phys. Rev. B **67**, 165331 (2003) and references therein.

[4] L. P. Kouwenhoven, A. T. Johnson, N. C. van der Vaart, C. J. P. M. Harmans, and C. T. Foxon, Phys. Rev. Lett. **67**, 1626 (1991).

[5] Y. Ono and Y. Takahashi, Appl. Phys. Lett. **82**, 1221 (2003).

[6] A. Fujiwara, N. M. Zimmerman, Y. Ono, and Y. Takahashi, Appl. Phys. Lett. **84**, 1323 (2004).

[7] J. Ebbecke, N. E. Fletcher, T. J. B. M. Janssen, F. J. Ahlers, M. Pepper, H. E. Beere, and D. A. Ritchie, Appl. Phys. Lett. **84**, 4319 (2004).

[8] R. Augke, W. Eberhardt, S. Strähle, F. E. Prins, and D. P. Kern, Microelectron. Eng. **46**, 141 (1999).

[9] T. Koester, F. Goldschmidtboeing, B. Hadam, J. Stein, S. Altmeyer, B. Spangenberg, H. Kurz, R. Neumann, K. Brunner, and G. Abstreiter, Jpn. J. Appl. Phys., Part 1 **38**, 465 (1999).

[10] G. J. Evans, H. Mizuta, and H. Ahmed, Jpn. J. Appl. Phys., Part 1 **40**, 5837 (2001).

[11] T. Shinada, S. Okamoto, T. Kobayashi, and I. Ohdomari, Nature (London) **437**, 1128 (2005).

[12] M. G. Ancona, J. Appl. Phys. **81**, 3311 (1997).

[13] H. Ikeda and M. Tabe, J. Appl. Phys. **99**, 073705 (2006) and references therein.

[14] K. K. Likharev, IEEE Trans. Magn. **23**, 1142 (1987).

[15] R. Nuryadi, Y. Ishikawa, and M. Tabe, Phys. Rev. B **73**, 045310 (2006).

[16] K. Uchida, J. Koga, R. Ohba, S. Takagi, and A. Toriumi, J. Appl. Phys. **90**, 3551 (2001).

[17] Y. Ono, J.-F. Morizur, K. Nishiguchi, K. Takashina, H. Yamaguchi, K. Hiratsuka, S. Horiguchi, H. Inokawa, and Y. Takahashi, Phys. Rev. B **74**, 235317 (2006).

[18] B. E. Kane, Nature (London) **393**, 133 (1998).

[19] F. R. Waugh, M. J. Berry, C. H. Crouch, C. Livermore, D. J. Mar, R. M. Westervelt, K. L. Campman, and A. C. Gossard, Phys. Rev. B **53**, 1413 (1996).

[20] Y.-S. Shin, W. Song, J. Kim, B.-C. Woo, N. Kim, M.-H. Jung, S.-H. Park, J.-G. Kim, K.-H. Ahn, and K. Hong, Phys. Rev. B **74**, 195415 (2006).