# A Submicrometer Lifted Diffused-Layer MOSFET

HIROSHI INOKAWA, TOSHIO KOBAYASHI, MEMBER, IEEE, AND KAZUHIDE KIUCHI

*Abstract*—**A new lifted diffused-layer (LID) MOSFET has been devised and fabricated, where the major portions of the source/drain (S/D) diffused layers are placed on top of the field insulator to reduce S/D parasitic capacitances. The primary feature of this MOSFET is that the structure and processing are especially developed for submicrometer gate lengths. The fabricated LID MOSFET with a 0.5-$\mu$m gate length and a 10-nm gate oxide thickness showed good electrical characteristics, such as a maximum transconductance of 115 mS/mm and an inverter delay time of 59 ps/stage.**

## I. Introduction

As THE size of a MOSFET is reduced, the parasitic capacitance of the source/drain (S/D) junction starts to limit its speed and power performance. This is because the lateral dimensions of the S/D junction cannot be scaled proportionally to the dimensions of the active area owing to the necessity of allowing for relatively large alignment error and preventing contact resistance increase.

In order to reduce the S/D junction capacitance, a unique lifted diffused-layer (LID) MOSFET has been produced. In this MOSFET, major portions of the S/D diffused layers are polycrystalline and are placed on top of the field insulator to reduce the S/D capacitances without using SOI [1]–[3] or a high-resistivity substrate [4]. Moreover, in contrast to other FET's similar to the LID MOSFET [5]–[7], the structure and processing of the LID MOSFET are especially developed for submicrometer gate lengths to take full advantage of the reduced S/D capacitances.

In this letter, we will briefly report on the structure, the fabrication process, and the electrical characteristics of submicrometer LID MOSFET's.

## II. Structure

A cross section of the LID MOSFET is shown in Fig. 1. In this MOSFET, the main portions of the S/D diffused layers are placed on top of the field insulator which, in this case, consists of layers of silicon nitride and silicon dioxide. This reduces the S/D parasitic capacitances. The channel region is located in a high-quality epitaxial silicon film deposited simultaneously with the S/D polysilicon film. In order to define the small gate region of a submicrometer MOSFET precisely, LOCOS techniques are avoided and the field insulator is directly patterned by anisotropic etching.

It should be noted that in the LID MOSFET, the gate electrode is placed exactly in a groove formed between the edges of the field insulator. Therefore the top of the gate, source, and drain electrodes can exist in one plane. This greatly relieves the difficulties in the metallization process caused by the irregularity of the device surface features.

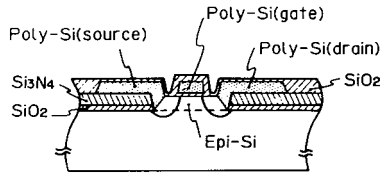



Fig. 1. Cross section of the LID MOSFET.

The additional advantages of the LID MOSFET structure, such as increased reliability of S/D contact, high immunity to the latch-up phenomenon in CMOS circuits, etc., have already been suggested elsewhere [2], [5]–[7].

## III. Fabrication Process

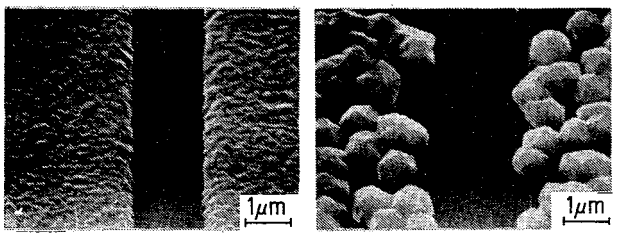
The LID MOSFET fabrication steps are as follows. First, a field insulator consisting of silicon nitride and silicon dioxide layers is patterned to define the gate region. Next, undoped epitaxial and polycrystalline silicon films are simultaneously deposited to a thickness of 240 nm using $SiH_4$ CVD. Then, each MOSFET is isolated by field oxidation, and this is followed by gate oxidation and channel implantation. After gate polysilicon deposition, gates with 0.5–50-$\mu$m lengths are defined in the small channel region with alignment errors less than 0.2 $\mu$m using optical lithography in a try-and-error manner. Although the gates could be defined using electron beam lithography or a self-alignment technique, conventional *g*-line lithography with overexposure is used for simplicity. Gate polysilicon oxidation, S/D implantation ($As^+$, 40 keV, $6\times10^{15}$ $cm^{-2}$), and the other fabrication steps follow the conventional n-MOS process flow.

The LID-MOSFET process contains two key steps. One is the simultaneous epitaxial and polycrystalline silicon film deposition. As reported earlier, polysilicon film deposited under high-temperature epitaxial conditions on silicon dioxide tends to have a rough surface owing to the reduced nucleus density [8]. This phenomenon, unsuitable for submicrometer structures, is prevented by two means. One is the use of a field insulator with a nitride top layer. The surface conditions of the polysilicon film deposited on silicon nitride and on silicon dioxide are shown in Fig. 2(a) and (b), respectively. The surface of the polysilicon on nitride is very smooth in contrast to that of polysilicon on oxide. An additional means of obtaining a smoother polysilicon surface is the reduction of the deposition temperature down to 950°C.

The other key step in the LID-MOSFET process is the etching of the gate polysilicon in the groove. In this etching, a

Manuscript received October 16, 198. revised December 3, 1986.
The authors are with NTT Electrical Communications Laboratories, 3-1, Morinosato Wakamiya, Atsugi-shi, Kanagawa 243-01, Japan.
IEEE Log Number 8613234.

0741-3106/87/0300-0098$01.00 




(a) (b)

Fig. 2. (a) Surface morphology of polysilicon film on silicon nitride, and (b) on silicon dioxide, deposited by atmospheric-pressure CVD at 950°C. Source gas is $SiH_4$ diluted by $H_2$. The center of the photograph is an epitaxial silicon film on an exposed silicon substrate.

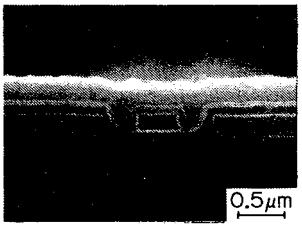



Fig. 3. SEM cross section of the fabricated LID MOSFET with a 0.5-μm gate length, covered with as-deposited PSG.

high etching rate ratio of polysilicon to silicon dioxide is needed. This is because the thickness in the vertical direction of the polysilicon on the groove wall is larger than that on the S/D diffused layer and the thin gate oxide on the S/D diffused layer must survive during the etching of the excessive polysilicon in the groove. To meet this need for high selectivity, anisotropic etching by low-pressure chlorine ECR plasma [9] is used to achieve a selectivity of 60. This results in a sharply etched profile with no residue.

Fig. 3 shows a fabricated LID MOSFET with a 0.5-μm gate length, covered with as-deposited PSG. It can be seen that most of the S/D diffused layer is lifted onto the insulator layer. Since the gate electrode is placed exactly in a groove, the surface of the PSG is very flat even without flow treatment.

## IV. Electrical Characteristics

All of the fabricated LID MOSFET's with gate lengths of 0.5–50 μm exhibited normal FET characteristics. The $I_d$–$V_d$ curves of an FET with a 0.5-μm gate length, a 50-μm gate width, 10-nm gate oxide thickness, and a channel doping of $6\times10^{16}$ $cm^{-3}$ are shown in Fig. 4. The maximum transconductance in the saturation region is calculated to be as high as 115 mS/mm, showing the effect of reducing the gate length down to the submicrometer range. The relatively high S/D resistance indicated in Fig. 4 is due to the high sheet resistance (480 Ω/□) of the lifted S/D region. This is the result of insufficient doping of the S/D region and the use of a polycrystalline material, and could be solved by optimizing the implantation condition and using the selective metal deposition or the self-aligned silicide technology.

Fig. 5 shows the subthreshold characteristics of the same LID MOSFET. The subthreshold slope is from 80 to 82 mV/decade and is the same as that of the long-channel one. Furthermore, the subthreshold slope does not vary with drain voltage between 0.01 and 3 V. This suggests that, although the

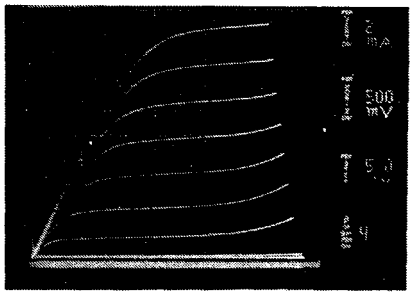


Fig. 4. $I_d$–$V_d$ curves of an LID MOSFET with a 0.5-μm gate length, a 50-μm gate width and a 10-nm gate oxide thickness. The gate voltage is stepped between 0 and 4 V. The maximum transconductance in the saturation region is 115 mS/mm.

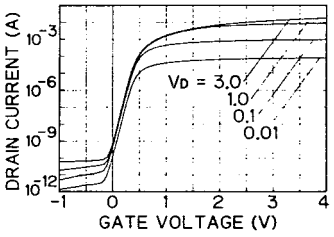



Fig. 5. Subthreshold characteristics of an LID MOSFET with a 0.5-μm gate length, a 50-μm gate width, and a 10-nm gate oxide thickness.

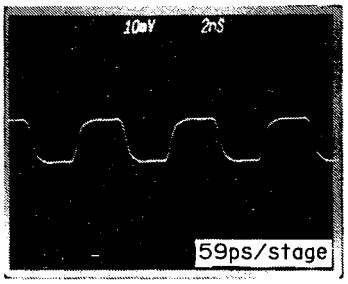



Fig. 6. Output waveform of a 51-stage E/E ring oscillator with a 0.5-μm gate length. The oscillator is operated with a single supply voltage of 5 V. The output source follower is supplied with 0.5 V.

gate length is as small as 0.5 μm, punchthrough does not occur in this device. The high leakage current shown in Fig. 5 could be attributed to the insufficient doping of the polysilicon S/D region.

Fifty-one-stage E/E ring oscillators were also fabricated and gave good results. The output waveform of an oscillator with a 0.5-μm gate length, operated at 5 V, is shown in Fig. 6. The gate delay time is 59 ps/stage and the power consumption is 3.1 mW/stage.

## V. Conclusions

Unique LID MOSFET's, where the S/D parasitic capacitance is reduced by placing the S/D diffused layer on a field insulator, have been designed and fabricated. In these MOSFET's submicrometer gate lengths are successfully realized by using an anisotropically etched field insulator with a nitride top layer and highly selective ECR plasma etching of the gate polysilicon.

The LID MOSFET with a 0.5-μm gate length and a 10-nm gate oxide thickness showed good electrical characteristics,

such as a maximum transconductance of 115 mS/mm and an inverter delay time of 59 ps/stage.

## Acknowledgment

The authors wish to thank H. Ikawa, S. Kuwano, and H. Yoshino for their technical cooperation in silicon CVD, and M. Kimizuka in ECR plasma etching. We also thank M. Kondo and E. Arai for helpful discussions.

## References

[1] B.-Y. Tsaur, R. W. Mountain, C. K. Chen, and J. C. C. Fan, "Merged CMOS/bipolar technologies utilizing zone-melting-recrystallized SOI films," *IEEE Electron Device Lett.*, vol. EDL-5, pp. 461–463, 1984.

[2] W. Baerg *et al.*, "A seeded-channel silicon-on-insulator (SOI) technology," *IEEE Electron Device Lett.*, vol. EDL-6, pp. 668–670, 1985.

[3] Y. Kobayashi, A. Fukami, and T. Nagano, "Characteristics of a 1.2-μm CMOS technology fabricated on an RF-heated zone-melting recrystallized SOI," *IEEE Electron Device Lett.*, vol. EDL-7, pp. 350–352, 1986.

[4] F. F. Fang and H. S. Rupprecht, "High performance MOS integrated circuit using the ion implanted technique," *IEEE J. Solid-State Circuits*, vol. SC-10, pp. 205–211, 1975.

[5] J. Sakurai, "A new buried-oxide isolation for high-speed high-density MOS integrated circuits," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 468–471, 1978.

[6] C. H. Dennison, A. T. Wu, P. K. Ko, C. I. Drowley, and D. Bradbury, "A novel MOS structure with S/D contacts over oxide (COO)," in *IEDM Tech. Dig.*, Dec. 1985, pp. 204–207.

[7] S. D. S. Malhi, K. E. Bean, R. Sundaresan, and L. R. Hite, "Overlaid CMOS," *Electron. Lett.*, vol. 22, pp. 598–599, 1986.

[8] W. A. P. Claassen and J. Bloem, "The nucleation of CVD silicon on $SiO_2$ and $Si_3N_4$ substrates," *J. Electrochem. Soc.*, vol. 127, pp. 194–202, 1980.

[9] T. Ono, C. Takahashi, M. Oda, and S. Matsuo, "Reactive ion stream etching and metallic compound deposition using ECR plasma technology," in *Symp. VLSI Technol., Dig. Tech. Papers*, May 1985, pp. 84–85.