Multipeak negative-differential-resistance device by combining single-electron and metal–oxide–semiconductor transistors

Hiroshi Inokawa,[a] Akira Fujiwara, and Yasuo Takahashi
NTT Basic Research Laboratories, 3-1 Morinosato Wakamiya, Atsugi-shi, Kanagawa Prefecture 243-0198, Japan

(Received 11 June 2001; accepted for publication 19 September 2001)

A multipeak negative-differential-resistance device is proposed. The device comprises a single-electron transistor (SET) and a metal–oxide–semiconductor field-effect transistor (MOSFET), and can, in principle, generate an infinite number of current peaks. Operation of the proposed device is verified at 27 K with a SET fabricated by the pattern-dependent oxidation process and a MOSFET on the same silicon-on-insulator wafer. Six current peaks and a peak-to-valley current ratio of 2.1 are obtained, and multiple-valued memory operation is successfully demonstrated. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1421085]

In a single-electron transistor (SET), Coulomb blockade is controlled by the gate, which is capacitively or resistively coupled to the Coulomb island, and the discreteness of the electric charge in the island results in unique current–voltage characteristics, i.e., a periodic increase and decrease of drain current as a function of the gate voltage.[1–3] Although this periodic nature is utilized in some applications,[4,5] the potential of SETs as functional elements has not been fully exploited. We report here a method by which to realize a SET-based multipeak negative-differential-resistance (NDR) device, that should have a wide range of applications such as multiple-valued memories,[6] analog-to-digital converters,[7] and multiple-valued logics.[8] Conventionally, multipeak NDR devices have been constructed with a series connection of resonant tunneling diodes (RTDs).[6–8] However, the number of peaks is determined by the number of diodes. It is also limited by accumulated series resistance, which should be smaller than the negative resistance of a single RTD.[6] The NDR device proposed here consists only of a SET and a metal–oxide–semiconductor field-effect transistor (MOSFET), and can, in principle, generate an infinite number of peaks. Using this device, multiple-valued memory operation is demonstrated.

A schematic of the proposed NDR device is shown in Fig. 1(a). The source of a MOSFET with fixed gate bias V_{gg} is connected to the drain of a SET. As illustrated in Fig. 1(b), the SET drain current I_d increases and decreases periodically as a function of the gate voltage V_{gs}.[1–3] However, the I_d has such a large dependence on the drain voltage V_{ds} that the peak current is almost proportional to V_{ds}, and the valley current increases more rapidly when the Coulomb blockade breaks. The MOSFET connected to the SET eliminates this large V_{ds} dependence of the SET characteristics by keeping V_{ds} nearly constant around $V_{gg}-V_{\mathrm{th}}$, where V_{th} is the threshold voltage of the MOSFET. This $V_{gg}-V_{\mathrm{th}}$ is set low enough to sustain Coulomb blockade. By connecting the SET gate to the MOSFET drain, the multipeak NDR characteristics shown in Fig. 1(c) are obtained as two-terminal $I-V$ characteristics. If a constant-current source I_o is connected to the combined SET-MOSFET device, the periodic nature of the $I-V$ characteristics results in a number of stability points, and this enables multiple-valued memory operation. Note that these multipeak characteristics originate from the characteristics of a single SET. And the number of peaks is infinite in principle, but is in practice limited by the breakdown voltage of the MOSFET drain or SET gate.

The above idea was verified with a SET fabricated by the pattern-dependent oxidation (PADOX) process[9–11] and with a MOSFET located on the same wafer. In the PADOX process, a one-dimensional Si wire patterned in silicon-on-insulator (SOI) is converted into a small Si island with a small tunnel capacitor at each end. Figure 2(a) shows the I_d-V_{gs} characteristics of a SET. Periodic drain–current peaks are clearly seen along with the effect of tunnel resistance modulation by the gate voltage. From Fig. 2 and a Coulomb diamond plot, the gate capacitance, source/drain capacitance, and tunnel resistance were calculated to be 0.27 aF, 2.7 aF, and 80–220 kΩ, respectively.

PADOX is highly compatible with the complementary MOS (CMOS) fabrication process, and areas other than that of the one-dimensional Si wire can readily be used as an ordinary MOSFET channel. Here, an n-type MOSFET with effective channel width of 12 μm, channel length of 14 μm, and gate oxide thickness of 90 nm was combined with the

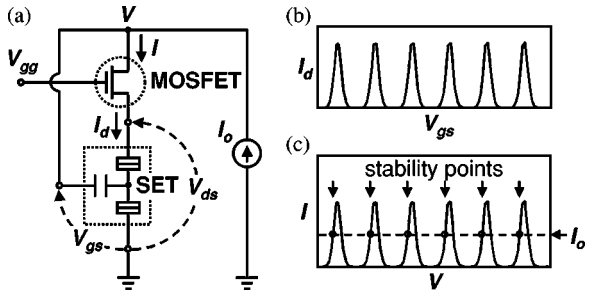

FIG. 1. (a) Schematic of the proposed multipeak NDR device comprising a SET and a MOSFET. A constant-current source I_o is connected for multiple-valued memory operation. (b) Typical I_d-V_{gs} (three-terminal) characteristics of a SET. (c) Expected $I-V$ (two-terminal) characteristics of the SET-MOSFET device. Load line I_o and the corresponding stability points for memory operation are also shown.

[a]Electronic mail: inokawa@aecl.ntt.co.jp

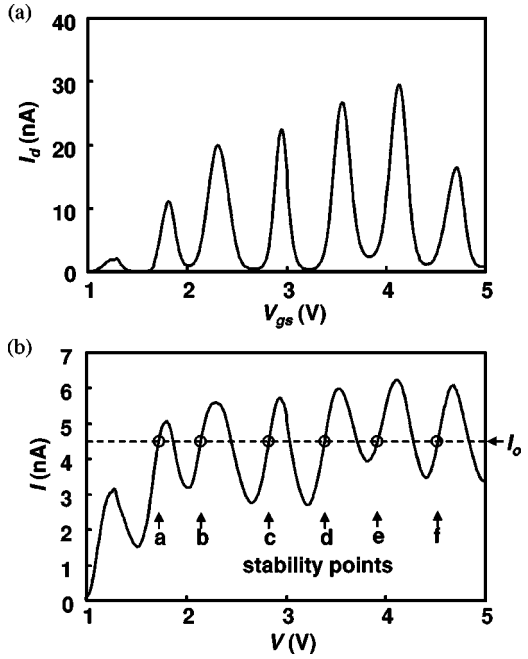

FIG. 2. (a) I_d–V_{gs} characteristics of a SET for V_{ds} of 10 mV, measured at 27 K. (b) $I-V$ characteristics of the proposed NDR device for V_{gg} of 1.08 V measured at 27 K. Stability points ($a-f$) expected for a current load of 4.5 nA are indicated by circles. The SET was fabricated by the PADOX process (Refs. 9–11) together with the MOSFET on the same SOI wafer.

SET. The threshold voltage V_{th} and subthreshold slope S corresponding to drain voltage V_{gs} of 3 V and operating current I_o of 4.5 nA, were 1.07 and 60 mV/dec, respectively. All devices were operated and measured at 27 K.

$I-V$ characteristics of the combined SET-MOSFET device are shown in Fig. 2(b). The current increases and decreases periodically, reflecting the I_d–V_{gs} characteristics of the discrete SET. More than six peaks are obtained. Since the period of the peaks is e/C_g, where e is a unit charge and C_g is the gate capacitance of the SET, the number of peaks can be increased by increasing C_g. For some combinations of an adjacent peak and valley, the peak-to-valley current ratio (PVCR) exceeds 2. If we connect a current source of 4.5 nA, stability points $a-f$ should appear, and multiple-valued memory operation can be expected.

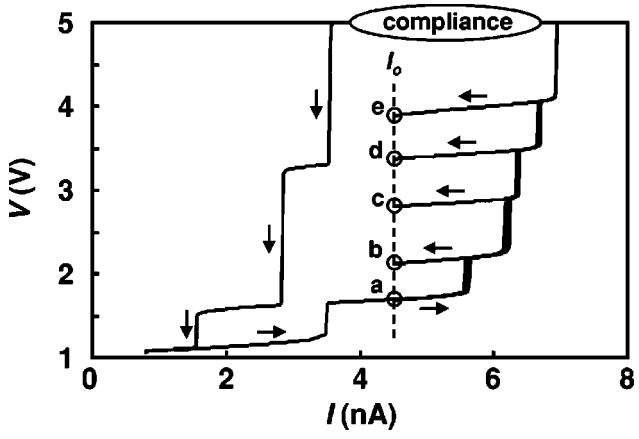

FIG. 3. Current sweep measurements of the NDR device in Fig. 2(b). The output voltage of the current source is limited by the compliance of 5 V.

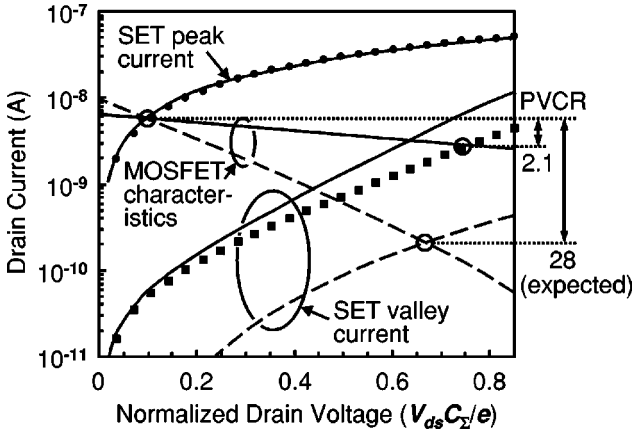

FIG. 4. Peak and valley currents of SETs as a function of drain voltage V_{ds}. Closed symbols are the measured data for the peak and valley between stability points c and d in Fig. 2(b), and the lines are simulated data (Ref. 12). Characteristics of the MOSFET connected to the SET drain are also shown. The continuous lines are fitted to the measured data, and the dashed lines correspond to the case where C_Σ is reduced by a factor of 5 and the tunneling resistance is increased by the same amount while keeping the other parameters constant.

The memory operation was confirmed by the current sweep measurements shown in Fig. 3. If the current starts from stability point a and increases, the voltage jumps when the current exceeds the second peak in the $I-V$ characteristics [Fig. 2(b)]. If the current sweep is reversed at this moment, stability point b can be reached. Other stability points, $c-e$, can also be reached by choosing higher current-sweep reversal points. Note that stability point f cannot be attained by this current-mode operation, because the last peak in the $I-V$ characteristics [Fig. 2(b)] is lower than the previous one. Direct access to any stability points can be made by the voltage-mode operation exemplified in RTD memory devices.[6]

Since the PVCR is one of the major parameters for NDR devices, we analyzed the present state and sought improvement by simulation.[12] Figure 4 shows the peak and valley currents of SETs as a function of drain voltage V_{ds}. Closed symbols are the measured data for the peak and valley between stability points c and d, and the lines are simulated data. Characteristics of the MOSFET connected to the SET drain are also shown, taking into consideration that the MOSFET gate-to-source voltage is given by $V_{gg}-V_{ds}$. The points of intersection indicated by circles are the peak and valley conditions for the combined SET-MOSFET device. Currently a PVCR of 2.1 is attained, and this can be further increased by reducing the SET valley current and/or increasing the slope of the MOSFET characteristics. The former can be attained by reducing temperature T, reducing C_Σ, or increasing tunneling resistance R_T, and the latter by reducing C_Σ or MOSFET subthreshold slope S. The dashed lines in Fig. 4 correspond to the case where C_Σ is reduced by a factor of 5 and R_T is increased by the same amount while keeping other parameters such as T and S constant. A PVCR as high as 28 can be expected as the result of this moderate scaling.

Room-temperature operation is also considered. If C_Σ and R_T are further scaled by a factor of 3, almost the same PVCR of 20 can be expected at 300 K. Note that the reduction of C_Σ is very effective in maintaining the PVCR, since

it reduces the effective temperature $2k_BTC_\Sigma/e^2$ and also increases the slope of the MOSFET characteristics in Fig. 4. This is the reason why scaling by a factor of 3 is sufficient, although room temperature is one order of magnitude higher than the present measurement temperature. Also note that the assumed S of 60 mV/dec is still attainable at room temperature if a MOSFET structure with a dominant gate capacitor is adopted.

In conclusion, we have devised a multipeak NDR device consisting of a SET and a MOSFET and verified the characteristics with devices fabricated on the same SOI wafer. Six current peaks and a PVCR of 2.1 were obtained at 27 K, and multiple-valued memory operation was confirmed with a constant current load. Simulation showed that the PVCR can be increased to 28 by moderate area scaling by a factor of 5, and nearly the same PVCR can be attained at room temperature by additional scaling by a factor of 3. The results open up the possibility of achieving multiple-valued functions in integrated silicon devices.

The authors thank Dr. Yukinori Ono for helpful discussions and for technical advice on the electrical measurements.

[1] T. A. Fulton and G. J. Dolan, Phys. Rev. Lett. **59**, 109 (1987).
[2] J. R. Tucker, J. Appl. Phys. **72**, 4399 (1992).
[3] M. A. Kastner, Rev. Mod. Phys. **64**, 849 (1992).
[4] H. Sunamura, T. Sakamoto, Y. Nakamura, H. Kawaura, J. S. Tsai, and T. Baba, Appl. Phys. Lett. **74**, 3555 (1999).
[5] S. J. Ahn and D. M. Kim, Electron. Lett. **34**, 172 (1998).
[6] A. C. Seabaugh, Y.-C. Kuo, and H.-T. Yuan, IEEE Electron Device Lett. **13**, 479 (1992).
[7] T. Waho and M. Yamamoto, Proceedings of the 27th International Symposium on Multiple-Valued Logic 35, 1997.
[8] L. Micheel, Proceedings of the 22nd International Symposium on Multiple-Valued Logic 18, 1992.
[9] Y. Takahashi, M. Nagase, H. Namatsu, K. Kurihara, K. Iwadate, Y. Nakajima, S. Horiguchi, K. Murase, and M. Tabe, Electron. Lett. **31**, 136 (1995).
[10] Y. Takahashi, H. Namatsu, K. Kurihara, K. Iwadate, M. Nagase, and K. Murase, IEEE Trans. Electron Devices **43**, 1213 (1996).
[11] A. Fujiwara, Y. Takahashi, H. Namatsu, K. Kurihara, and K. Murase, Jpn. J. Appl. Phys., Part 1 **37**, 3257 (1998).
[12] C. Wasshuber, H. Kosina, and S. Selberherr, IEEE Trans. Comput.-Aided Des. **16**, 937 (1997).