A Compact Analytical Model for Asymmetric Single-Electron Tunneling Transistors

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***Abstract*—Analytical model for asymmetric single-electron tunneling transistors (SETTs), in which resistance and capacitance parameters of source/drain junctions are not equal, has been developed. The model is based on the steady-state master equation, takes only the two most-probable charging states into account, and is therefore very simple. Even so, it can accurately reproduce the peculiar behaviors of an asymmetric SETT, such as the skew in the drain current-gate voltage characteristics and the Coulomb staircase in the drain current-drain voltage characteristic. Analytical expressions for the charge in the Coulomb island and the capacitance components of the SETT are also derived according to the same scheme, and it is demonstrated that the model can precisely describe the various aspects of the SETT behavior.**

***Index Terms*—Asymmetric SETT, compact modeling, Coulomb staircase, input capacitance, master equation, single-electron tunneling transistor (SETT).**

I. Introduction

SINGLE-ELECTRON tunneling transistor (SETT) [1]–[3] is a very promising device since it can work in smaller dimensions and with less power consumption. It also has unique characteristics such as periodic increase and decrease of drain current with respect to gate voltage, and staircase-like increase of drain current as a function of drain voltage. Such characteristics lead to higher functionality with a smaller number of circuit elements [4]–[7]. To take full advantage of the unique features of the SETT in practical applications, analysis of its behavior in circuits is important; therefore, simple and accurate modeling is highly desired. Numerical simulators [8]–[11] could be used for this purpose and are more accurate for extreme operating conditions. However, they are not simple, and are not suitable for analyzing large-scale circuits or attaining a clear insight into the device behavior. In contrast, analytical models are superior in terms of simplicity, but the models developed so far [12]–[16] lack accuracy or have substantial limitations. Some early models [12], [13] are only applicable to small drain biases or low temperatures. One proposed by Uchida *et al.* [16] can be used over a wide range of drain voltage and temperature, but cannot handle the asymmetric cases, i.e., when source and drain tunneling resistances are different. One model proposed by Wang and Porod [15] covers the asymmetric case, but it is inaccurate in the middle of Coulomb blockade (CB) region, so an "interpolation procedure" must be used to compensate this inaccuracy. The macro model by Yu *et al.* [14] does not have a physical basis and has to be calibrated by real devices or other simulators.

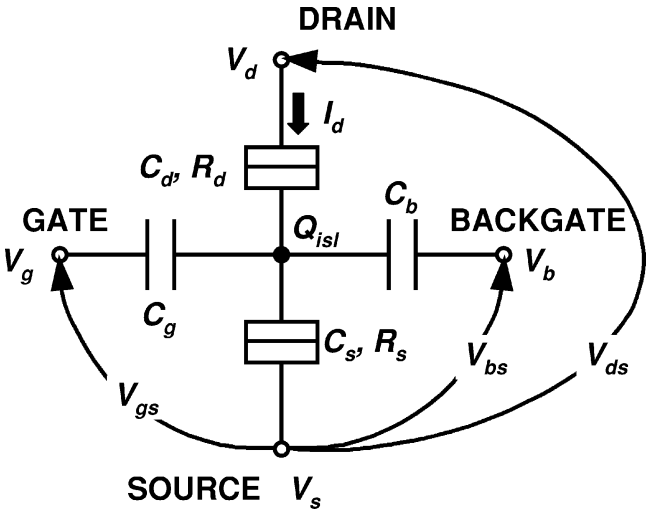

Fig. 1. Schematic diagram of a single-electron tunneling transistor (SETT). In this study, asymmetric SETT, in which tunneling resistances $(R_d,\ R_s)$ and capacitances $(C_d,\ C_s)$ on the drain and source sides are not equal, is newly modeled.

To overcome the above-mentioned drawbacks, in the current study, we have extended the applicable range of the analytical models while keeping their simplicity. This new model can precisely express a SETT with asymmetric source/drain tunneling resistances over a wide range of drain voltage and temperature. As a result, the skew in drain current (I_d) versus gate-to-source voltage (V_{gs}) characteristics and the Coulomb staircase [1]–[3] in I_d versus drain-to-source voltage (V_{ds}) characteristics can be accurately reproduced for the first time. The same simple scheme is used to derive expressions for charges in the Coulomb island and capacitance components.

II. Asymmetric SETT Model

A. Current Model

Fig. 1 shows a schematic diagram of a SETT. The Coulomb island and the source/drain leads are assumed to be metallic. Source/drain tunneling resistances R_s/R_d may be asymmetric in this model, as long as they are larger than the resistance quantum, h/e^2 about 25.8 kΩ. Capacitance parameters may take arbitrary values. The backgate is not essential, but is practically important because it can be used to adjust the "phase" of $I_d - V_{gs}$ oscillation or used as the second gate of a two-input SETT [4]. In order that the SETT can be regarded as an independent circuit element, the source/drain terminal should be driven

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by a constant-voltage source or connected to a large reservoir whose capacitance is larger than the total capacitance $C_\Sigma\,(=C_g+C_b+C_s+C_d)$ of the SETT.

The model is based on the steady-state master equation [1]. For a given bias condition, only the two most-probable charging states of the Coulomb island are considered [16]. Under such an assumption, the equation becomes

$$(\Gamma_{s,n+1,n}+\Gamma_{d,n+1,n})P_n-(\Gamma_{s,n,n+1}+\Gamma_{d,n,n+1})P_{n+1}=0 \quad (1)$$

where P_n and P_{n+1} are the probabilities that the numbers of electrons in the island are n and $n+1$, respectively, $\Gamma_{s,n,n+1}$ and $\Gamma_{s,n+1,n}$ are the tunneling rates at the source junction for a decreasing number of electrons from $n+1$ to n and an increasing number of electrons from n to $n+1$, respectively, and $\Gamma_{d,n,n+1}$ and $\Gamma_{d,n+1,n}$ are the corresponding tunneling rates at the drain junction. Considering that $P_n+P_{n+1}=1$, drain current I_n can be expressed as

$$I_n=e\frac{\Gamma_{d,n,n+1}\Gamma_{s,n+1,n}-\Gamma_{d,n+1,n}\Gamma_{s,n,n+1}}{\Gamma_{s,n,n+1}+\Gamma_{s,n+1,n}+\Gamma_{d,n,n+1}+\Gamma_{d,n+1,n}}. \quad (2)$$

The tunneling rates are given by the orthodox theory [1] as functions of terminal voltages, and the terms can be neatly rearranged by using the newly introduced asymmetry factor $r=(R_d-R_s)/(R_d+R_s)$ and the hyperbolic sine function

$$I_n=\frac{e}{4C_\Sigma R_T}\frac{(1-r^2)\left(\tilde{V}_{gs}^2-\tilde{V}_{ds}^2\right)\sinh\left(\frac{\tilde{V}_{ds}}{\tilde{T}}\right)}{A} \quad (3)$$

$$A=\left\{\tilde{V}_{gs}\sinh\left(\frac{\tilde{V}_{gs}}{\tilde{T}}\right)-\tilde{V}_{ds}\sinh\left(\frac{\tilde{V}_{ds}}{\tilde{T}}\right)\right\}+r\left\{\tilde{V}_{ds}\sinh\left(\frac{\tilde{V}_{gs}}{\tilde{T}}\right)-\tilde{V}_{gs}\sinh\left(\frac{\tilde{V}_{ds}}{\tilde{T}}\right)\right\} \quad (4)$$

$$\tilde{V}_{gs}=\frac{2C_gV_{gs}}{e}+\frac{2C_bV_{bs}}{e}-\frac{(C_g+C_b+C_s-C_d)V_{ds}}{e}-2n-1. \quad (5)$$

Here, $\tilde{V}_{ds}$ is the normalized drain-to-source voltage, $C_\Sigma V_{ds}/e$, $\tilde{T}$ is the normalized temperature, $k_BT/(e^2/2C_\Sigma)$, and R_T is the harmonic mean of the tunneling resistances, $2R_dR_s/(R_d+R_s)$. Only the term $(1-r^2)$ in (3) and the terms following r in (4) are added to express the asymmetry of the SETT; thus, the analytical approach is still simple.

I_n as a function of $\tilde{V}_{gs}$ exhibits bell-shape characteristics with quasi-exponential decays on both sides, and can represent only one peak. It is also inaccurate in the CB regions on both sides of $\tilde{V}_{gs}$ where there are one dominant charging state and two almost-equally minor states that determine the leakage current. Summation of I_n's for different n's in the relevant gate-voltage range makes the drain current periodically oscillate [16], and simultaneously compensates the inaccuracy caused by the insufficient number of charging states considered in the model.

Fig. 2 shows the I_d-V_{gs} characteristics of the SETTs with different degrees of asymmetry in tunneling resistance. The lines are calculated according to the model and the symbols are calculated by the Monte Carlo simulator SIMON [10]. Skew of the current peaks to the low-V_{gs} side for $R_d\gg R_s$ and vice versa are described well by the model, and there is virtually no difference between the results of the model and the reference simulator.

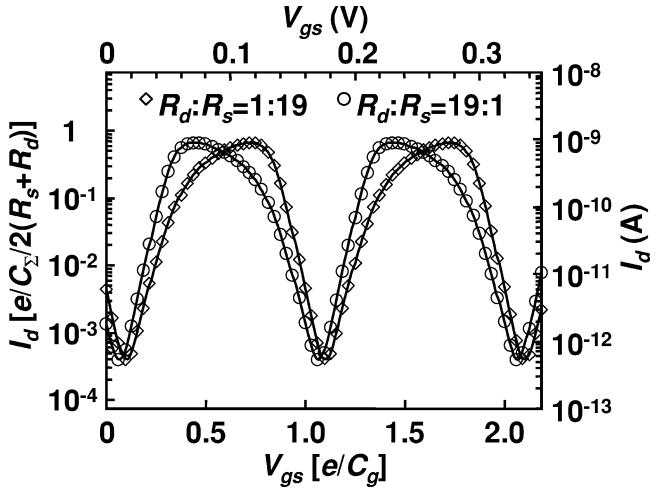

Fig. 2. I_d-V_{gs} characteristics of asymmetric SETTs calculated by the model (lines) and the reference simulator (symbols) for R_d/R_s of 1 MΩ/19 MΩ (open diamonds) and 19 MΩ/1 MΩ (open circles). Other parameters are $C_d=C_s=C_g=1$ aF, $C_b=0$, $V_{ds}=26.7$ mV ($\tilde{V}_{ds}=0.5$), and $T=18.6$ K ($\tilde{T}=0.06$).

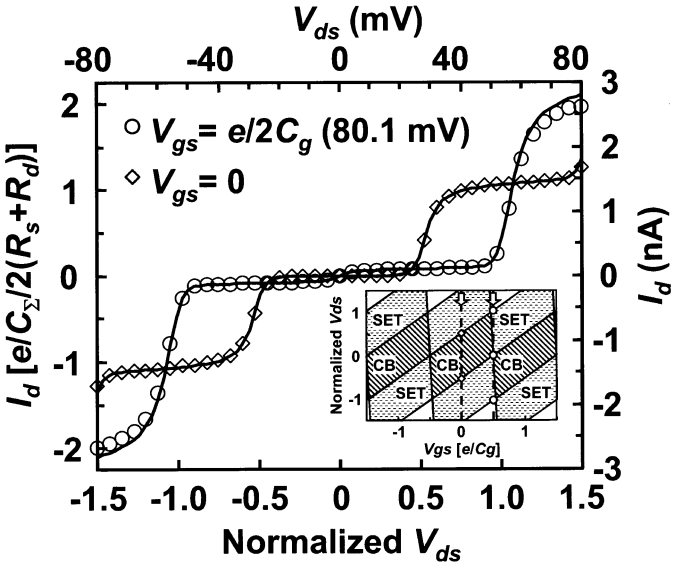

Fig. 3. Coulomb staircase (I_d-V_{ds} characteristics) of an asymmetric SETT calculated by the model (lines) and the reference simulator (symbols) for $V_{gs}=0$ (open diamonds) and $V_{gs}=e/2C_g$ (80.1 mV) (open circles). Other parameters are $R_d=1$ MΩ, $R_s=19$ MΩ, $C_d=0.1$ aF, $C_s=1.9$ aF, $C_g=1$ aF, $C_b=0$, and $T=18.6$ K ($\tilde{T}=0.06$). Sweep paths (dashed lines pointed by open arrows) in the $V_{ds}-V_{gs}$ space with Coulomb blockade (CB) regions and single-electron tunneling (SET) regions are shown in the inset. Note that both capacitance and resistance of the source/drain tunnel junction are made asymmetric to attain Coulomb staircase characteristics. In other examples of asymmetric SETT characteristics, only the resistance is made asymmetric.

Fig. 3 reproduces the Coulomb staircase, which is peculiar to asymmetric SETTs, for different gate biases. For $V_{gs}=0$, V_{ds} starts from the CB region and increases (or decreases) through the single-electron tunneling (SET) region, as shown in the inset. For $V_{gs}=e/2C_g$, V_{ds} increases (or decreases) through the SET region close to the SET-CB boundary and then goes out of the SET region. The results calculated according to the model coincide well with the simulated ones, at least

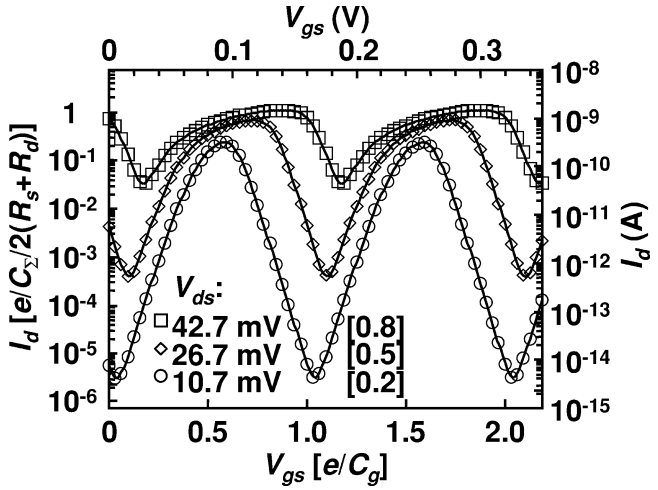

Fig. 4. $I_d - V_{gs}$ characteristics of asymmetric SETTs calculated according to the model (lines) and the reference simulator (symbols) for various drain voltages. Values in square brackets are normalized drain voltages $\tilde{V}_{ds}$. Other parameters are $R_d = 1\,\mathrm{M\Omega}$, $R_s = 19\,\mathrm{M\Omega}$, $C_d = C_s = C_g = 1\,\mathrm{aF}$, $C_b = 0$, and $T = 18.6\,\mathrm{K}$ ($\tilde{T} = 0.06$).

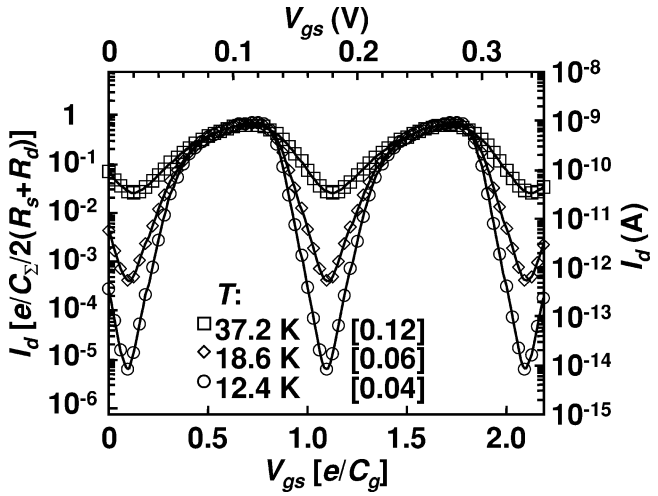

Fig. 5. $I_d - V_{gs}$ characteristics of asymmetric SETTs calculated by the model (lines) and the reference simulator (symbols) for various temperatures. Values in square brackets are normalized temperature $\tilde{T}$. Other parameters are $R_d = 1\,\mathrm{M\Omega}$, $R_s = 19\,\mathrm{M\Omega}$, $C_d = C_s = C_g = 1\,\mathrm{aF}$, $C_b = 0$, and $V_{ds} = 26.7\,\mathrm{mV}$ ($\tilde{V}_{ds} = 0.5$).

in the CB and SET regions, as can be expected under the two-charging-state assumption.

B. Accuracy

Accuracy of the current model was evaluated over a wide range of drain voltage and temperature. Fig. 4 shows the $I_d - V_{gs}$ characteristics of an asymmetric SETT for various drain voltages. Matching between the model and the reference simulator is excellent over the entire range of the gate voltage, including the peak and valley portions, even at the highest drain voltage $\tilde{V}_{ds}$ of 0.8. Fig. 5 shows the $I_d - V_{gs}$ characteristics at various temperatures. No discrepancies are evident at temperature $\tilde{T}$ up to 0.12.

Fig. 6 shows the percentage deviations of the modeled drain current from the simulated one as a function of normalized drain voltage $\tilde{V}_{ds}$ for asymmetric and symmetric cases. The results for $V_{gs} = 0$ correspond to the V_{ds} sweep starting from the current valley in the $I_d - V_{gs}$ characteristics, and those for $V_{gs} = e/2C_g$ correspond to the sweep from the current peak. The deviation is quite small, and the difference between the asymmetric and symmetric cases is not conspicuous until $\tilde{V}_{ds}$ exceeds 1.3. Above that point, the deviation for the asymmetric SETT for $V_{gs} = e/2C_g$ rises more rapidly than that for the symmetric one. The threshold $\tilde{V}_{ds}$ of about 1.3 is probably related to the thermally diffused boundary of the SET region at $\tilde{V}_{ds}$ of 1.5 for both $V_{gs} = 0$ and $e/2C_g$.

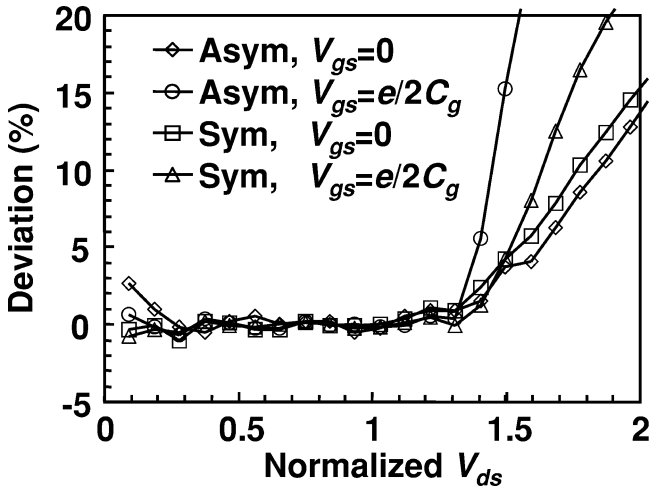

Fig. 6. Deviation of the modeled drain current from the simulated one as a function of normalized drain voltage $\tilde{V}_{ds}$ for asymmetric ($R_d = 1\,\mathrm{M\Omega}$, $R_s = 19\,\mathrm{M\Omega}$) and symmetric ($R_d = 10\,\mathrm{M\Omega}$, $R_s = 10\,\mathrm{M\Omega}$) cases. $V_{gs} = 0$ corresponds to the V_{ds} sweep starting from the current valley in $I_d - V_{gs}$ characteristics, and $V_{gs} = e/2C_g$ corresponds to the sweep from the current peak. Other parameters are $C_d = C_s = C_g = 1\,\mathrm{aF}$, $C_b = 0$, and $T = 18.6\,\mathrm{K}$ ($\tilde{T} = 0.06$).

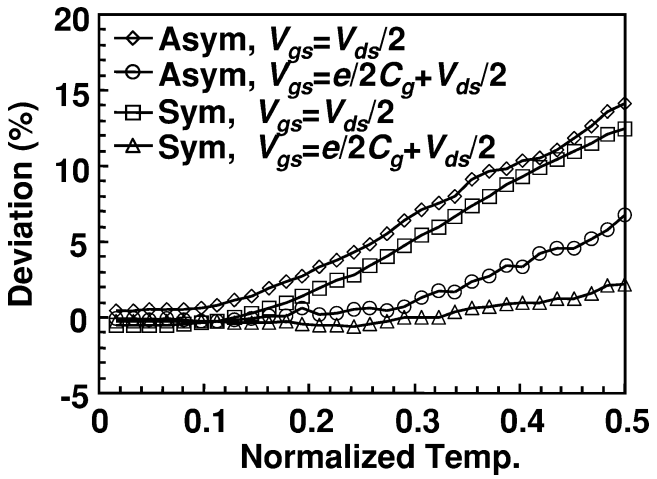

Fig. 7. Deviation of the modeled drain current from that of the reference simulator as a function of normalized temperature $\tilde{T}$ for asymmetric ($R_d = 1\,\mathrm{M\Omega}$, $R_s = 19\,\mathrm{M\Omega}$) and symmetric ($R_d = 10\,\mathrm{M\Omega}$, $R_s = 10\,\mathrm{M\Omega}$) cases. $V_{gs} = V_{ds}/2$ corresponds to the current valley in $I_d - V_{gs}$ characteristics and $V_{gs} = e/2C_g + V_{ds}/2$ does to the current peak. Other parameters are $C_d = C_s = C_g = 1\,\mathrm{aF}$, $C_b = 0$, and $V_{ds} = 26.7\,\mathrm{mV}$ ($\tilde{V}_{ds} = 0.5$).

Fig. 7 shows the deviation as a function of the normalized temperature $\tilde{T}$. The results for $V_{gs} = V_{ds}/2$ nearly correspond to the current valley in the $I_d - V_{gs}$ characteristics and those for $V_{gs} = e/2C_g + V_{ds}/2$ correspond to the current peak. In contrast to the drain voltage dependence in Fig. 6, there is no clear threshold of degradation, but the deviation is small as long

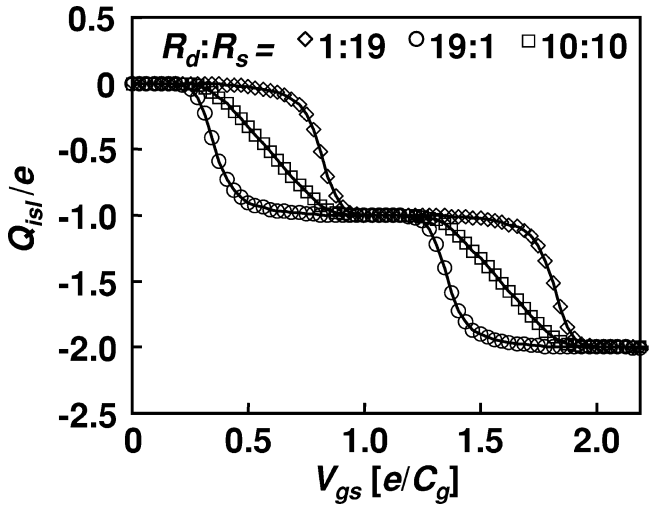

Fig. 8. Averaged charge in the Coulomb island Q_{isl} as a function of gate voltage V_{gs} calculated by the model (lines) and the reference simulator (symbols) for R_d/R_s of 1 MΩ/19 MΩ (open diamonds), 19 MΩ/1 MΩ (open circles), and 10 MΩ/10 MΩ (open squares). Other parameters are the same as those for Fig. 2 [$C_d = C_s = C_g = 1$ aF, $C_b = 0$, $V_{ds} = 26.7$ mV ($\tilde{V}_{ds} = 0.5$), and $T = 18.6$ K ($\tilde{T} = 0.06$)].

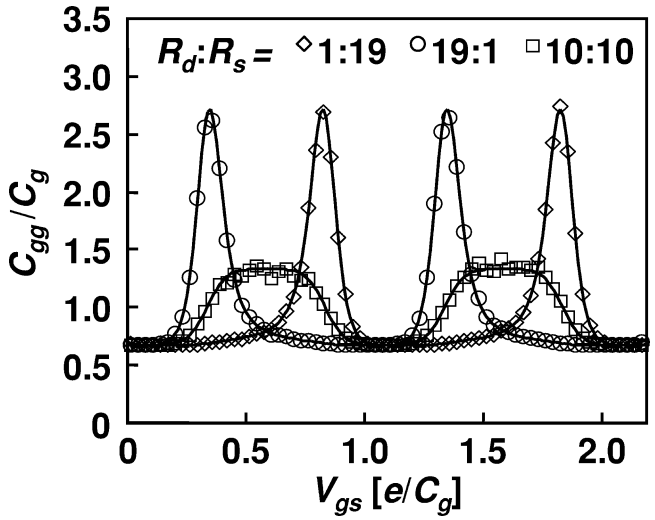

Fig. 9. SETT input capacitance C_{gg} as a function of gate voltage V_{gs} calculated by the model (lines) and the reference simulator (symbols) for R_d/R_s of 1 MΩ/19 MΩ (open diamonds), 19 MΩ/1 MΩ (open circles), and 10 MΩ/10 MΩ (open squares). Other parameters are the same as those for Figs. 2 and 8. According to [17], the charge sensitivity of the SETT electrometer is proportional to C_{gg} multiplied by absolute transconductance $|\mathrm{d}I_d/\mathrm{d}V_{gs}|$. The data shown in this figure and Fig. 2 indicate that higher sensitivity in the asymmetric case.

as $\tilde{T}$ is less than 0.1. The deviation for the asymmetric SETT at $V_{gs} = e/2C_g + V_{ds}/2$ rises rapidly compared to the symmetric case, but the difference is still smaller than that caused by the gate bias. Both in Figs. 6 and 7, the difference caused by the asymmetry is small in the middle of the CB region, i.e., at $V_{gs} = 0$ and $V_{gs} = V_{ds}/2$, respectively. This is probably due to the fact that there is one dominant charging state in the CB region regardless of the asymmetry.

C. Extension to Charge and Capacitance Models

Since the model considers only the two most-probable charging states and the probabilities of taking these states, P_n and P_{n+1}, are already known, the averaged charge in the Coulomb island Q_{isl} can easily be derived as follows:

$$\begin{aligned} Q_{isl} &= -e\{nP_n + (n+1)P_{n+1}\} \\ &= -\frac{e}{2}\left(2n+1+\frac{(\tilde{V}_{gs}+r\tilde{V}_{ds})B}{A}\right) \end{aligned} \tag{6}$$

$$B = \cosh\left(\frac{\tilde{V}_{gs}}{\tilde{T}}\right) - \cosh\left(\frac{\tilde{V}_{ds}}{\tilde{T}}\right). \tag{7}$$

Fig. 8 shows the $Q_{isl} - V_{gs}$ characteristics of the SETTs with different asymmetries in tunneling resistance. As in Figs. 2–5, the lines and symbols correspond to the results calculated by the model and the reference simulator, respectively, and both match quite well. Values of Q_{isl} for asymmetric SETTs change more abruptly to take imbalance charging states, i.e., large P_{n+1} in the large-R_d case and large P_n in the large-R_s case, in the common single-electron tunneling region.

Since the charge in the island is known, the capacitance components of the SETT can be derived. In the following, input capacitance C_{gg} is taken as an example, which is an important parameter for the charge-sensitive electrometer [17].

$$C_{gg} = \frac{C_g}{C_\Sigma}\left[C_b + C_d + C_s + C_g\left\{\frac{B}{A} + \frac{(\tilde{V}_{gs}+r\tilde{V}_{ds})\sinh\left(\frac{\tilde{V}_{gs}}{\tilde{T}}\right)}{A\tilde{T}} - B(\tilde{V}_{gs}+r\tilde{V}_{ds}) \times \frac{\left(\sinh\left(\frac{\tilde{V}_{gs}}{\tilde{T}}\right) + \frac{\tilde{V}_{gs}\cosh\left(\frac{\tilde{V}_{gs}}{\tilde{T}}\right)}{\tilde{T}} + r\left(\frac{\tilde{V}_{ds}\cosh\left(\frac{\tilde{V}_{gs}}{\tilde{T}}\right)}{\tilde{T}} - \sinh\left(\frac{\tilde{V}_{ds}}{\tilde{T}}\right)\right)\right)}{A^2}\right\}\right]. \tag{8}$$

The $C_b + C_d + C_s$ term in square brackets is the passive components that can be observed in an ordinary capacitor network, and the others are active ones caused by the SETT operation. Fig. 9 shows the C_{gg} corresponding to the cases in Fig. 8. The model well describes the peculiar behavior of asymmetric SETTs, i.e., the sharp and high peaks in $C_{gg} - V_{gs}$ characteristics. The increased peak values in C_{gg} in Fig. 9, along with the increased absolute transconductances (the slopes in Fig. 2), result in charge sensitivities much larger than that of the symmetric one.

III. Discussion

A. Applicable Temperature and Drain-Voltage Ranges

Since the model considers only two major charging states, increased probability of taking other states, which is caused by high temperature and/or high drain biases, results in errors. According to Figs. 6 and 7, which describe the difference between symmetric and asymmetric cases, and the argument by Uchida *et al.* [16] about the accuracy in the symmetric case, we can say that the error of the model is less than 5% in the range of $\tilde{V}_{ds} < 1$ and $\tilde{T} < 0.1$, because the asymmetry does not affect much in this range. Note

that this range of drain voltage and temperature covers the practical operating conditions of SETT circuits, which are determined by the margin and the error rate of the circuit operation [18], [19]. It is also obvious that the on-off ratio of the SETT drain current almost vanishes beyond this range, and useful circuit operation cannot be expected (see Figs. 4 and 5).

B. Transient Analysis

Strictly speaking, as the model is based on the steady-state master equation, it cannot be used in transient analysis. However, the assumption for making the SETT an independent circuit element, i.e., the source/drain terminal is connected to a reservoir whose capacitance is much larger than C_Σ, automatically creates a quasisteady-state condition and validates the "transient" analysis. In fact, Amakawa *et al.* built a steady-state master equation in the SPICE circuit simulator [20], and found that the error in the gate delay time, relative to the result from the time-dependent master equation or the Monte Carlo method, is less than 7% when the load capacitance is $32C_\Sigma$. Although more detailed analysis is necessary, we believe that the full-scale time-dependent analysis is an overkill for most circuit applications.

C. Co-Tunneling

Co-tunneling has not been considered so far, but is noticeable in the CB region at low temperature or when tunneling resistances are low. The expression for the inelastic co-tunneling current I_{in} [21], which is practically more important than the elastic one, is rewritten below by using the common parameters given in this paper,$\tilde{V}_{gs}$, $\tilde{V}_{ds}$, and $\tilde{T}$.

$$I_{in} = \frac{4\hbar}{3\pi e R_s R_d C_\Sigma}\left\{\frac{1-\tilde{V}_{ds}}{(\tilde{V}_{gs}+\tilde{V}_{ds})(\tilde{V}_{gs}-\tilde{V}_{ds}+2)}\right\}^2 \times\left\{\tilde{V}_{ds}^2+(\pi\tilde{T})^2\right\}\tilde{V}_{ds}. \tag{9}$$

However, the applicable ranges of $\tilde{V}_{ds}$ and $\tilde{V}_{gs}$ in (9) do not match those in (3). For example, $\tilde{V}_{ds}$ should be much smaller than one. Furthermore, to avoid the divergence of (9), it is safe to fix the $\tilde{V}_{gs}$ at minus one, where I_{in} is the smallest but is noticeable due to the small ordinary SETT current. This will secure a minimum compensation for the co-tunneling. The resulting equation is

$$I_{in} = \frac{4\hbar}{3\pi e R_s R_d C_\Sigma}\frac{\left\{\tilde{V}_{ds}^2+(\pi\tilde{T})^2\right\}\tilde{V}_{ds}}{(1-\tilde{V}_{ds})^2}. \tag{10}$$

Addition of I_{in} to the ordinary SETT current in (3) provides a simple correction to the present model.

IV. Conclusions

A compact analytical model for asymmetric SETTs was devised based on the steady-state master equation and the two-charging-state assumption. The skew in the I_d-V_{gs} characteristics and the Coulomb staircase in $I_d - V_{ds}$, which are peculiar to asymmetric SETTs, were successfully expressed by the model. Comparison with a Monte Carlo simulator revealed that the error in the modeled drain current is not much affected by the asymmetry; it is below 5% when $\tilde{V}_{ds}$ and $\tilde{T}$ are less than 1 and 0.1, respectively. According to the same scheme of the master equation and the assumption, the averaged charge in the Coulomb island and the capacitance components were also modeled. It was demonstrated by the model that asymmetric SETTs show steeper change in the island charge with respect to the gate voltage and higher peaks of the input capacitance. The versatility, simplicity and accuracy of the proposed model make it useful for large-scale circuit simulations and enable straightforward understanding of the device behavior.

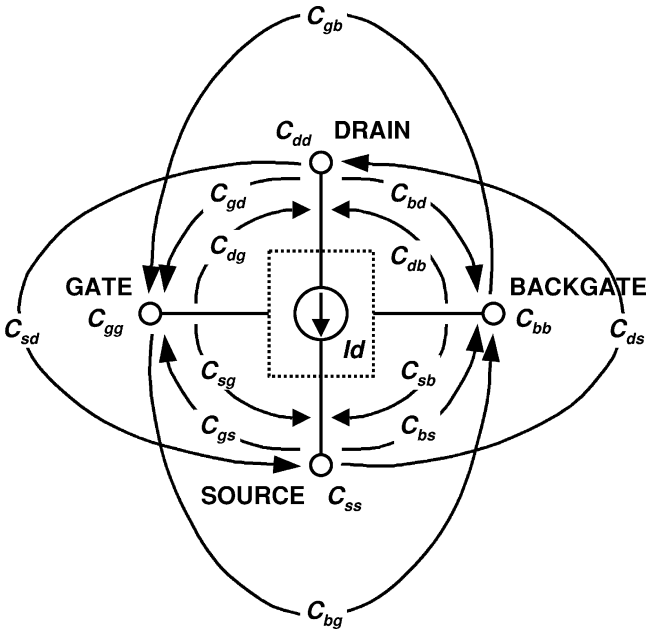

Fig. 10. Schematic diagram of capacitance components in a SETT.

Appendix

Definition and Derivation of Capacitance Components

As shown in Fig. 10, there are 16 capacitance components in a SETT with a backgate. They are defined as

$$C_{ij} = -\partial Q_i/\partial V_j \quad \text{for } i \neq j \tag{A1}$$

and

$$C_{ii} = \partial Q_i/\partial V_i, \tag{A2}$$

where V_i is the terminal voltage, and Q_i is the charge induced on the terminal side of the capacitor, C_g, C_b, C_s or C_d. In the present model, it is sufficient to derive the four components related to the gate, C_{gg}, C_{gd}, C_{gs}, and C_{gb}, because the source/drain terminal is to be connected to a large reservoir, and the components related to the backgate, C_{bb}, C_{bg}, C_{bd} and C_{bs}, can easily be obtained by interchanging the gate and the backgate.

For charge conservation

$$C_g(V_g - V_{isl}) + C_b(V_b - V_{isl}) + C_s(V_s - V_{isl}) + C_d(V_d - V_{isl}) + Q_{isl} = 0 \tag{A3}$$

should be satisfied, where V_{isl} is the potential of the Coulomb island. This can be rewritten as

$$V_{isl} = \frac{(C_g V_g + C_b V_b + C_s V_s + C_d V_d + Q_{isl})}{C_\Sigma}. \tag{A4}$$

If the potentials are considered relative to the source potential, then C_{gg} can be expressed as

$$C_{gg} = C_g \frac{\partial}{\partial V_{gs}}(V_{gs} - V_{isl,s}) = \frac{C_g}{C_\Sigma}\left(C_b + C_s + C_d - \frac{\partial Q_{isl}}{\partial \tilde{V}_{gs}}\frac{\partial \tilde{V}_{gs}}{\partial V_{gs}}\right) \quad \text{(A5)}$$

By combining (5), (6), and (A5), (8) for C_{gg} is obtained. In a similar manner, C_{gb}, C_{gd}, and C_{gs} are given by

$$C_{gb} = \frac{C_g}{C_\Sigma}\left(C_b + \frac{\partial Q_{isl}}{\partial \tilde{V}_{gs}}\frac{\partial \tilde{V}_{gs}}{\partial V_{bs}}\right) \quad \text{(A6)}$$

$$C_{gd} = \frac{C_g}{C_\Sigma}\left(C_d + \frac{\partial Q_{isl}}{\partial \tilde{V}_{gs}}\frac{\partial \tilde{V}_{gs}}{\partial V_{ds}} + \frac{\partial Q_{isl}}{\partial \tilde{V}_{ds}}\frac{\partial \tilde{V}_{ds}}{\partial V_{ds}}\right) \quad \text{(A7)}$$

and

$$C_{gs} = \frac{C_g}{C_\Sigma}\left\{C_s - \frac{\partial Q_{isl}}{\partial \tilde{V}_{gs}}\left(\frac{\partial \tilde{V}_{gs}}{\partial V_{bs}} + \frac{\partial \tilde{V}_{gs}}{\partial V_{gs}} + \frac{\partial \tilde{V}_{gs}}{\partial V_{ds}}\right) - \frac{\partial Q_{isl}}{\partial \tilde{V}_{ds}}\frac{\partial \tilde{V}_{ds}}{\partial V_{ds}}\right\}. \quad \text{(A8)}$$

The final results are obtained by differentiating (5) and (6), and inserting them into the above equations as

$$C_{gb} = \frac{C_g}{C_\Sigma}\left[C_b - C_b\left\{\frac{B}{A} + \frac{(\tilde{V}_{gs}+r\tilde{V}_{ds})\sinh\left(\frac{\tilde{V}_{gs}}{\tilde{T}}\right)}{A\tilde{T}} - B(\tilde{V}_{gs}+r\tilde{V}_{ds}) \times \frac{\left(\sinh\left(\frac{\tilde{V}_{gs}}{\tilde{T}}\right) + \frac{\tilde{V}_{gs}\cosh\left(\frac{\tilde{V}_{gs}}{\tilde{T}}\right)}{\tilde{T}} + r\left(\frac{\tilde{V}_{ds}\cosh\left(\frac{\tilde{V}_{gs}}{\tilde{T}}\right)}{\tilde{T}} - \sinh\left(\frac{\tilde{V}_{ds}}{\tilde{T}}\right)\right)\right)}{A^2}\right\}\right] \quad \text{(A9)}$$

$$C_{gd} = \frac{C_g}{C_\Sigma}\left[C_d - \frac{C_\Sigma}{2}\left\{\frac{rB}{A} - \frac{(\tilde{V}_{gs}+r\tilde{V}_{ds})\sinh\left(\frac{\tilde{V}_{ds}}{\tilde{T}}\right)}{A\tilde{T}} - B(\tilde{V}_{gs}+r\tilde{V}_{ds}) \times \frac{\left(-\sinh\left(\frac{\tilde{V}_{ds}}{\tilde{T}}\right) - \frac{\tilde{V}_{ds}\cosh\left(\frac{\tilde{V}_{ds}}{\tilde{T}}\right)}{\tilde{T}} + r\left(\sinh\left(\frac{\tilde{V}_{gs}}{\tilde{T}}\right) - \frac{\tilde{V}_{gs}\cosh\left(\frac{\tilde{V}_{ds}}{\tilde{T}}\right)}{\tilde{T}}\right)\right)}{A^2}\right\} + \frac{C_g+C_b+C_s-C_d}{2}\left\{\frac{B}{A} + \frac{(\tilde{V}_{gs}+r\tilde{V}_{ds})\sinh\left(\frac{\tilde{V}_{gs}}{\tilde{T}}\right)}{A\tilde{T}} - B(\tilde{V}_{gs}+r\tilde{V}_{ds}) \times \frac{\left(\sinh\left(\frac{\tilde{V}_{gs}}{\tilde{T}}\right) + \frac{\tilde{V}_{gs}\cosh\left(\frac{\tilde{V}_{gs}}{\tilde{T}}\right)}{\tilde{T}} + r\left(\frac{\tilde{V}_{ds}\cosh\left(\frac{\tilde{V}_{gs}}{\tilde{T}}\right)}{\tilde{T}} - \sinh\left(\frac{\tilde{V}_{ds}}{\tilde{T}}\right)\right)\right)}{A^2}\right\}\right] \quad \text{(A10)}$$

and

$$C_{gs} = \frac{C_g}{C_\Sigma}\left[C_s + \frac{C_\Sigma}{2}\left\{\frac{rB}{A} - \frac{(\tilde{V}_{gs}+r\tilde{V}_{ds})\sinh\left(\frac{\tilde{V}_{ds}}{\tilde{T}}\right)}{A\tilde{T}} - B(\tilde{V}_{gs}+r\tilde{V}_{ds}) \times \frac{\left(-\sinh\left(\frac{\tilde{V}_{ds}}{\tilde{T}}\right) + \frac{\tilde{V}_{ds}\cosh\left(\frac{\tilde{V}_{ds}}{\tilde{T}}\right)}{\tilde{T}} + r\left(\sinh\left(\frac{\tilde{V}_{gs}}{\tilde{T}}\right) - \frac{\tilde{V}_{gs}\cosh\left(\frac{\tilde{V}_{ds}}{\tilde{T}}\right)}{\tilde{T}}\right)\right)}{A^2}\right\} + \frac{C_g+C_b-C_s+C_d}{2}\left\{\frac{B}{A} + \frac{(\tilde{V}_{gs}+r\tilde{V}_{ds})\sinh\left(\frac{\tilde{V}_{gs}}{\tilde{T}}\right)}{A\tilde{T}} - B(\tilde{V}_{gs}+r\tilde{V}_{ds}) \times \frac{\left(\sinh\left(\frac{\tilde{V}_{gs}}{\tilde{T}}\right) + \frac{\tilde{V}_{gs}\cosh\left(\frac{\tilde{V}_{gs}}{\tilde{T}}\right)}{\tilde{T}} + r\left(\frac{\tilde{V}_{ds}\cosh\left(\frac{\tilde{V}_{gs}}{\tilde{T}}\right)}{\tilde{T}} - \sinh\left(\frac{\tilde{V}_{ds}}{\tilde{T}}\right)\right)\right)}{A^2}\right\}\right] \quad \text{(A11)}$$

Note that the relationship, $C_{gg} = C_{gd} + C_{gs} + C_{gb}$ holds as can be expected from the principle of superposition.

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