A clocked AC-DC voltage multiplier for increasing the power conversion efficiency in vibration energy harvesting

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Nomenclature

CP: charge pump, V_{IN}: AC input voltage, f: frequency of V_{IN}, N: stage number, C: capacitance of a main capacitor per stage, V_{DD}: amplitude of V_{IN}, θ_s: phase at which the output current begins to flow, I_{OUT}: output current, I_{IN}: input current, f_c: clock frequency, β: ratio of parasitic capacitance to C, V_{OUT}: output voltage, P_{IN}: input power, V_{TH}^{EFF}: effective threshold voltage of diode, V_T: thermal voltage, I_s: diode saturation current, η_{CP}: power efficiency of CP.

1. Introduction

In energy harvesting (EH), environmental energy is converted into electric power [1]. Because the power obtained by EH is generally too small to directly drive integrated circuits, it is necessary to boost the voltage using CPs [2]. However, vibration energy harvesters operate at a low frequency of 10Hz-1kHz, resulting in a low I_{OUT} from CPs. In this research, we propose a clocked AC-DC-CP to improve power conversion efficiency and to increase output power. We also derive model equations for V_{OUT} - I_{OUT} and V_{OUT} - P_{IN} characteristics.

2. Proposed Circuit and its model

In the conventional AC-DC-CP, V_{IN} is also used for CLK (Fig. 1). I_{OUT} becomes small at low frequency [3]. In the proposed circuit (Fig. 2), a higher I_{OUT} can be obtained by increasing f_c with an oscillator and buffer added on chip. Average I_{OUT} ($\overline{I_{OUT}}$) and average P_{IN} ($\overline{P_{IN}}$) are derived by calculating the sum of charges for each clock ([4],[5]) and averaging it over $1/f$ ((3),(4)).

$$(1)\ V_{TH}^{EFF} = V_T \ln\left(\frac{4^{\frac{1}{N+1}}(1+\beta)f_c C V_T}{I_s}\right)$$

$$(2)\ \theta_s = \sin^{-1}\left[\{V_{OUT} + (N+1)V_{TH}^{EFF}\}/\left\{\frac{1+\beta}{V_{DD}(1+\beta+N)}\right\}\right]$$

$$(3)\ \overline{I_{OUT}} = \frac{1}{\pi}\frac{(1+\beta)Cf_c}{N}\left[\left(\frac{N}{1+\beta}+1\right)V_{DD}\cos\theta_s - \left(\frac{\pi}{2}-\theta_s\right)\{(N+1)V_{TH}^{EFF}+V_{OUT}\}\right]$$

$$(4)\ \overline{P_{IN}} = \frac{1}{4\pi}\frac{(1+\beta)Cf_c}{N}\left\{\left(\frac{N}{1+\beta}+1\right)^2 V_{DD}^2(\pi-2\theta_s+\sin 2\theta_s) - \left(\frac{N}{1+\beta}+1\right)V_{DD}\{(N+1)V_{TH}^{EFF}+V_{OUT}\}\cos\theta_s\right\} + \frac{1}{4\pi}\left(\frac{\beta}{1+\beta}\right)f_c NCV_{DD}^2(\pi-2\theta_s+\sin 2\theta_s)$$

$$(5)\ \eta_{CP} = \overline{I_{OUT}}\times V_{OUT}/\overline{P_{IN}}$$

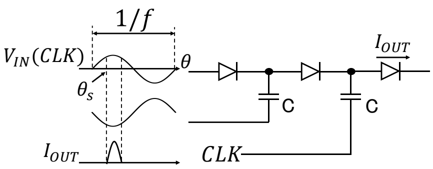

Fig. 1. Conventional AC-DC-CP

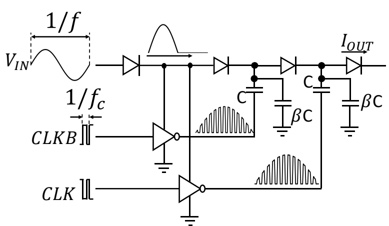

Fig. 2. Clocked AC-DC-CP

3. Result

Fig. 3 shows $\overline{I_{OUT}}$ as a function of f_c, which is normalized by $\overline{I_{OUT}}$ of the conventional CP. Furthermore, the calculated value and the SPICE simulation are compared. ROHM 0.18μm, 1.8V CMOS transistors were used for SPICE simulation. Threshold voltage of transistors were lowered to $\pm$0.2V for low voltage operation. The values of the parameters are N=10, C=10[pF], $V_{DD}=0.5$[V], β=0.05, V_{OUT}=2[V], I_s=12[nA], f=1[kHz] as a demonstrations. The model (3) is in good agreement with SPICE simulation results within an error of 5% at $f_c \leq$ 1MHz. $\overline{I_{OUT}}$ increases up to about 600 times at f_c of 20MHz. Because transistors do not run properly at $f_c >$ 30MHz, $\overline{I_{OUT}}$ starts dropping at 30MHz. Fig. 4 shows η_{CP} ratio -$\overline{I_{OUT}}$ ratio. 600x higher current is achieved with a trade-off of η_{CP} ratio of 0.6. In other words, system power conversion efficiency, $\eta_{sys} \equiv \overline{P_{OUT}}/P_{EH}$, can be increased by a factor of 600 as far as $P_{EH} > \overline{P_{IN}} + P_{OSC}$ where P_{EH} is the power generated by EH, $\overline{P_{OUT}} = \overline{I_{OUT}} \times V_{OUT}$, and P_{OSC} is power of the oscillator. Or instead, one can reduce the CP area by a factor of 600 to have the same I_{OUT} as the conventional CP.

4. Conclusion

We proposed a clocked AC-DC voltage multiplier which can obtain high I_{OUT} even with low frequency AC input. System power conversion efficiency can be increased by a factor of 600 when the input frequency of 1kHz is increased to 20MHz by the internal oscillator. We also proposed the model equations.

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5. Reference

[1] T. J. Kaźmiersuki et al., "Energy Harvesting Systems: Principles, Modeling and Applications," Chap. 1, Springer 2010.
[2] N. Tran et al., IEEE RFICS, Jun.3–5, pp. 281–284, 2007.
[3] X. Wang et al., IEEE A-SSCC, 9-3, pp. 252-255, Nov. 2007.
[4] T. Tanzawa, IEICE Trans. Fund. Elec., Vol. E100.A No.5, pp.1137-1144, 2017.
[5] T. Tanzawa, IEEE ISCAS, pp. 1358-1361,2015.

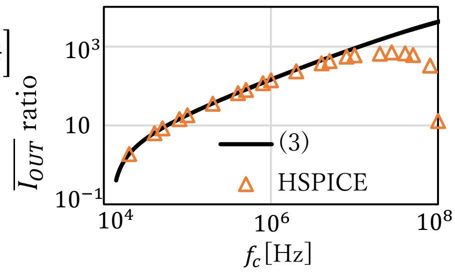

Fig. 3. f_c - $\overline{I_{OUT}}$

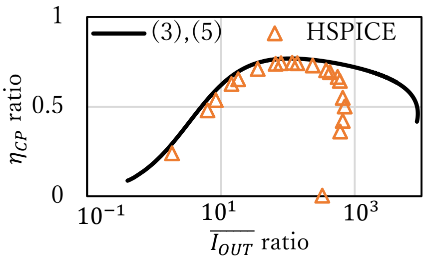

Fig. 4. $\overline{I_{OUT}}$ ratio - η_{CP} ratio