Toward a minimum-operating-voltage design of DC-DC charge pump circuits for energy harvesting

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1. Introduction In energy harvesting (EH), external energy such as solar and thermal energy is converted into electric power. Because it fluctuates depending on the input energy, the output voltage can be as low as several hundreds to several tens of mV in some cases [1]. Therefore, it is necessary to boost the voltage in order to operate integrated circuits. However, theoretical research on the lower limit of the input voltage for charge pumps (CPs) [2] has not been reported. In this research, we propose an algorithm to design circuit parameters for extremely low voltage operation.

2. Proposed design flow Parameters are defined as follows.

V_{DD}: input voltage, V_{OUT}: output voltage, I_{OUT}: average output current, *N*: number of stages, *C*: capacitance of capacitor, $\alpha_{T(B)}C$: parasitic capacitance on the upper (lower) side of capacitor, C_{ox}: capacitance density of capacitor, *f*: frequency, V_T: thermal voltage, I_S: saturation current, V_{TH}^{EFF}: effective threshold voltage of diode, A_D: area of a unit diode, N_D: number of parallel diodes, C_j: junction capacitance of a unit diode, A_{CP}: total area of CP, A_{cap}: capacitor area per stage, R_{PMP}: effective output impedance of CP, V_{MAX}: maximum attainable voltage, η: power efficiency, V_{PP}: output voltage at the operating point, I_{PP}: average value of the output current at the operating point

$I_s, A_D, C_{ox}, C_j, \alpha_B$ and V_T are assumed to be predetermined. The relationships between I_{OUT}, V_{OUT} and η are expressed by (1)-(5) [3], [4]. The size of CP is defined by (6). Because one parameter depends on another, one needs to determine each parameter in a proper order. The proposed flow is as follows when the reverse current is considered to be sufficiently small.

$$I_{OUT} = \frac{V_{MAX} - V_{OUT}}{R_{PMP}} \quad (1) \qquad R_{PMP} = \frac{N}{(1+\alpha_T)Cf} \quad (2)$$

$$V_{MAX} = \left(\frac{N}{1+\alpha_T} + 1\right)V_{DD} - (N+1)V_{TH}^{EFF} \quad (3)$$

$$V_{TH}^{EFF} = V_T ln\left(4^{\frac{1}{N+1}}\frac{(1+\alpha_T)fCV_T}{N_D I_S}\right) \quad (4)$$

$$\frac{1}{\eta} = \frac{V_{DD}}{V_{OUT}}\left[\left(\frac{N}{1+\alpha_T}+1\right) + \left(\frac{\alpha_T}{1+\alpha_T}+\alpha_B\right)\frac{fNCV_{DD}}{I_{OUT}}\right] \quad (5)$$

$$A_{CP} = C/C_{ox} \times N + N_D A_D \times (N+1) \quad (6)$$

#1: Give initial values to $V_{DD}, V_{PP}, A_{CP}, V_{TH}^{EFF}$ and N_D.
#2: Assuming $\alpha_T \ll 1$, the minimum stage number N_{min} to generate V_{PP} is determined using (3) by replacing V_{MAX} with V_{PP}. An optimum number of stages (N_{OPT}) is determined by $1.6 \times N_{min}$ [5].
#3: Calculate *C* using (6). Calculate α_T with $C_j A_D N_D / C$.
#4: Calculate *f* using (4).
#5: Calculate R_{PMP} and V_{MAX} using (2), (3)
#6: Draw $I_{OUT} - V_{OUT}$ to get I_{PP}.
#7: Calculate the required CP area (A_{tot}) for $I_{OUT}(V_{PP}) = I_{PPtgt}$ with $A_{CP} \times SF$ where $SF = I_{PPtgt}/I_{PP}$. Update C and N_D with $C_{new} = C \times SF$, $N_{D\_new} = N_D \times SF$.
#8: Calculate η using (5).

By executing steps #1 to #8 for various V_{TH}^{EFF} and N_D, one can draw $A_{tot} - \eta$ characteristics. Three designs are taken as representative ones: the design with the maximum efficiency (η_{max}), the design with the smallest area (A_{min}), and the design where power efficiency and area are balanced (*balanced*). By changing V_{DD}, one can perform the same procedure, to identify a minimum operating voltage.

3. Demonstration Demonstration is performed with the following parameters, where a Schottky barrier diode [6] and 1.8V CMOS are assumed.

$A_{CP} = 2 \times 10^4 \mu m^2, V_{PP} = 0.5V, I_{PPtgt} = 10\mu A,$
$C_{ox} = 10fF/\mu m^2, \alpha_B = 0.1, A_D = 10\mu m^2, V_T = 25mV,$
$I_S = 10nA, C_j = 3.5fF/\mu m^2,$
$V_{TH}^{EFF} = 0.02 \sim 0.08V, N_D = 1 \sim 120, V_{DD} = 0.1 \sim 0.3V$

Fig.1 (a) and (b) respectively shows $V_{DD} - A_{tot}$ and $V_{DD} - \eta$. One can design CP operating at $V_{DD} = 0.1V$ and $V_{PP} = 0.5V$ with an area overhead per 10μA of 1.99mm^2 and $\eta = 34\%$. If the Si area is the priority, one may have to run EH system at $V_{DD} = 0.2V$ with an area overhead per 10μA of 0.46mm^2 and $\eta = 46\%$ for *balanced* or 0.12mm^2 and $\eta = 24\%$ for A_{min}.

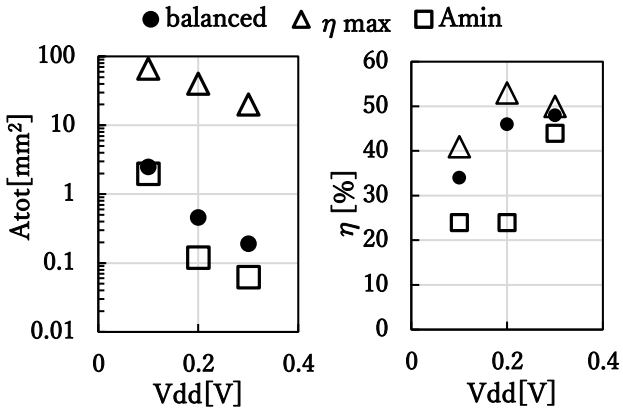

Fig.1 (a)$V_{DD} - A_{tot}$, (b)$V_{DD} - \eta$

4. Conclusion We proposed an algorithm to determine design parameters of CP under low voltage conditions and demonstrated for V_{DD} = 0.1~0.3V. By using the proposed flow under given conditions, one can easily estimate the trade-off between V_{DD}, circuit area and power efficiency.

5. References

[1] Y. Manoli, IEEE ESSCIRC, pp.27-36, Sep. 2010.
[2] J. F. Dickson, IEEE JSSC, vol.11, no.3, pp.374-378, Jun. 1976.
[3] T. Tanzawa, IEICE, Vol. E100.A, No.5, pp.1137 – 1144, 2017.
[4] T. Tanzawa, IEEE ISCAS, pp. 1358- 1361, 2015.
[5] T. Tanzawa, IEEE TPE, Vol.29, No.2 pp.534-538, 2014.
[6] N. Tran et al., IEEE RFIC, pp281-284, 2007.

This work is supported by VDEC, Synopsys, Inc., Cadence Design Systems, Inc. and Rohm Corp..