A system design of clocked AC-DC converters for vibration energy harvesting

Hayato Kawauchi and Toru Tanzawa
Shizuoka University

Nomenclature

Table. 1. Design parameters

Name	parameter (value if any)
P_{EH}	power generated by EH
P_{CP}	input power of the CP (variable)
P_{OSC}	power of the oscillator (variable)
P_{OUT}	output power (variable)
P_{total}	power of the system ($P_{CP}+P_{OSC}$)
V_{DD}	AC input voltage (the peak is 0.5V)
V_{SS}	ground (0V)
V_{REC}	rectified voltage
f_{IN}	frequency of V_{DD}(1kHz)
f_{CLK}	clock frequency (variable)
V_{OUT}	output voltage (2V)
I_{OUT}	output current (variable)
N	stage number of the CP (10)
C	capacitance per stage (10pF)
β	ratio of parasitic capacitance to C (0.05)
I_S	diode saturation current (1.2nA)

1. Introduction

In energy harvesting (EH), environmental energy is converted into electric power [1]. Because the power obtained by EH is generally too small to directly drive ICs, it is necessary to boost the voltage using charge pumps (CPs) [2]. Vibration power generation and electromagnetic waves can be environmental AC energy sources. Boosting circuits for electromagnetic waves to drive ICs have already been put into practical use. However, when the same circuits are used for the vibration EH, it is not sufficient to drive ICs because the frequency is too low (10Hz-1kHz) [3]. In the previous paper [4], we proposed a clocked AC-DC converter to reduce reactive power and demonstrated its validity. In this research, we report a system design of the clocked AC-DC converter.

2. Proposed system

In the conventional AC-DC-CP, V_{DD} is also used for CLK. I_{OUT} becomes small at low frequency [3]. In the proposed circuit, higher I_{OUT} can be obtained by increasing f_{CLK} with an on-chip oscillator [4].

A clocked AC-DC converter system is designed as shown in Fig.1, based on a 0.18 μm CMOS technology. Fig. 2 shows the simulation waveform of the system. To find an optimum f_{CLK}, P_{CP}, P_{OSC}, P_{OUT} and P_{total} are calculated as a function of f_{CLK} under the condition that the output resistance of EH is much smaller than the input resistance of the CP system.

3. Result

Fig. 3 compares calculated values of P_{CP}, P_{OSC}, P_{total}, P_{OUT} with SPICE simulation results. Calculated values are derived from the model (3) and (4) of [4]. 0.18μm, 1.8V CMOS transistors and schottky diodes were used for SPICE simulation. Threshold voltages of transistors were assumed to be as low as $\pm$0.2V for low voltage operation. The values of the design parameters are listed in Table.1. As shown in Fig. 3, when $f_{CLK} \leq$ 1MHz, calculated values are in good agreement with simulation results within an error of 8%. For $f_{CLK} \gg$ 1MHz, the error increases due to the frequency characteristic of the clock buffer. When $f_{CLK} \leq$ 10MHz, P_{osc} is about 10~25% of P_{CP}. For $f_{CLK} \geq$ 10MHz, P_{OSC} becomes a dominant factor of P_{total}. Since it is assumed that $P_{EH} > P_{total}$, it is desirable that $f_{CLK} \leq$ 10MHz under this condition. Also, P_{OUT} is maximized at $f_{CLK} =$ 10MHz, which is 190 times as large as that of the conventional CP. In other words, system power conversion efficiency, $\eta_{sys} \equiv P_{OUT}/P_{EH}$, can be increased by a factor of 190.

4. Conclusion

A clocked AC-DC system was designed and verified. System power conversion efficiency was increased by a factor of 190 when the frequency of V_{DD} of 1kHz is increased to 10MHz by an on-chip oscillator.

This work is supported by VDEC, Synopsys, Inc., Cadence Design Systems, Inc. and Rohm Corp..

5. Reference

[1] T. J. Kaźmiersuki et al., "Energy Harvesting Systems: Principles, Modeling and Applications," Chap. 1, Springer 2010
[2] N. Tran et al., IEEE RFICS, Jun.3–5, pp. 281–284, 2007.
[3] X. Wang et al., IEEE A-SSCC, 9-3, Nov. 2007.
[4] H. Kawauchi, IEICE general conf., C-12-16, Mar. 2018.

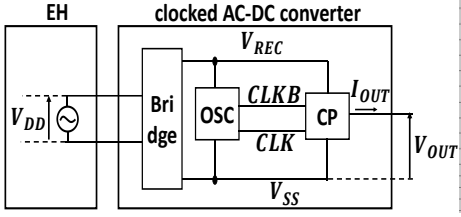

Fig. 1. Block diagram of the clocked AC-DC converter

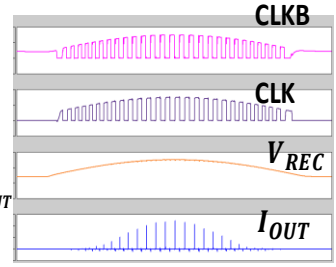

Fig. 2. Simulation waveform of the clocked AC-DC converter

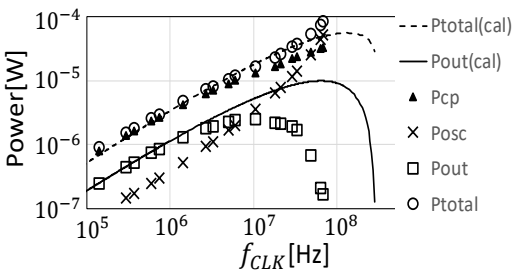

Fig. 3. f_{CLK}-Power