# Formulation of minimal delay time with pre-emphasis pulses for dense parallel RC lines

Kazuki Matsuyama and Toru Tanzawa
Shizuoka University

## 1. Introduction

Pre-emphasis pulses are used in transmission line [1], display [2] and memory [3], to reduce the wiring delay time. However, a general optimization method for the pre-emphasis pulses has not been formulated. In the previous paper [4], we reported a closed-form expression to minimize the delay time and the energy-delay product when single RC delay lines are driven by the pre-emphasis pulses (Fig. 1). In memory arrays in advanced technology, the capacitance between adjacent WLs is much more dominant than the ground capacitance [3], [5], which can be modeled as three RC delay lines as shown in Fig. 2(a). In this study, we formulated the minimum delay time of three RC delay lines driven by pre-emphasis pulse.

## 2. Formulation and verification

Parameters used for the calculation are defined as follows. $T$: pre-emphasis time, $E$: target voltage, $\alpha$: ratio of $E$ to the pre-emphasis voltage, $\beta$: error rate to $E$, $x$: delay line position ($x$=0 for the nearest, $x$=$l$ for the farthest), $r$: resistance per unit length, $c$: capacitance per unit length, $e(x,t)$: voltage at a position $x$ and a time $t$, $t_{delay\_min}$: minimal time for the slowest node voltage to reach $\beta E$. $N$: number of divisions of RC delay lines for circuit analysis, $R$: $R = rl/N$, $C$: $C = cl/N$. First we converted the circuit for simple calculation. Because of its symmetry the potential at P in Fig. 2(a) is the same as that of Q at any time when all three lines are fully discharged at t=0. As a result, Fig. 2(a) can be reduced to Fig. 2(b). Fig. 2(c) is equivalent to Fig. 2(b) when $C = C_1//C_2$ and $V_{in} = V_{in1} + V_{in2}$. At the rising edge of $V_{in}$, the potential at node R and S in Fig. 2(b) is equal to $V_{in}$ $(R/2)/(R/2+R) = 1/3V_{in}$ When one chooses $V_{in1} = 2/3V_{in}$, $V_{in2} = 1/3V_{in}$, $C_1 = 1.5C$ and $C_2 = 3C$, the intermediate node between $C_1$ and $C_2$ stay at $V_{in2}$ in any time. Therefore, Fig. 2(c) is converted to Fig. 2(d).

Thus, the original circuit model of Fig. 2(a) is simplified as an equivalent circuit model as shown in Fig. 2(d). Since Fig. 2(d) can be regarded as a single RC delay line, the calculation performed in [4] can be applied. The minimal delay condition and minimal delay time based on Fig. 2(d) are calculated to be (1) and (2), respectively,

$$T_{opt} \fallingdotseq \gamma\tau \, ln\frac{\alpha}{\alpha-1} \qquad (1)$$

$$t_{delay\_min} \fallingdotseq \gamma\frac{\tau}{9} ln\left[\frac{4\alpha}{3\pi\beta}\left(\frac{\alpha}{\alpha-1}\right)^8\right] \qquad (2)$$

where $\tau$ is a time constant given by $4rcl^2/\pi^2$ and γ is a model dependent coefficient which is 1.5 for the three RC line model and 1 for the single RC line model. One can easily determine $T_{opt}$ when α, r and c are given. Fig. 3 shows $t_{delay\_min}$ as a function of α for β=0.01 when set by (1), which is normalized by $t_{delay\_min}$ with α = 1 in case of a step pulse. (2) is in good agreement with SPICE simulation results within an error of 2% for 1.1≦α≦2. For example, by setting $\alpha$ = 2, the delay time can be reduced to 1/4.

## 3. Conclusion

We formulated a pre-emphasis pulse to reduce the RC delay time, and identified the minimal delay condition (1) and the delay time (2) for three RC delay lines as well as single RC delay lines. One can easily design pre-emphasis pulses for RC delay lines by using these equations.

## 4. References

[1] A. Fiedler, et al., ISSCC, pp. 238-9, 1997.
[2] J. Bang, et al., ISSCC, pp. 212-213, 2016.
[3] W. Jeong et al., IEEE JSSC, Vol. 51, No. 1, pp. 204-212, 2016.
[4] K. Matsuyama et al., IEICE general conf. C-12-35, Mar. 2018.
[5] T. Tanzawa et al., IEEE ASSCC, Nov. 2016.

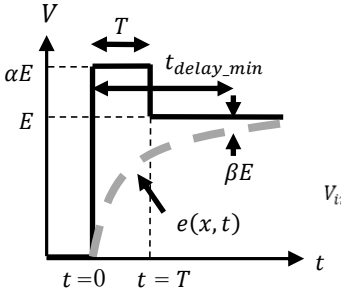

Fig. 1. Pre-emphasis

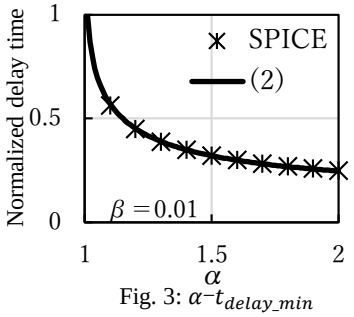

Fig. 3: $\alpha$–$t_{delay\_min}$

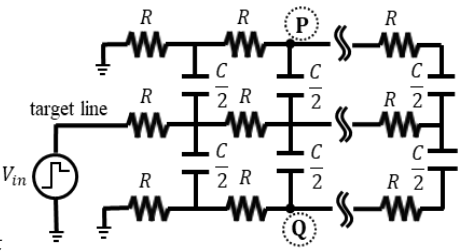

Fig. 2(a): Three RC delay lines

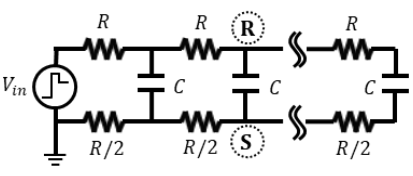

Fig. 2(b): The equivalent circuit of Fig .2 (a)

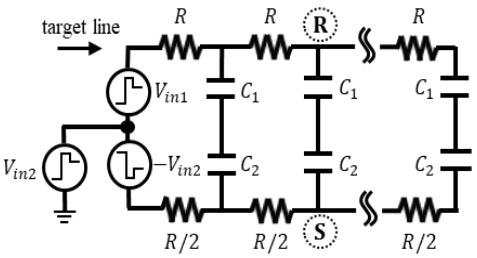

Fig. 2(c): The circuit conversion of Fig.2(b)

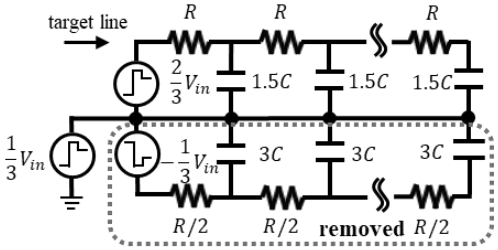

Fig. 2(d): Equivalent circuit of target line