A Study on Silicon-On-Insulator Nanowire Photodetectors with Bow-Tie Surface Plasmon Antenna

Doctor Thesis

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A Study on Silicon-On-Insulator Nanowire Photodetectors with Bow-Tie Surface Plasmon Antenna

ボウタイ表面プラズモンアンテナ付きシリコン・オン・インシュレーター　ナノワイヤ光検出器の研究

シャルマ　ヤシャ

静 岡 大 学

大学院自然科学系教育部

ナノビジョン工学専攻

２０１８年６月

Abstract

The main objective of this research is to put forward a novel idea of incorporating a surface plasmon (SP) antenna in the shape of a bow-tie to photodetectors, viz. silicon-on-insulator (SOI) nanowire pn photodiode and SOI nanowire n-type metal-oxide-semiconductor field-effect transistor (MOSFET). SOI nanowire photodiodes are expected to realize high speed operation due to the reduced parasitic capacitances, associated with small geometry and lower dielectric constant of the buried oxide below the silicon (Si) layer. However, they suffer from poor sensitivity due to the small Si thickness and the small area for light absorption.

Scaled down SOI MOSFET (gate length L= 65 nm and channel width W= 105 nm) has been recently characterized to be used as single photon detector centered on counting single hole, having various advantages and can outperform the conventional single-photon detectors. Conventional photodiodes for instance avalanche photodiodes and photomultiplier tubes rely on carrier multiplication to detect the incident photons. However, the carrier multiplication process leads to after pulses, high operational voltage, large dark counts and high electron transit time. SOI MOSFET photon detector based on single-hole counting can overcome such issues since the detection mechanism is based on counting

holes one by one. However, it suffers from low quantum efficiency due to less light absorption area.

By incorporating a surface plasmon (SP) antenna, the light absorption efficiency in a small thickness can be enhanced, and the light receiving area can be increased simultaneously. It is expected that when the light enters the nanoantenna, it resonantly excites the surface plasmons on the surface of gold bow-tie structure. Initially, the bow-tie is closed, but a nanogap can be created at the junction of the bow-tie by electromigration. The excited surface plasmons can result in an enhancement of electric field near the nanogap. Eventually, the optical near field will generate extra carriers within the depleted Si nanowire. A bow-tie structure is considered mainly for the simplicity of the design and it can also be used as a gate electrode of the SOI MOSFET, and can possibly enhance the electric field near the nanogap generating extra holes to be counted by the MOSFET. This may lead to increment in the quantum efficiency of the SOI MOSFET photon detector. Similarly bow-tie antenna can increase the cathode current in SOI pn-junction photodiode.

In the first part of the thesis, we explain the fabrication process of the nanowire photodetectors. Top-down approach is used, mainly because of the better control on the nanowire size and position and the repeatability of the processes involved. The fabrication process comprises of various

process steps of electron beam lithography, dry/wet etching, metal and dielectric deposition and annealing. Pre-developed recipes are used when available. New recipes are also developed to fabricate the devices efficiently.

In the next part of the thesis, we perform electrical and optical characterization of pn-junction photodiodes in visible incident light. We demonstrate the formation of nanogap in the bow-tie antenna by controlled passage of current through the bow-tie structure, thereby creating a nanogap by electromigration. The nanogap size can be quantitatively estimated by the tunneling current. Finite-difference time-domain simulations are also performed, which clearly show the electric field generated in the bow-tie structure is concentrated at the nanogap and there is an enhancement of electric field in the Si nanowire under the bow-tie antenna.

In the final part of the thesis, we experimentally demonstrate single-hole counting operation of the SOI nanowire MOSFET. The hole generation rate is observed to be directly proportional to the intensity of the incident light.

Since the fabrication process is compatible with the CMOS fabrication in the semiconductor industry, such devices bring about the new functionality of photon detection to CMOS integrated circuits.

Acknowledgment

In the beginning, I would like to express my deepest gratitude to my supervisor, Professor Hiroshi Inokawa, who believed in my passion and my ability to work in this field. I am grateful to him for his generous help and support. I am also thankful to him for guiding me through this work, and for his instructive advice that helped me observe problems from different angles. I have learned a lot from him about how to combine smartness and kindness, great dream and patience, as well as professionalism and humbleness at the same time, making me feel very fortunate to work under his guidance. I also would like to thank the members of my dissertation committee, Prof. Akihiro Ishida, Prof. Jun Kondoh and Prof. Hiroya Ikeda for their invaluable comments and suggestions in improving the quality of this work.

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Finally, I would like to sincerely appreciate my parents, Dr. Rajiv Sharma and Kamalakshi Sharma and brother Mayank Sharma for their never-ending love and unconditional support. My parents taught me to think big and work hard. They taught me that nothing can prevent a person's will to reach his dreams, except himself.

Hamamatsu, June 2018

Yash Sharma

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Chapter 1

INTRODUCTION

1.1 Research Background

In early 20th century it was proposed by Max Planck [1] and then by Albert Einstein [2] that the energy of a light beam is distributed in discrete bundles, called photons. Only in the year 1977 the first indisputable proof of the quantum nature of light was shown [3, 4]. Single photon generation and detection technologies find applications in various areas as shown in Fig. 1. The applications of single photon detectors are in three major domains. First, in order to detect weak light the distinct nature of light should be considered. Such instances can be observed in these sensing activities: low ambient light sensing and surveillance, medical imaging, astronomy, etc. Second, quantized energy structure of matter is crucial element. For instance photoelectric, infrared sensing and spectroscopic applications. In the third group, sensing activities take into consideration the quantum nature of light. For example in the realm of quantum computation and quantum communication, wherein photons are used as quantum bits [5], and quantum key distribution [6], to safely transfer information over long distances.

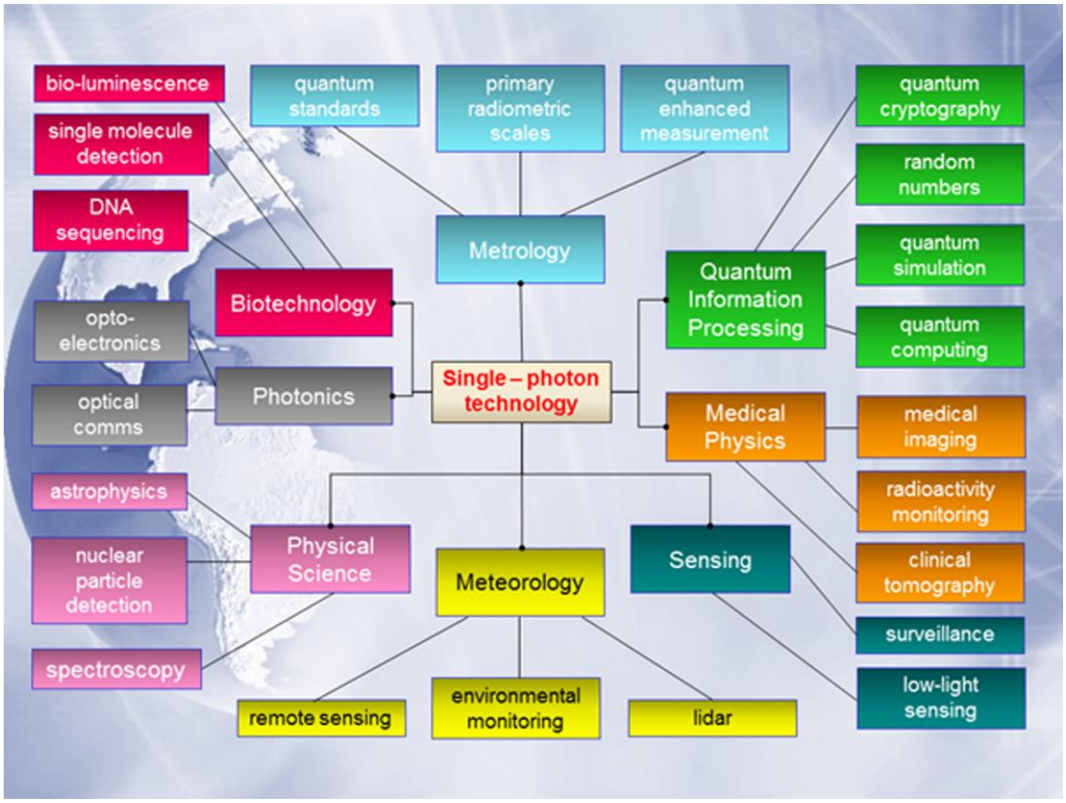

Fig. 1-1 Application areas of single photon generation and detection [7].

Quantum communication networks make use of optical fiber cables in which, information is sent using a single photon source thus, keeping the number of photons per pulse < 1. For receiving the information single photon detector can be used. Transmission of quantum information over long distances needs unconventional regeneration techniques which require sharing of polarization entangled photon pairs across communication channel. A detector is required at every repeater node of the channel to detect arrival of one photon entangled pair in a non-interfering way while maintaining the polarization information. Another application is quantum cryptography, which uses Heisenberg's uncertainty

principle by encoding information onto the intrinsic quantum states of single photons to enhance the security of the communication. Therefore, single photon detectors have to detect not just the presence of single photon but also provide a read out mechanism for the quantum states of single photon over a quantum communication network.

1.2 Overview of Photon Counting Technologies

This section presents the background behind the single photon detection technologies. A summary of several photon counting tools is provided.

Currently, there exist many photon detection tools that exhibit single-photon sensitivity [8]. Recognized detectors such as photo-multiplier tubes are vacuum tubes, whereas avalanche photodiodes, quantum dot detectors and superconducting detectors [9] are solid-state detectors.

When comparing photon detection technologies, several crucial parameters must be considered, such as: operational wavelength range of detector (spectral range), retune time of detector (dead time), number of false counts per second (dark count), ratio of output to input photons (quantum efficiency), resolving capability of the detector to many incident

photons (photon number resolution) and division of signal arrival times once photon has hit the detector (timing jitter) and noise equivalent power.

In established single photon detectors such as photomultiplier tubes and avalanche photodiodes the performance is inadequate because of carrier proliferation by large electric field, the long recovery time and afterward pulses, etc.

However, such problems can be addressed by straightaway counting the photo-generated carriers one after another instead of carrier multiplication by incident photon. Also, the operation speed is not limited by recovery time and after pulse cause by multiplication carriers. Thanks to the advances made in integrated circuit technology, a scaled down solid state device can be used as single-photon detector created on single charge counting.

Various examples of photon detectors, based on photon detection technique: such as detection by carrier multiplication in photomultiplier vacuum tubes and avalanche photodiodes, and detection by charge counting have been explained and summarized in the next section.

1.2.1 Photomultiplier Tubes (PMTs)

Demonstrated in the year 1935 [10, 11], PMT being the initial recognized photon-counting technology [12] consisted of a vacuum tube which has a light absorbing photocathode which emits electrons through photo-electric effect as shown in Fig 1-2.

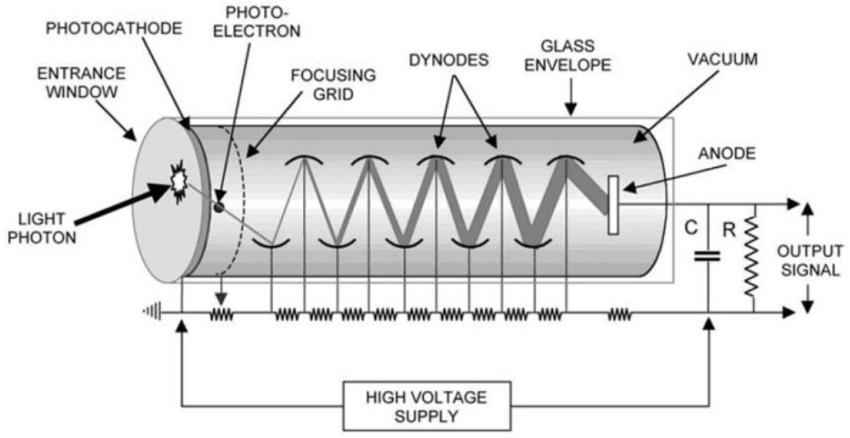

Fig. 1-2 Schematic view of a photomultiplier tube [13].

The operating principle of PMTs is easy to explain. The incident photon having photon energy larger than the work function of the material of photocathode, photocathode releases photoelectrons. These photoelectrons are then accelerated by applying potential to the 1st dynode of the tube and electron multiplication happens via secondary electron emission. Then secondary electrons are rushed towards the 2nd dynode of the tube and further multiplication happens.

At each subsequent stage more magnitude of electrons than previous stages are released. Finally the electrons are collected by anode and the photocurrent is detected.

PMTs are commercially available and used in experiments internationally: 13000 PMTs were used in the Super Kamiokande observatory [14] to detect Cerenkov radiation from solar neutrinos. Since the operation of PMTs rely on carrier multiplication, it cannot resolve multiple photon entering at the same time and also require high voltage for operation. The detection of photons using PMTs can also be affected by external magnetic fields as it is a vacuum tube. Another disadvantage is not being mechanically robust. Some of these issues can be addressed by using a solid state photon detector such as an avalanche diode.

1.2.2 Avalanche Photodiodes (APDs)

First solid-state photon detection was based on avalanche photodiodes (APDs) and was invented in 1961 [16]. APDs can be considered as semiconductor analog to PMTs. APDs are highly sensitive semiconductor based photodetectors that convert incident light to electricity by photoelectric effect and are operated under reverse bias. They provide a built-in 1st stage of internal gain through avalanche multiplication of carriers. In general, higher the reverse voltage, higher the gain. Due to

this internal gain mechanism, APDs are efficient in detecting low light and are used in various applications. The APD structure is a typical p-n junctions or p-i-n junctions as shown in Fig. 1-3.

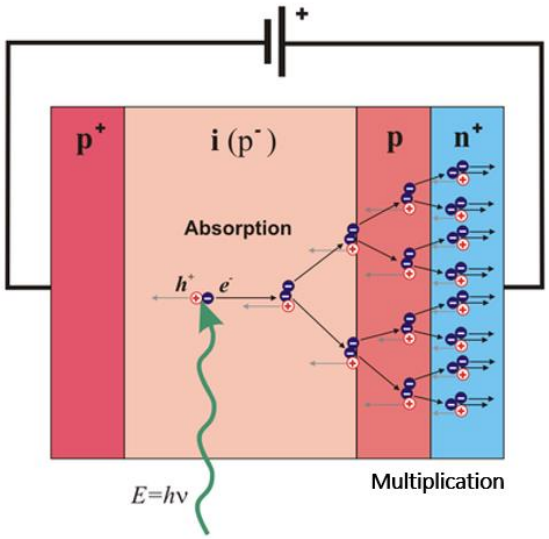

Figure 1-3 Cross-section of an avalanche photodiode [17].

The mechanism of detection can be explained as follows: incident photon on entering the photodiode, creates an electron-hole pair in the depletion region of the p-n junction, if photon energy is greater than the band gap of material. The created electron-hole pairs are separated by the electric field, resulting in electrons drifting near the n^+ side and holes drifting near p^+ side. On increasing the external reverse bias, higher electric field can be created resulting in acceleration of holes and electrons. These accelerated electrons then collide with the crystal lattice and create secondary electron-hole pairs. This phenomenon is known as impact ionization. This impact ionization leads to creation of large electron-hole

pairs know as avalanche process. Generally, impact ionization commences at electric field strengths of $>10^5$ V/cm. [18]

1.2.3 Single-Photon Avalanche Photodiode (SPAD)

In 1980, single-photon avalanche diodes (SPADs) were realized as technique of operating APDs to sense distinct photons [19]. By running the APD in 'Geiger-mode', in which external reverse bias bigger than APD's breakdown voltage is used [20], APD provides digital pulses on absorption of single photons. SPAD is a solid-state device with p-n diode structure as shown in Fig. 1-4, having replaced PMTs in many applications. The important distinction among SPAD and APD is: SPADs are explicitly designed to function with reverse-bias voltage higher than the breakdown voltage, however APDs function below the breakdown voltage.

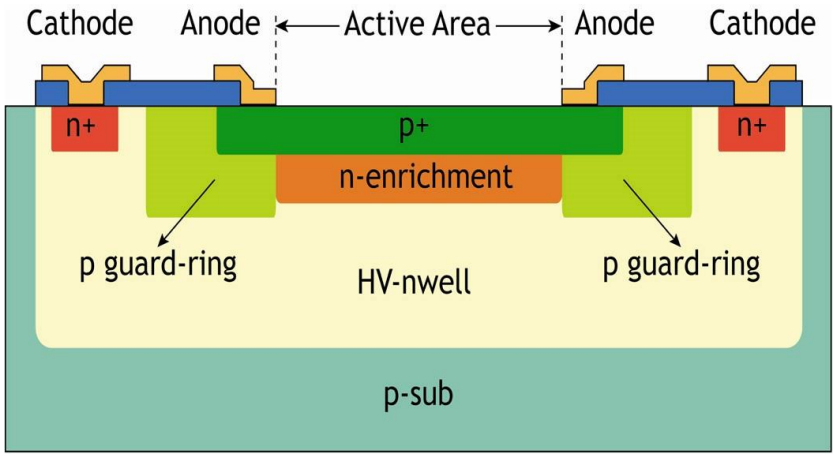

Fig. 1-4 Schematic cross section of single-photon-counting avalanche diode device. HV: High-voltage [21].

On biasing SPAD at higher voltages than breakdown voltage, electron-hole pairs get produced at a quicker rate than can be obtained by the resultant electric field which is very high (higher than 3×10^5 V/cm). When photon is incident on the photodiode electron-hole pairs will be created and an avalanche process will take place. Instantaneous reduction of avalanche is crucial to avoid loss to photodiode and this creates small current pulse signifying the discovery of one photon. This avalanche pulse actions as binary signal, even though if any photon was not sensed, contrasting to the analog signal acquired from electron multiplication in APDs. Reduction can be realized through a passive quenching resistor or by a complicated active quenching circuits. Main SPAD figures-of-merit comprise of detection probability, spectral response, dark count rate, timing precision (jitter), sampling speed and active area.

Silicon centered SPADs functioning in Geiger mode accomplish single-photon sensitivity in VIS-NIR, having little dark counts. Also, the timing jitter is shortened to small magnitudes of 10^{-12} s. SPADs have a shortcoming since resolution of incident photons is not good because the binary output signal cannot represent number of input of photon.

1.3 Single-Photon Detector based on Single-Charge Counting

1.3.1 Photodetector based on Single Electron Transistor

Photon detection based on a metallic single-electron transistor (SET) electrometer was demonstrated in the year 1992 by A. N Cleland et al. The device showed intrinsic noise smaller than one electron per unit bandwidth at 20 mK. The circuit diagram is shown in Fig. 1-5, SET consists of ultra-small planar tunnel junctions joined in series. Metallic SET was fabricated on oxidized p-type Si chip with a room-temperature resistivity of 6 Ω-cm, boron doping density of $2x10^{15}/cm^3$. Oxide layer thickness was 450 nm, no electrical contacts were created to Si substrate.

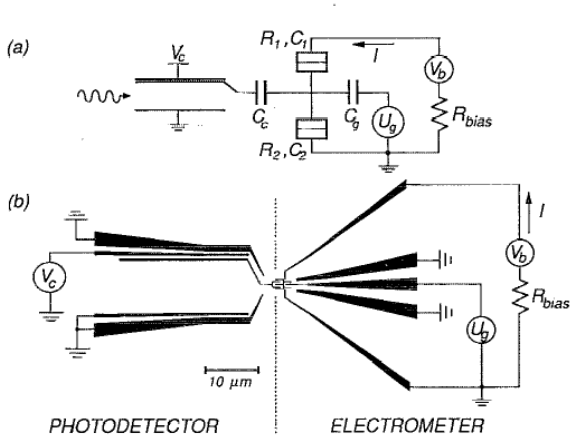

Figure 1-5 (a) Circuit diagram for the experiment, (b) Geometrical layout of the metallic parts, deposited on the photon-absorbing Si substrate [22].

Assuming a perfect detector having collection efficiency of $\eta = 1$, dark current resembles to minutest light flux of $\Gamma = 0.06$ photons/s. For IR light with $\lambda = 30$ μm, the noise-equivalent power can be estimated to be $NEP = (hc/\lambda)(2\Gamma)^{1/2} = 2\times10^{-21}$ W/Hz$^{1/2}$, and equivalent detectivity for this detector with area $A = 300$ μm^2 can be estimated $D^* = \sqrt{A}/NEP = 8 \times 10^{17}$ cm*√Hz /W.

1.3.2 Photodetector based on GaAs SET Quantum Dots

O. Astafiev et al. in 2002 demonstrated single-photon counting by SET designed with capacitively coupled GaAs/$Al_xGa_{1-x}As$ parallel quantum dots (QDs) at microwave frequencies approximately 500 GHz [23]. The device is typically an SET containing double QDs fabricated on a high mobility modulation doped GaAs/$Al_xGa_{1-x}As$ single-heterostructure crystal with two-dimensional electron gas having sheet density of $n_s = 0.9\times10^{15}$ m^{-2} and a mobility of $\mu = 190$ m^2/V s at $T = 4.2$ K. The sample is an SET consisting of double QDs as represented in Fig. 1-6(a). The dark switch rate (W_{DS}) is 0.01 s^{-1} and quantum efficiency (QE) is 0.1%, and the noise equivalent power (NEP) is the order of 10^{-21} W/Hz$^{1/2}$, which is steady with the projected power of incident radiation.

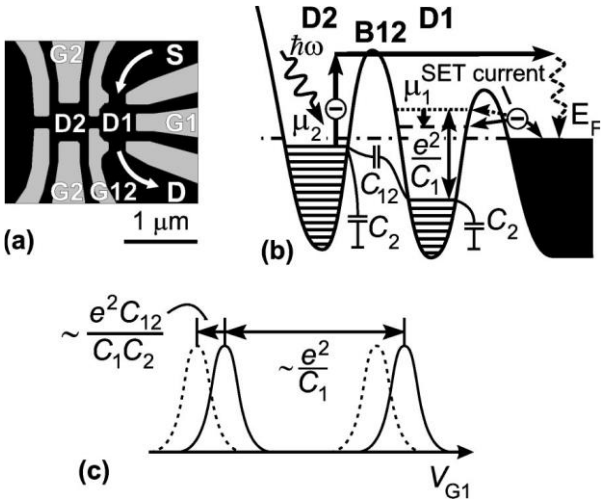

Figure 1-6 (a) Top view of double-QD photon detector, (b) Schematic representation of photo excitation mechanism, (c) Conductance oscillation and a peak shift caused by single photoexcitation event [23].

1.3.3 Photodetector based on Silicon Two-Dimensional Multiple-Tunnel-Junction Array

Single-photon detection operating on Si-based two-dimensional (2D) multiple-tunnel-junction (MTJ) field-effect transistor (FET) was described in 2006 by R. Nuryadi et al [24]. The schematic view of the device is shown in Fig. 1-7 (a). At an operational temperature of 15 K, single photon is detected as random telegraph signal (RTS) in the tunneling current regime. The wavelength and intensity of the incident light determines the frequency of the RTS events.

For an equivalent 2D circuit based on an array of 7 x 8 dots as shown in Fig. 1-7 (b) Monte Carlo simulation depicts that when a photon is

absorbed in the dots the on-state of RTS occurs. The charging effect of the dot influences the current in the circuit. Similarly when the dot is discharged the off-state of the RTS appears. Also, it was observed that for large screening lengths, RTS is activated not only by charging of the adjacent dots, but also by the charging of dots far-away from path. Results confirmed the possibility of development of single-photon detector using 2D dots system.

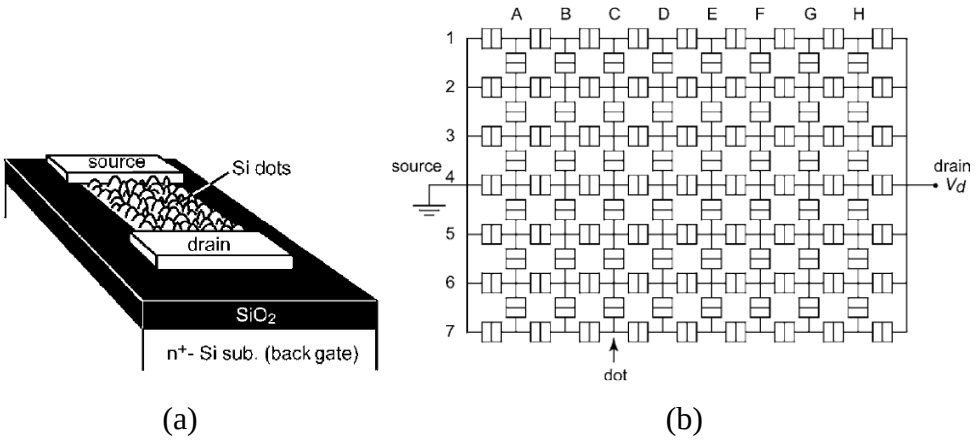

Figure 1-7 (a) Schematic view of a 2D Si multi-dot channel FET. (b) Equivalent circuit of the 2D tunnel junction array consisting of 7x8 dots used in the simulation. [24]

1.3.4 Photodetector based on GaAs FET gated by layer of Quantum Dots

In 2000, A. J. Shields et al had reported about a quantum-dot-based photon detector that uses coulomb interaction resulting from trapping of photo excited carrier by quantum dot [25]. The change of source-drain

current in the device can be interpreted as a coulomb interaction, measured at 4 K. The device structure and SEM image of the gate of quantum dot field-effect transistor-based single-photon detector is depicted in Fig. 1-8.

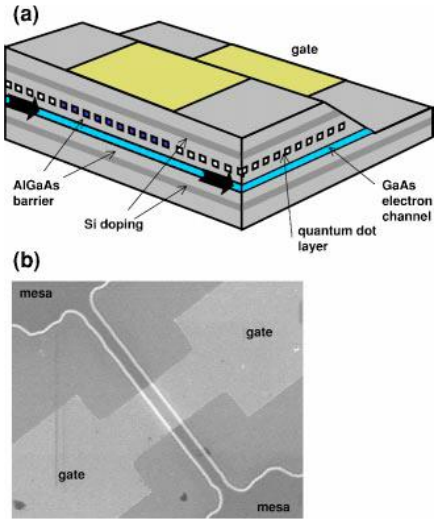

Figure 1-8 (a) Schematic of the quantum-dot FET structure, (b) SEM image of gate region [25].

The device contains a GaAs/$Al_{0.33}Ga_{0.67}As$ modulation-doped FET comprising a layer of InAs quantum dots divided from the 2DEG in the GaAs channel by a thin $Al_{0.33}Ga_{0.67}As$ barrier.

Upon illumination of the device, electron–hole pairs are produced within the structure. Due to the internal electric field the photo-excited holes in quantum well are drifted near negatively charged quantum dots. After tunneling recombination with surplus electrons occurs . Temporarily, photo-excited electron remains in 2DEG layer. Hence, illumination diminishes the quantity of electrons confined within dots, with a equivalent proliferation in the 2DEG density.

1.3.5 IR detection with Silicon Nano field-effect-transistors

In 2007, K. Nishiguchi et al., characterized nanoscale metal-oxide-semiconductor field-effect transistors (MOSFETs) to detect infrared (IR) signal at room temperature. It is a gain cell (GC) (shown in Fig. 1-9), which is used for charge detecting having single-electron resolution. The incoming IR signal stimulates conduction-band electrons in the intrinsic channel of MOSFET and are introduced via energy blockade into a storage node (SN) electrically made by the MOSFET. Small signals, beginning after electrons, deposited in SN are observed by the electrometer with single-electron resolution.

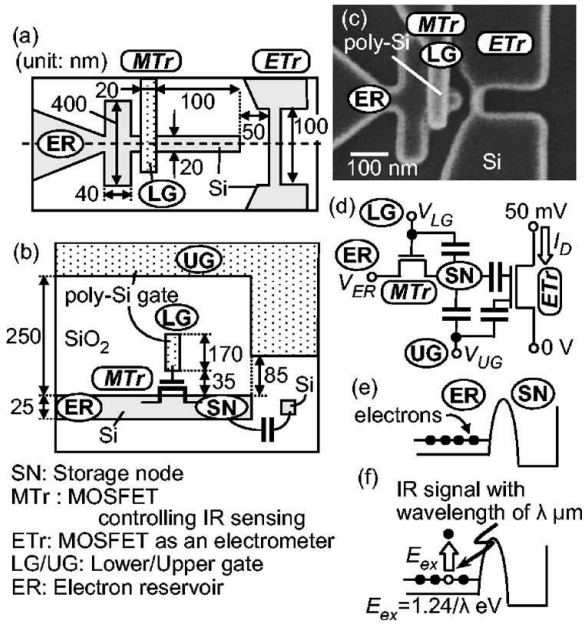

Figure 1-9 (a) Schematic top view, (b) Cross-sectional view, (c) SEM image, (d) Equivalent circuit, (e) Energy band diagram without IR signal, and (f) Energy band diagram when IR signals are irradiated [26].

1.3.6 Photodetector based on Si Nanowire field-effect-transistor

A. Fujiwara et al demonstrated recognition of lone electrons and lone holes at room temperature in Si nanowire transistors by means of an electron-hole system. The schematic top view and cross section of the Si nanowire MOSFET and is shown in Fig. 1-10. When light is incident on the device, carriers are generated and accumulated in one quantum dot electrically produced in Si nanowire by top gate. These collected charges disturb the current of flowing electrons along the bottom of the Si nanowire.

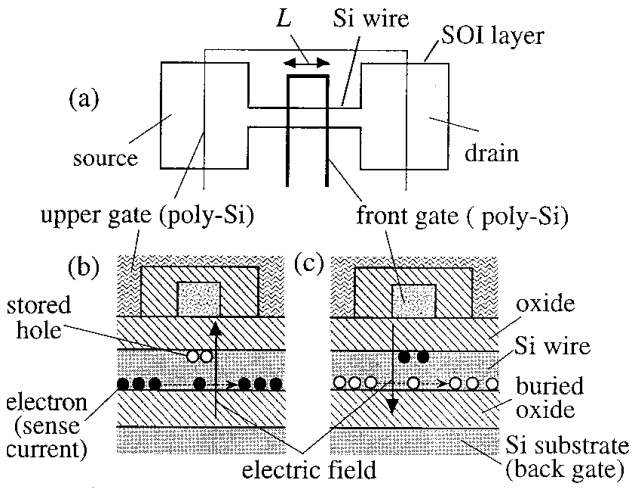

Figure 1-10 (a) Schematic top view of the Si-wire MOSFET, (b) Schematic cross section of the device along the Si wire for the *n*-channel MOSFET, (c) Schematic cross section for the *p*-channel MOSFET [27].

The device is fabricated on silicon-on-insulator (SOI) wafer with top Si layer thickness of 30 nm and detector area 64 μm^2.The efficiency of light absorption was anticipated to be 1.4% at λ= 650 nm. The efficiency of accumulating holes into Si wire was calculated to be 0.9%. Despite having

poor quantum efficiency of 0.013%, the background generation rate of 0.012 s^{-1} results in low NEP of $7x10^{-15}$ W at 1 Hz and $2x10^{-17}$ W at 10^{-3} Hz, which are similar to present photodetectors.

1.4 Photodetectors with Surface Plasmon Nanoantennas

1.4.1 Si Nano-Photodiode with Bull's eye Surface Plasmon Antenna

T. Ishi et al in the year 2005, had proposed a nano-photodiode with a subwavelength active area by means of optical near-field enhanced by surface plasmon resonance. A Si Schottky photodiode was fabricated that contains operational area of 300 nm in diameter and surface plasmon antenna in shape of *bull's eye* to produce the carrier inside the operational area. The surface plasmon antenna basically has a subwavelength aperture with concentric grating structure made of silver on top of chromium. The fabricated photodiode showed an upsurge of photocurrent by large amount in comparison to that devoid of a surface plasmon antenna. This outcome proposed an improved photogeneration of carriers inside the semiconductor due to the application of surface plasmon resonance. This kind of Si nano-photodiode is a prospective fast-speed optical signal

detector since optoelectronic exchange process happens within subwavelength scale.

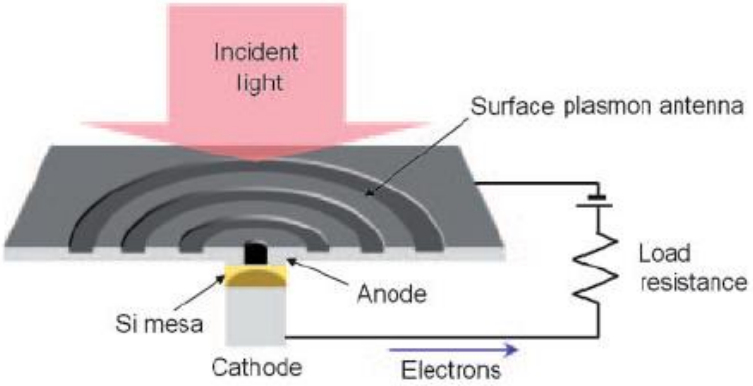

Figure 1-11 Schematic cross sectional view of nano-photodiode [40].

1.4.2 Si photodiodes with Au Resonant Antenna

M. W. Knight et al in the year 2005, showed that two distinct, independent functions viz. light harvesting by nanoantennas and conversion of light into a current of electrons by photodiodes can be united into one device. Photons incident on the gold nanoantenna stimulate resonant plasmons, which loose energy to create “hot” electrons. These are then brought over the potential wall present by nanoantenna and semiconductor interface, causing a photocurrent. This resulting design is

extremely dense and has spectral response ranging to energy lesser than the band gap.

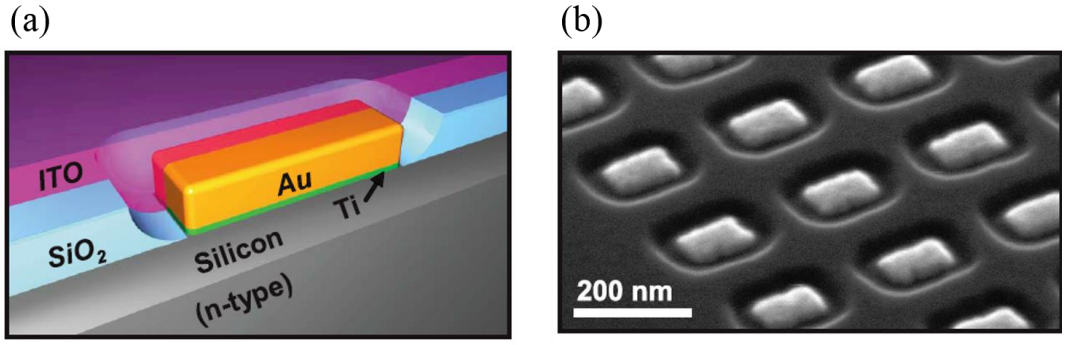

Figure 1-12 (a) Representation of a single Au resonant antenna on an n-type silicon substrate, (b) Scanning electron micrograph of a representative device array [41].

1.5 Motivation of Present Work

As described in previous sections, conventional photodetectors viz. PMT and APD experience high dark counts, limited speed of operation, large recovery time and high operation voltage mainly due to using carrier multiplication mechanism for photon detection. These issues can be solved by photon detection based single-charge counting. However, the reported devices still have issues in low QE, operation speed and temperature. The low QE and poor sensitivity mainly arise due to small Si thickness and small area for light absorption. By incorporating a surface plasmon (SP)

antenna [40], the light absorption efficiency in a small thickness can be enhanced, and the light receiving area can be increased simultaneously.

This thesis aims at putting forward a novel idea of incorporating a surface plasmon antenna in shape of a bow-tie to photodetectors viz. SOI nanowire pn photodiode and SOI nanowire n-type MOSFET.

The benchmark comparison of single-photon detectors is provided in Table 1.1. Our study is focused on fabrication of SOI nanowire photodiode and MOSFET with bow-tie nanoantenna and their photo response.

Table 1.1 Benchmark comparison of single-photon detectors

S.No.	Detector type		Dark Count Rate	Max. Count Rate	Quantum Efficiency	Wavelength	Light receiving area	Timing Resolution	Photon-number resolution	Operation temperature (K)	References
1	PMT	Visible-NIR	100 Hz	10 MHz	40% @ 500 nm	300-720 nm	5 mm^2	300 ps	Very limited	300	[28]
		IR	200 Hz	10 MHz	2% @ 1550 nm	300-1700 nm	3 x 8 mm^2	300 ps	Very limited	200	[29]
2	APD	Si	<25 Hz	10 MHz	70% @ 630 nm	400-1700 nm	170 μm^2	300 ps	Very limited	300	[30]
		InGaAs	$<10^4$	1 MHz	25% @ 1550 nm	900-1700 nm	300 x 250 x 150 mm	300 ps	No	200	[31]
3	SPAD	Si	25 Hz	10 MHz	49% @ 550 nm	375- 1000 nm	20 μm^2	35 ps	No	200	[32]
		InGaAs	91 Hz	10 MHz	10% @ 1550 nm	300-1700 nm	25 μm^2	370 ps	No	200	[33]
4	SSPD	SSPD	<0.01	250 MHz	10% @ 1550 nm	400-5600 nm	10 x 10 μm^2	18 ps	Study Ongoing	2-4.2	[34, 35]
		TES	<0.001	20 kHz	92% @ 1550 nm	100- 5000 nm	25 x 25 μm^2	300 ns	Yes	0.1	[36, 37]
5	Single Charge Counting	Si NW FET	<0.01	10 Hz	0.013% @ 650 nm	650 nm	64 μm^2	-	Yes	300	[27]

Here we research on fabrication and characterization of surface plasmon antenna in shape of a bow-tie to photodetectors viz. SOI nanowire pn photodiode and SOI nanowire n-type MOSFET. The research done in this thesis can be broadly summarized as follows:

1. Creation and optimization of process flow, process conditions and recipe for fabrication of SOI nanowire MOSFET and pn photodiode with bow-tie surface plasmon nanoantenna.
2. Optimization of measurement conditions related to the photo response of the SOI nanowire photodiode with bow-tie nanoantenna. Effective detector area of photodiode is measured with respect to the incident light wavelength.
3. Characterization of SOI MOSFET for single photon sensitivity, electrical and optical response of the fabricated SOI nanowire MOSFET with gold bow-tie antenna.

1.6 Synopsis of Book Chapters

This thesis consists of five chapters and content of each chapter is summarized as follows:

In **Chapter 1,** we present the research background related to various photon counting technologies. It covers the conventional and state of the art photodetectors based on, two mechanism of photon detection: carrier

multiplication and detecting single carriers one by one. Important advances that set the grounds for photon detection by SOI MOSFET and reports on conventional single-photon detectors including ones based on single-charge counting are summarized. The motivation behind current research is presented in this chapter.

In **Chapter 2**, we explain the various fabrication steps required to fabricate SOI nanowire devices with gold bow-tie surface plasmon antenna. The devices are fabricated in a top-down approach on a commercially available SOI wafer from Soitec™ in a clean room facility with state of the art equipment. The fabrication process is compatible with CMOS fabrication done in semiconductor industry.

Chapter 3, provides detailed methodology of characterization of SOI nanowire pn photodiode with gold bow-tie surface plasmon antenna. The measurement setup to measure the spectroscopic response of the device is explained. Creation of nanogap in the junction of bow-tie by process of electromigration is explained and its effect on the spectroscopic response of the photodiode is measured. Also, 3D finite difference time domain simulation is presented to simulate the near-file profile in the bow-tie antenna without and with nanogap.

In **Chapter 4**, we investigate the single photon detection by SOI MOSFET with upper and lower gates. Typical drain current waveform and histograms at various incident light intensities are presented. Also, we

perform electrical and optical characterization of fabricated SOI nanowire MOSFET with bow-tie antenna. The measurement setup used is also explained.

Chapter 5 contains the summary and conclusions of this research and provides suggestion on the direction for future development in this area.

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Chapter 2

FABRICATION OF SILICON-ON-INSULATOR NANOWIRE DEVICES WITH GOLD BOW-TIE SURFACE PLASMON ANTENNA

2.1 Introduction

This chapter is dedicated to the fabrication of step by step methods developed to fabricate the device. CMOS technology follows the approach of top-down to fabricate the devices. Although bottom-up methods are able to grow nanowires with diameters as small as few nanometers, [1-3], and out of a wide variety of materials in a high-yield and reproducible manner [4-7], they suffer from difficulties during assembly of nano-structures. Top-down methods are able to create nanowires at the desired locations [8]. The ability of placing an individual nano-component onto a precise location is an important fabrication step in our device fabrication, therefore top-down methods are preferred to fabricate a silicon-on-insulator (SOI) nanowire metal-oxide-semiconductor (MOS) field-effect transistor (FET) and nanowire photodiode.

The objective of the gold bow-tie nanoantenna to be fabricated is to act as an optical surface plasmon antenna at a resonant incident light wavelength. Due to dependence of geometry and sizes of the nanoantenna on the resonance, construction of nanoantennas involves consistent fabrication procedures with resolution lesser than 10 nm so that small sizes can be correctly fabricated, especially antenna length. Due to many novel nano-designing methods are pushed to their limits and is studied as a challenge in fulfilment of optical antennas and plasmonic devices. Several bottom-up and top-down nanofabrication techniques have been utilized to fabricate optical antennas. Bottom-up methodologies, employ the chemical synthesis and self-assembly of metal nanoparticles. To be effective, bottom-up fabrication techniques usually need accurate size control and nano-positioning. Also, assembly approaches to generate significant designs. Many efforts to develop the purpose and consistency of nano-structuring and also to correctly comprehend the function of crystallinity in accomplishment of better-quality light responses for plasmonic structures are going on. The uneven exteriors and multi-crystalline materials can be unfavorable because of improved dispersion of plasmons and not properly distinct geometric factors that result from anisotropic reaction of multi-crystalline constituents throughout assembly. On the other hand, top-down approaches, viz. electron-beam lithography (EBL)

and focused-ion beam (FIB) milling, usually begin from thin metal film on top of a transparent but electrically conductive substrate, required to prevent charging results. Generally, top-down approaches are efficient in fabricating large arrays of almost indistinguishable nanostructures with distinctly demarcated lengths and orientations.

The fabrication steps in this chapter will focus on fabrication of **n-channel MOSFET** and **pn-diode** devices with gold bow-tie nanoantenna.

We have used 100 mm SOI wafers from Soitec™ with initial SOI thickness of 340 nm ± 50 nm. Buried oxide (BOX) thickness of 400 nm ± 7.5 nm. The SOI wafer has been produced by Separation by Implantation of Oxygen (SIMOX) processing, wherein oxygen ion beam implantation process occurs after high temperature annealing in order to create the BOX [9]. The initial impurity (boron) concentrations in the SOI and the substrate are both 1×10^{15} cm^{-3}, with the crystal orientation of <100>. As shown in Fig. 2-1, SOI chips of 2 cm x 2 cm dimensions were cut using a diamond cutter and n-type MOSFET and pn-diode devices were fabricated. Thickness of top Si layer is 60 nm, which is achieved by SOI thinning by thermal oxidation of Si and removal of oxide. Thicknesses of buried oxide and gate oxide are 400 and 25 nm, respectively. SOI thinning is done using wet thermal oxidation, where water is used instead of oxygen (used in dry oxidation), the water molecule can dissociate at high temperatures that can diffuse in the silicon

faster than molecular oxygen. It results in a higher growth rate of oxide resulting in faster thinning of SOI. Whereas, the gate oxide is grown by dry thermal oxidation since it results into better quality oxide having high density oxide and higher breakdown voltage.

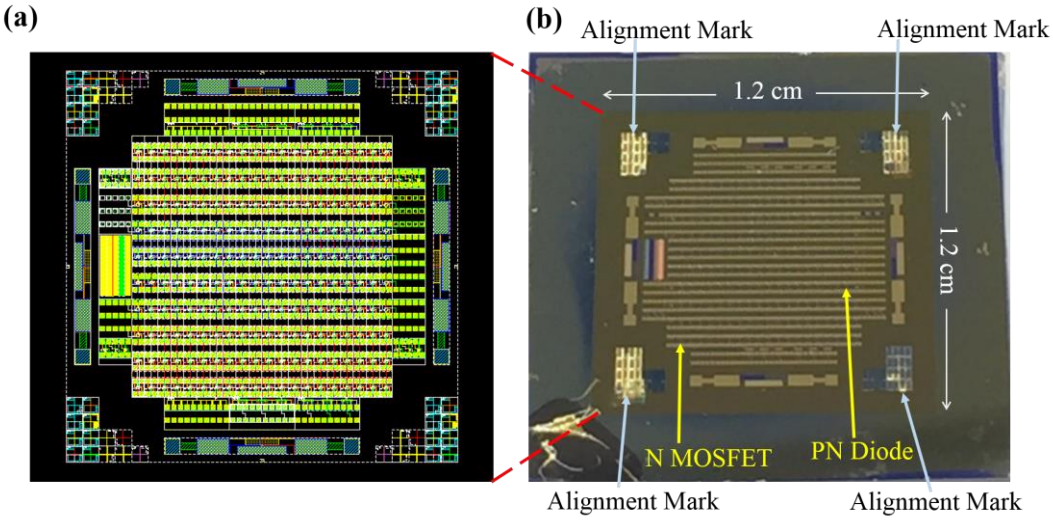

Fig. 2-1 (a) CAD Layout with various mask pattern for UV lithography and electron beam lithography, (b) Fabricated SOI chip with alignment marks and n-type MOSFETs and pn-diode devices.

2.2 Fabrication of n-type SOI Nanowire MOSFET

The device fabrication is divided into 4 major steps: (1) fabricating the junctions (doping) source/drain, (b) Patterning of SOI to delineate Si nanowire and form active regions, (c) Opening of contact holes, (d) source, drain and gate contacts.

Source/drain region is patterned in SOI by UV lithography and phospho-silicate spin-on-glass (PSG) is spun on the SOI. Major fabrication steps are shown in Fig. 2-2. A conventional doping technique, based on thermal-

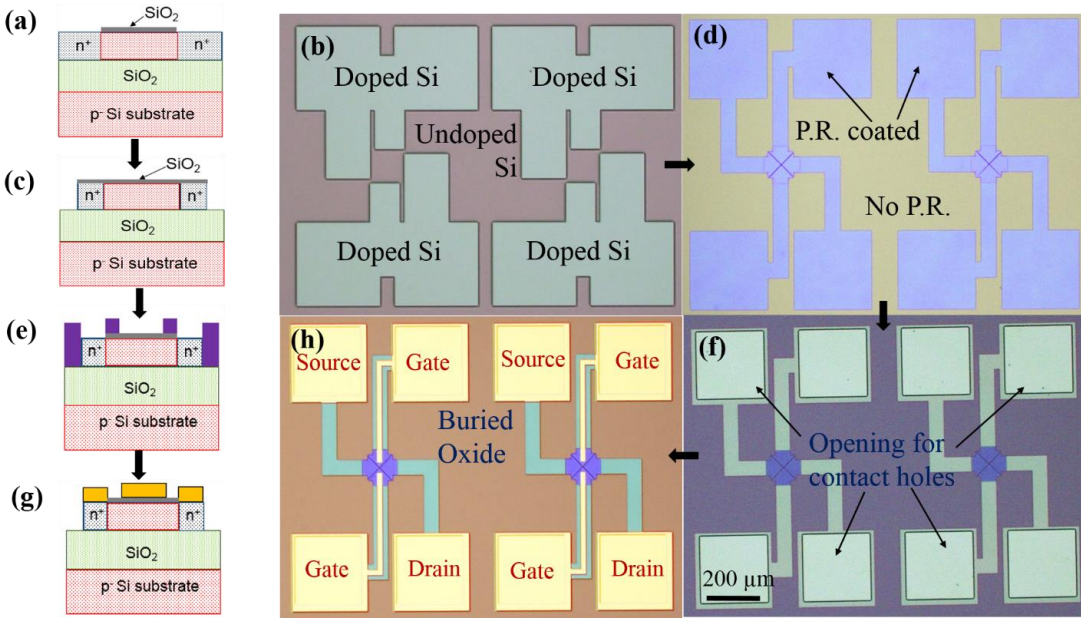

Fig. 2-2 (a) Major fabrication steps (a) Phosphorus doping of SOI for source/drain region, (b) corresponding optical microscope (OM) image (c) Patterning of SOI to delineate Si nanowire. (d) OM image, (e) Opening of contact holes (f) OM image, (g) Deposition of Au/Ti for terminals (h) Corresponding OM image.

diffusion from PSG as a dopant source, was used to create phosphorus (P)-doped source/drain regions.

For P doping process, oxide layer with thickness 20 nm was used as a P-doping mask, as shown in Fig. 2-2(a). On the open region (without mask), 1 nm oxide was grown as a protective layer. This 1 nm layer reduces the surface roughness of the doped silicon area. The phosphorus is then diffused at 880ºC for 20 minutes to achieve sheet resistance of 87 Ω/□ estimated by four point probe method. The resistivity was calculated considering the thickness of the SOI layer and the doping concentration was estimated to be >2 x 10^{19} cm^{-3} by using Irwin's curves (resistivity vs impurity concentration).

Fig. 2-2 (e, f) shows the opening of the contact holes on the silicon. It is done by etching of the gate dielectric (SiO_2 and SiN_x) by buffered hydrofluoric acid (BHF). Wet etching is isotropic in nature and since the gate dielectric has to be completely etched and the geometry of the etched SiO_2 is not a concern, it is preferred.

The channel of the SOI MOSFET is in the form of a Si nanowire (NW), it has been patterned using electron beam lithography (EBL) with positive tone resist and etched using reactive ion etching (RIE). The dose of electron beam during EBL is important to be optimized so that the resulting pattern is not over or under developed.

Various process steps to fabricate the n-type SOI nanowire MOSFET are tabulated in Table 1.

Table 2.1 Fabrication process flow of the SOI MOSFET

Process 1: SOI thickness adjustment	Process 4: SOI Patterning	Au/Ti Dep osition Ti: 5 nm, Au: 50 nm
		Liftoff
Wafer Introduction SOI (Si 340 nm/BOX 400 nm, p-type, 14~22 Ω·cm)	Thermal Oxidation (Dry 900 degC, Target: SiO2 20 nm)	Cleans
Thermal Oxidation (Wet 1000 degC, Target: SiO2 523 nm)	Thermal Annealing (Dry 1000 degC)	
SiO2 Removal (50% HF 25 cc, Water 100 cc)	Resist Coating (HMDS, OFPR/Positive tone resist)	Process 8: Back SiO2 Removal
Thermal Oxidation (Dry 1000 degC, Target: SiO2 57 nm)	UV Lithography	
SiO2 Removal (50% HF 25 cc, Water 100 cc)	SiO2 Etching (Wet Etching BHF)	Resist Coating for Protection of Top Surface (HMDS 3000rpm, OFPR CP-54)
Thermal Oxidation (Dry 1000 degC, Target: SiO2 57 nm)	Resist Removal (Wet)	Back SiO2 Removal (BHF)
SiO2 Removal (50% HF 25 cc, Water 100 cc)	OCD coating removal (HF Cleans)	Resist Removal (Acetone)
Process 2: Alignment Mark Fabrication	Process 5: Si NW Fabrication	Process 9: Contact Hole Fabrication
		Resist Coating
Thermal Oxidation (Dry 900 degC, Target: SiO2 20 nm)	Resist Coating (HMDS, ZEP diluted)	UV Lithography
Resist Coating (HMDS, OFPR/Positive tone resist)	EB Exposure	Resist Development
UV Lithography	SiO2 Etching (RIE CHF3)	SiNx and SiO2 Etching (Wet BHF)
Resist Development	Resist Removal (RIE O2)	Resist Removal
SiO2 Etching (Wet Etching BHF)	Bulk Si Etching (RIE SF6)	
SOI: Si Etching (RIE SF6)	Piranha 1 Clean	Process 10: PAD Fabrication
BOX: SiO2 Etching (Wet Etching BHF)		Resist Coating (1/2 Lower)
Bulk Si Etching (RIE SF6)	Process 6: Gate dielectric	Resist Coating (2/2 Upper)
Resist Removal (RIE O2)		EB Exposure
	Piranha 1 Clean	Resist Development (2/2 Upper)
Process 3: Phosphorus Doping	Thermal Oxidation (Dry 900 degC, Target: SiO2 20 nm)	Resist Development (1/2 Lower)
	SiNx deposition (Target: 6 nm. ECR Sputtering System)	NHF4 Clean (Just before E-beam PVD for Metal Deposition)
Thermal Oxidation (Dry 900 degC, Target: SiO2 20 nm)		Au/Ti Deposition Ti: 20 nm, Au: 300 nm
Resist Coating (HMDS, OFPR/Positive tone resist)	Process 7: Antenna Fabrication	Liftoff
UV Lithography		Cleans
SiO2 Etching (Wet Etching BHF)	Resist Coating (HMDS, ZEP diluted)	
OCD coating: Spin on glass	EB Exposure	
Pre-deposition, Drive-in: Heating furnace	Resist Development	
OCD coating removal		

The electron beam dosage during electron beam lithography can be calculated by the following formula:

$$\text{Dosage } (\mu C/cm^2) = \frac{\text{Beam current (A) x Dose time (s)}}{(\text{Scan step})^2\ (m^2)} \qquad (1)$$

Fig. 2-3 shows the optimization of the electron beam dose. Various beam dose from 90 to 140 $\mu C/cm^2$ were used as shown in Fig. 2-3 (a-f).

The scan step and beam current are fixed at 2 nm and 100 pA, respectively. By optical microscope it is observed that at electron beam dose of 90 and 100 μC/cm^2 the photoresist does not get completely developed and it is still present at the corners of the test pattern indicating an underdeveloped pattern, suggesting an insufficient dose.

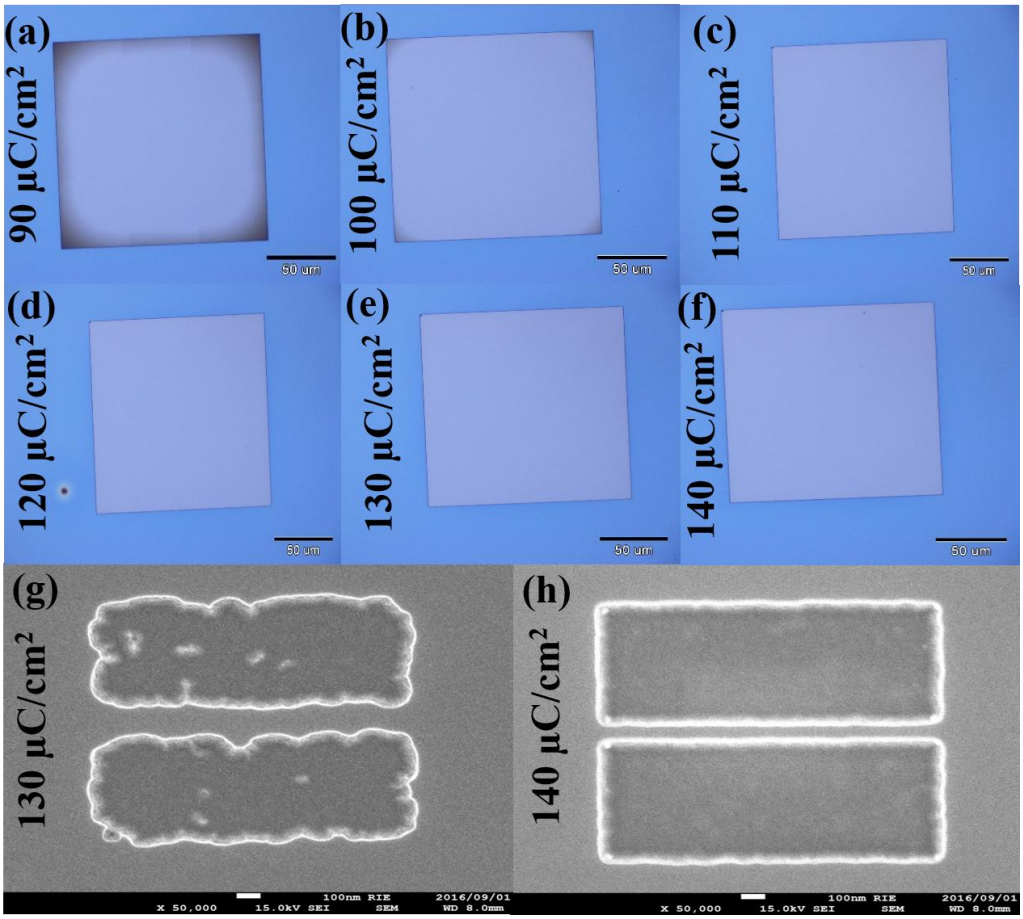

Fig. 2-3 (a-f) OM images of test pattern on Bulk Si samples after EBL to check for appropriate electron beam dosage energy at electron beam energy of 90, 100, 110, 120, 130 and 140 μC/cm^2, respectively. In (a, b) photoresist is present at the corners which shows the pattern is underexposed. Suggesting insufficient dosage. (g, h) FE-SEM images at electron beam energy of 130 and 140 μC/cm^2. (g) The Si NW pattern is underdeveloped at dosage of 130 μC/cm^2 which is also insufficient. (h) Dosage of 140 μC/cm^2 results in a good pattern.

Field emission scanning electron microscope (FE-SEM) image of Si NW for dose of 130 and 140 μC/cm^2 is shown in Fig. 2-3 (g-h). At the dose of 130 μC/cm^2, the geometry of the developed nanowire is not appropriate indicating an underdeveloped pattern. Whereas, the beam dose of 140 μC/cm^2 yields a better developed pattern. It is correct to consider 140 μC/cm^2 as minimum electron beam dosage required for a properly fabricated Si NW.

With the beam dosage of 140 μC/cm^2, various Si NWs of designed widths (W_{Si}) from 52 to 300 nm were fabricated on bulk Si substrate and SOI substrate to optimize the e-beam dose and exposure time during EBL and RIE recipe.

After patterning for Si NW and development of the photoresist, reactive ion etching (RIE) of silicon in SF_6 + O_2 plasma is done. Etching by SF_6 at low pressures, such as 5 Pa results in high etching anisotropy of the etched silicon NWs. The flow rates of 24 sccm and 6 sccm for SF_6 and O_2, respectively are maintained. The etching time is varied based on the thickness of top silicon layer. In order to optimize the etching conditions, silicon NWs were fabricated in bulk Si and SOI samples. From Fig. 2-4, it can be observed that the etching rate in RIE for bulk Si and SOI samples is same but the actual width (AW) of Si NWs after

fabrication is 70 to 80 nm narrower than the designed width due to the lateral etching of the Si by RIE.

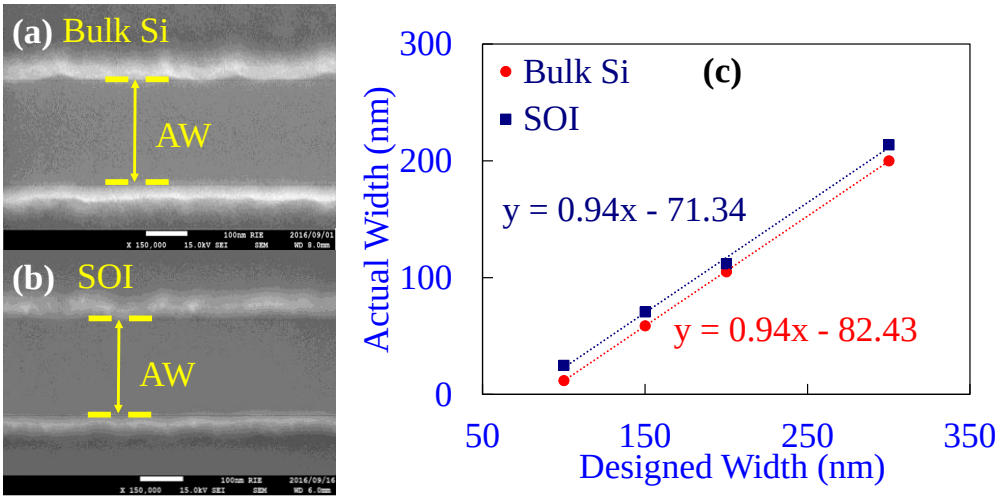

Fig. 2-4 (a, b) FESEM image of Si NW, W_{Si} = 300 nm in bulk Si and SOI substrate. (c) Variation of designed width and top actual width (AW) for bulk Si and SOI substrates. Bottom AW is larger than top AW.

20 nm thick gate oxide for MOSFET was grown by dry thermal oxidation as dry oxidation leads to high density oxide and over which SiN_x was deposited over using electron cyclotron resonance (ECR) sputtering. In a MOSFET, the gate electrode controls the current inside the channel of the MOSFET based on the voltage applied to the gate. Here, the gate electrode is a gold metallic gate in the shape of a bow-tie which can store the holes generated in the Si NW by the incident photons and can simultaneously function as an optical nanoantenna. The bow-tie structure with various designed antenna lengths (L_{ANT}) from 240 to 400 nm have been fabricated and designed channel length (L_C) is varied from 40 to 72

nm as shown in Fig. 2-5 (a, b). The bow-tie structure is patterned using EBL. After resist exposure and development, 5 nm of titanium and 50 nm of gold are deposited by electron beam evaporation at a slow rate of 0.5 nm/s to reduce surface roughness and developed photoresist is lifted off by ultrasonic agitation to fabricate the pattern.

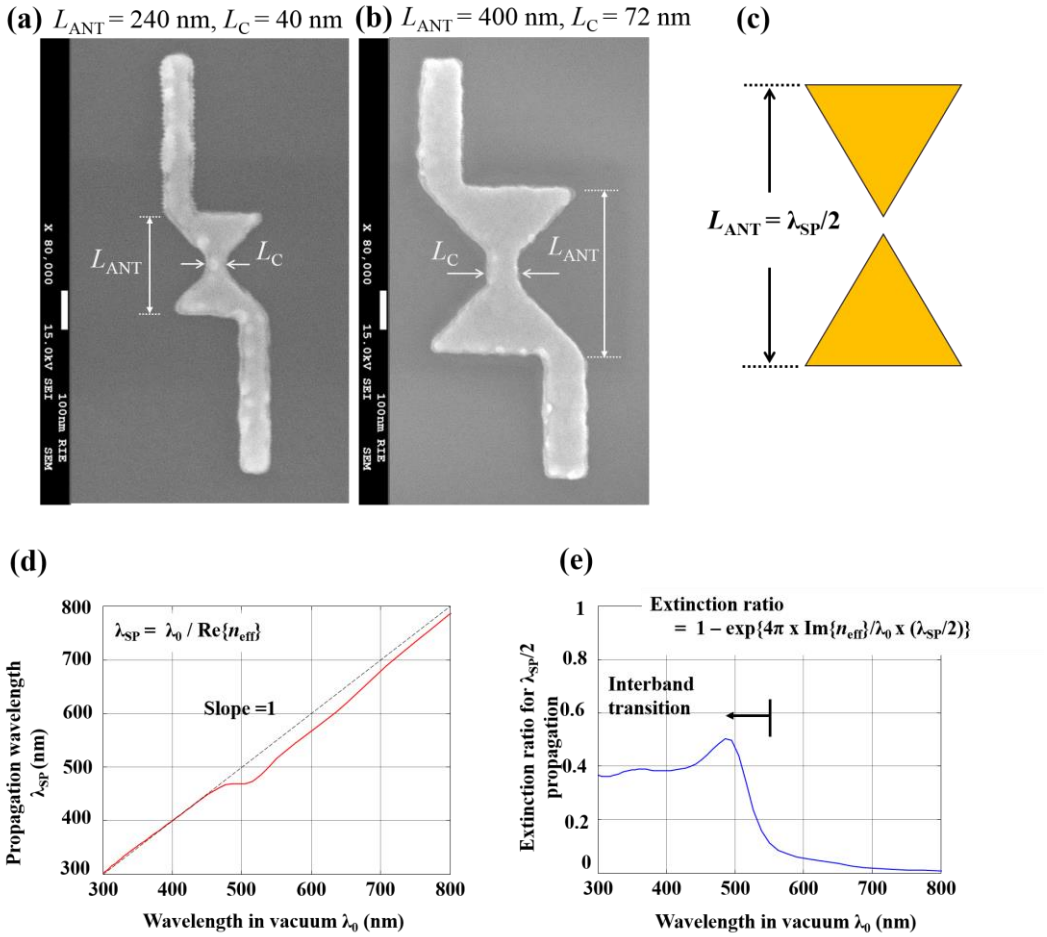

Fig. 2-5 Au bow-tie nanoantenna (a) FESEM image with L_{ANT} = 240 nm, L_C = 40 nm, (b) FESEM image with L_{ANT} = 400 nm, L_C = 72 nm, (c) nanoantenna design, (d) surface plasmon propagation wavelength in gold vs propagation wavelength in vacuum, (e) extinction ratio (loss of surface plasmon) vs wavelength of propagation is vacuum.

Titanium is used as transition metal film to improve adhesive strength between Au and SiO_2, resulting in improved stability of the fabricated nanostructure during ultrasonic agitation. As shown in Fig. 2-5 (c), the bow-tie nanoantenna is a half wavelength surface plasmon (SP) antenna, which implies that L_{ANT} is half of the surface plasmon propagation wavelength. It was observed by the FESEM images that the dimensions of the deposited gold bow-tie structures were similar to the designed dimensions and not drastically different. The wavelength of light in vacuum and that of SPs on the surface of Au is similar (slope ~ 1) as shown in Fig. 2-5 (d, e) also due to the inter-band transition in gold metal, at incident light wavelengths < 550 nm there is large absorption of surface plasmons in gold resulting in loss of SPs. Hence, the area of focus for measurement has to be in the wavelength range of 550 to 800 nm. Keeping these facts in mind the L_{ANT} of the nanoantenna is varied from 240 to 400 nm.

The effective refractive index for the SP mode along Au/vacuum interface is defined as follows considering its dispersion relation [10]

$$n_{\text{eff}} = \sqrt{\varepsilon_1 \varepsilon_2 / (\varepsilon_1 + \varepsilon_2)} \qquad (1)$$

where, ε_1 and ε_2 are dielectric constants of vacuum and Au, respectively. λ_{SP} along the Au/vacuum interface is given by

$$\lambda_{SP} = \frac{\lambda_0}{\mathrm{Re}\{n_{eff}\}} \tag{2}$$

Many metals satisfy the condition to be SP media, i.e. real part of ε_2 should be negative and its absolute value should be larger than ε_1, and imaginary part of ε_2 should be small for small propagation loss such as for Au, silver (Ag), aluminum (Al) and copper (Cu).

The propagation loss of SP for half-SP-wavelength propagation is given by

$$\text{Extinction ratio} = 1 - e^{\frac{4\pi \mathrm{Im}\{n_{eff}\}}{\lambda_0} \times \frac{\lambda_{SP}}{2}} \tag{3}$$

Fig. 2-6 shows the extinction ratio for various metals vs wavelength.

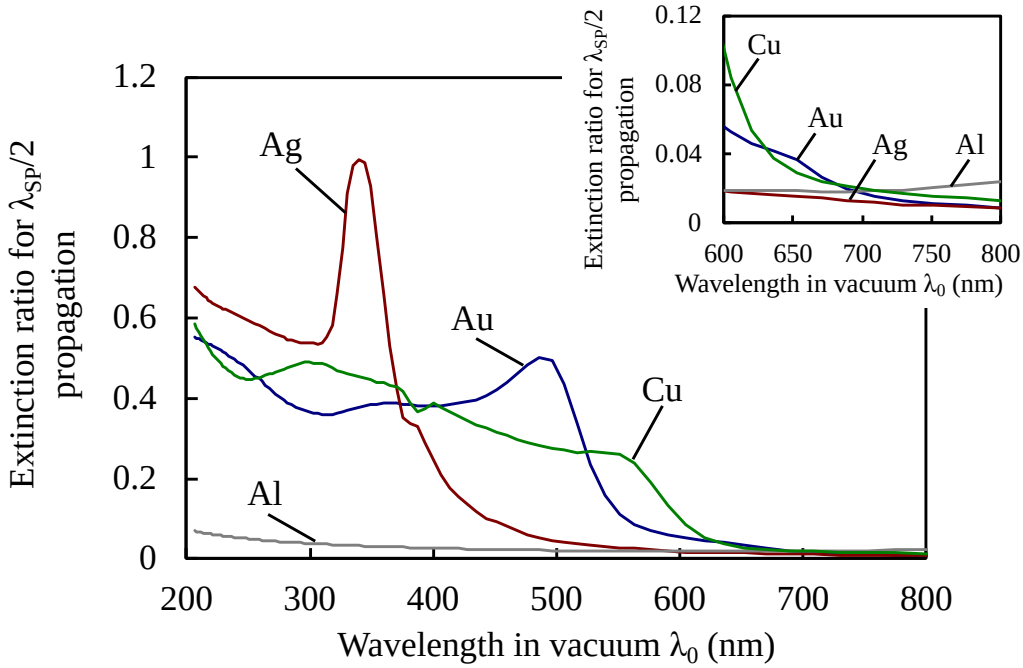

Fig. 2-6 Extinction ratio vs wavelength in vacuum. Inset is the magnified plot for the wavelength between 600 and 800 nm.

It can be observed that Ag shows the smallest extinction in the longer wavelength region, and Al is good in the shorter region and UV. Cu has higher extinction ratio in longer wavelength region compared to Ag and Au. Hence, for longer wavelength region both Au and Ag can be used as material for SP antenna. However, Au is selected for its low toxicity and being less prone to oxidation.

It is expected that when the light enters the antenna, it resonantly excites the SPs on the surface of Au bow-tie nanoantenna. Initially, the bow tie is closed, but a nanogap can be created at the junction by flowing current and inducing electromigration [11]. The excited SP leads to the improvement of electric field near the nanogap [12]. Lastly, the optical near field will generate extra carriers within the depleted Si nanowire.

In order to fabricate the contact pads for source/drain and gate terminals 20 nm of titanium and 200 nm of gold have been deposited using electron beam evaporation system at a slow rate of 0.5 nm/s. Finally, the top view of the fabricated n-type SOI MOSFET is shown in Fig. 2-7. There is a lightly doped offset region between gate and n^+ source/drain to allow the current control by the short gate in this device. The working and structure of the device will be explained in detail in next chapters.

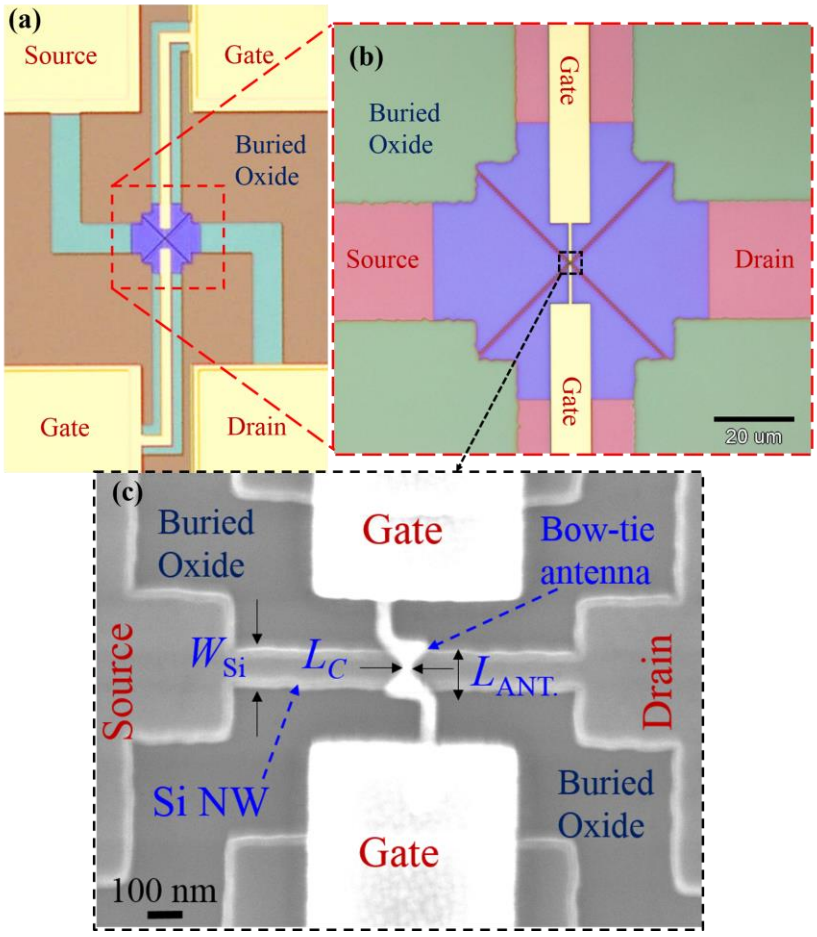

Fig. 2-7 (a) OM image of a discrete SOI MOSFET, b) Magnified OM image of the silicon region where Si NW is fabricated and (c) FESEM image of the active area of device, W_{Si} = 150 nm, L_{ANT} = 240 nm, L_C = 40 nm.

2.3 Fabrication of SOI Nanowire PN Photodiode

The pn photodiode is fabricated on the same chip along with n-channel SOI MOSFET. The device fabrication steps are similar to SOI MOSFET and are divided into 4 major steps: (1) fabricating the junctions (doping) cathode /anode, (b) Patterning of SOI to delineate Si nanowire and form active regions, (c) Opening of contact holes, (d) cathode, anode and gate contacts.

Instead of source/drain terminals of SOI MOSFET, the pn diode has anode/cathode terminals. The cathode of the pn photodiode is patterned by UV lithography and phosphosilicate spin-on-glass (PSG) is spun on the SOI. The dopant concentrations in cathode, anode are >2 x 10^{19} cm^{-3} and 1 x 10^{15} cm^{-3}, respectively. The top view of the fabricated pn photodiode is shown in Fig. 2-8. The structure of the device will be presented in the next chapters.

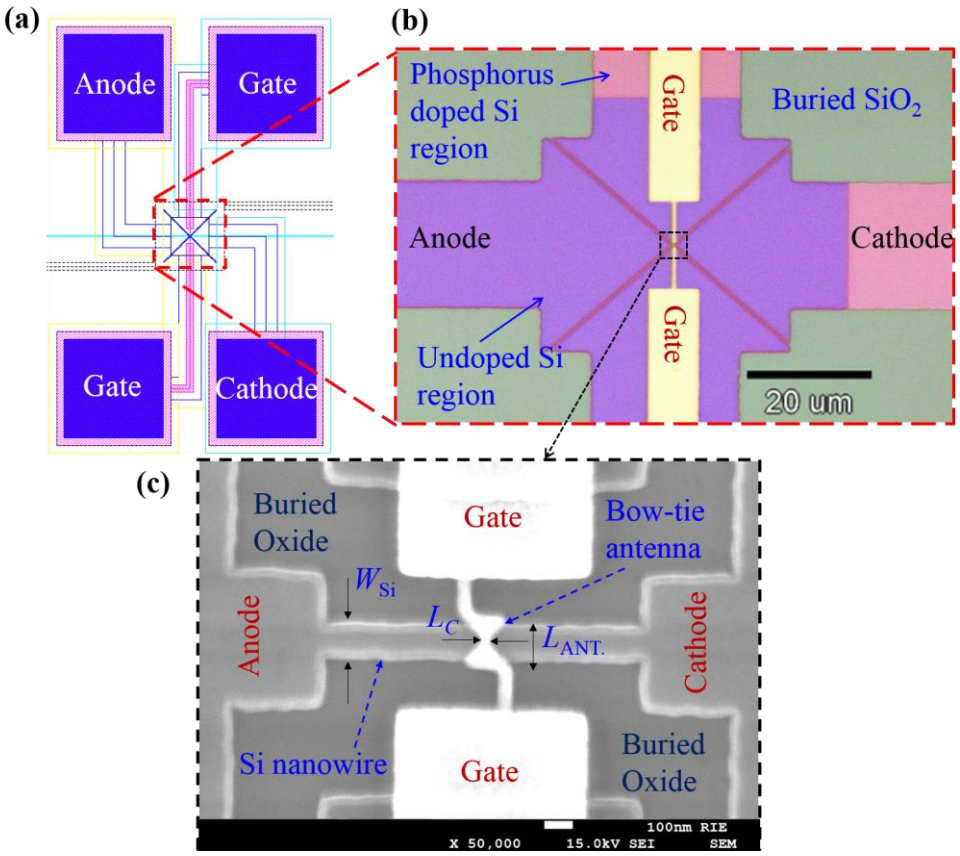

Fig. 2-8 (a) CAD layout design of a Si nanowire PD. Electrical bias to the device is given to the contact pads named as: anode, cathode and gates. The nanowire is fabricated at the center (b) Optical microscope image of the patterned top silicon layer with doped regions to form cathode and undoped region to form anode, (c) FESEM enlarged view of the active area of Si nanowire PD.

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Chapter 3

CHARACTERIZATION OF NANOWIRE PHOTODIODE WITH GOLD BOW-TIE SURFACE PLASMON ANTENNA

In the previous chapter, we have explained in detail various processes required to fabricate a pn silicon-on-insulator (SOI) nanowire photodiode (PD) with gold bow-tie surface plasmon nanoantenna. It is expected that when the light enters the nanoantenna, it resonantly excites the surface plasmons on the surface of gold bow-tie nanoantenna. Initially, the bow tie is closed, but a nanogap can be created at the junction by flowing current and inducing electromigration [1]. The excited surface plasmons lead to the improvement of the electric field near the nanogap [2]. Lastly, the optical near field will generate extra carriers within the depleted Si nanowire.

In this chapter, we evaluate experimentally the spectroscopic response of the SOI nanowire PD before and after the creation of nanogap in the bow-tie nanoantenna. Also, we present the electromagnetic simulations showing the effect of bow-tie nanoantenna on illumination.

3.1 Device Structure

A schematic diagram of the SOI nanowire PD is shown in Fig. 3-1. The device has designed nanowire width (W_{Si}), antenna length (L_{ANT}) and channel length (L_C) of 150, 240 and 40 nm, respectively. The thicknesses of buried oxide, SOI and gate oxide are 400, 60 and 20 nm, respectively. The doping concentration in cathode (n^+) is >2 x 10^{19} cm^{-3} and the doping concentration anode and substrate (p^-) is 1 x 10^{15} cm^{-3}. The gate electrode which is in shape of a bow-tie nanoantenna is fabricated by deposition of 5 nm of titanium and 50 nm of gold. There is an offset region present between the gate and the cathode/anode. The nanoantenna is in the shape of bow-tie because bow-tie structure has small intersectional area between

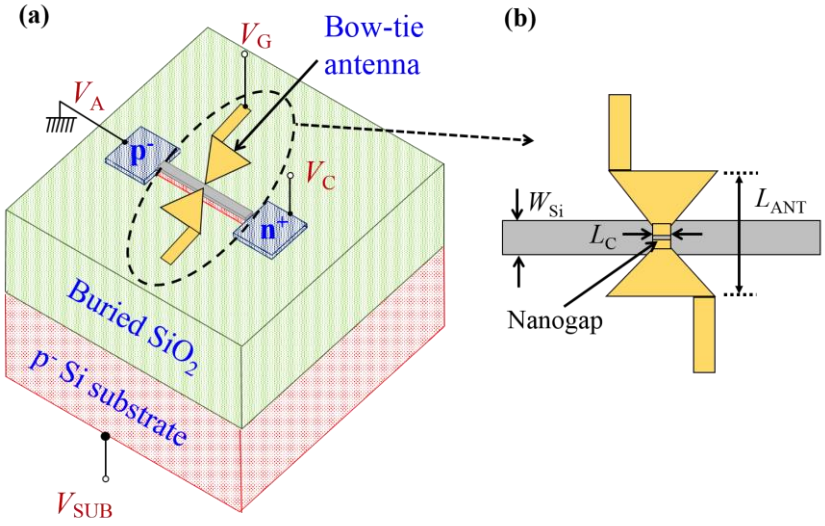

Fig. 3-1 (a) Schematic diagram of SOI nanowire PD with gold bow-tie nanoantenna. Thicknesses of buried oxide, SOI and gate oxide are 400, 60 and 20 nm, respectively, (b) Enlarged image of bow-tie nanoantenna in fabricated SOI PD.

the antenna and the nanowire PD, which will minimize the increase in the parasitic capacitance. In case of the SOI MOSFET single-photon detector, the small intersectional area realizes localized storage of photogenerated holes and large shift of the threshold voltage per hole. Also due to the simplicity of fabrication of bow-tie antenna it is preferred. In the spectroscopic measurement the applied gate voltage V_G is kept at 0 V. The photodiode is operated under reverse bias with cathode voltage V_C given is 1 V and anode terminal is grounded. Substrate voltage, V_{SUB} applied is -20 V. The cathode current is measured at 300 K and the incident wavelength is varied from 400 to 800 nm.

3.2 Measurement Setup

The block diagram of the measurement system is shown in Fig. 3-2.

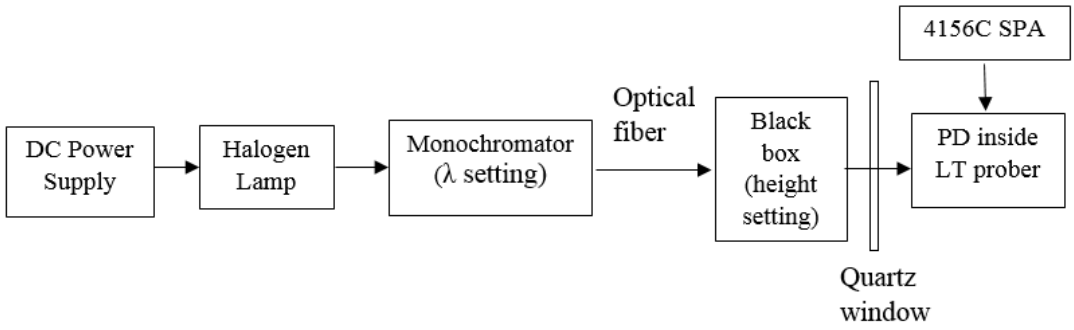

Fig. 3-2 General block diagram of the measurement setup for wavelength dependency of effective light detection area in SOI nanowire photodiode.

DC power supply= Constant voltage 11.0 V. Monochromator: No polarization filter, three neutral density filters (all 100% transmission).

The main measurement system utilized in this work consists of equipment listed below and shown in Fig. 3-3.

1) Low-temperature prober Grail21-205-6-LV-R from Nagase Techno-Engineering Co., Ltd.
2) Compact monochromator H-20VIS from Horiba Jobin Yvon with halogen lamp as a light source.
3) Fiber optics for light guide.
4) Optical transfer system as an interface between light source and low-temperature prober.
5) Semiconductor parameter analyzer (SPA) 4156C from Agilent Technologies for DC electrical measurement and biasing.
6) ATAGO MIC 7 wavelength controller.

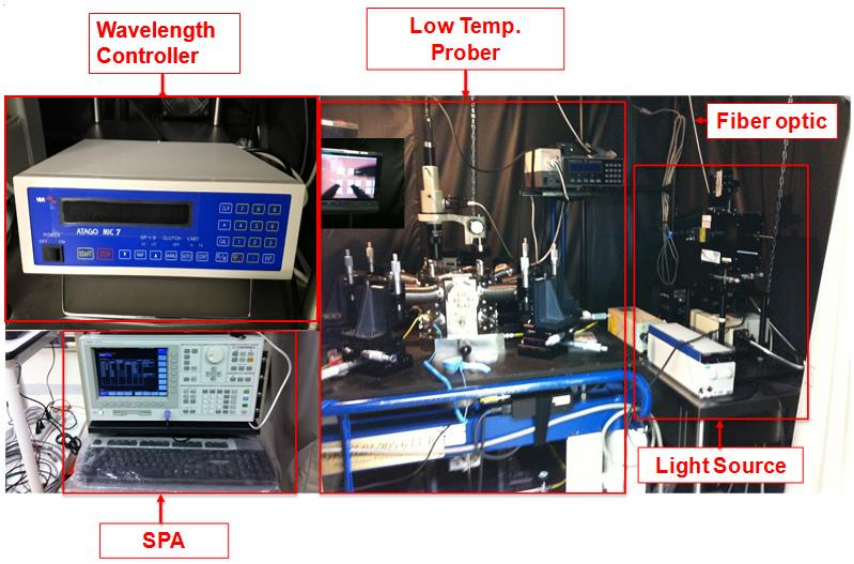

Fig. 3-3 Measurement system consisting of a low-temperature prober, light source, semiconductor parametric analyzer (SPA).

In this experiment, the sample temperature is kept at 298K, the probe chamber is evacuated by a turbo pump to 10^{-2} Pa. Temperature controller (Cryocon 32) is used to control the temperature.

The low-temperature prober with three main parts, as shown in Fig. 3-4, did not operate at low temperature in this experiment. The upper part is a measurement chamber with a sample stage and 6 probe needles, with gold tips. Electrical input to these needles are given from outside the measurement chamber by tri-axial connecters. From the connecters, two to six tri-axial cables, depending on the devices being measured and the measurement conditions, are connected to the semiconductor parameter analyzer (4156C SPA). The temperature inside the chamber is controlled by external temperature controller. Two temperatures: temperature of the sample stage and temperature of the refrigeration is displayed in the controller display and can be controlled based on the measurement conditions. The middle part is an area for the refrigerator driven by an external helium compressor.

In order to allow light illumination from outside, the upper part of the measurement chamber is covered by transparent quartz glass window. This window also allows us to observe the sample by a digital microscope in order to precisely place the probes on the sample pads.

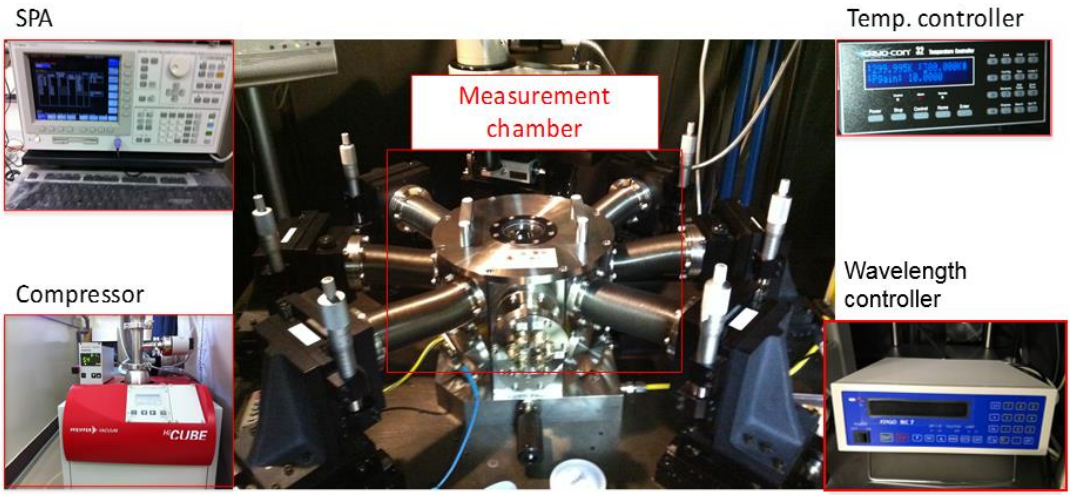

Fig. 3-4 Low-temperature prober and supporting equipment.

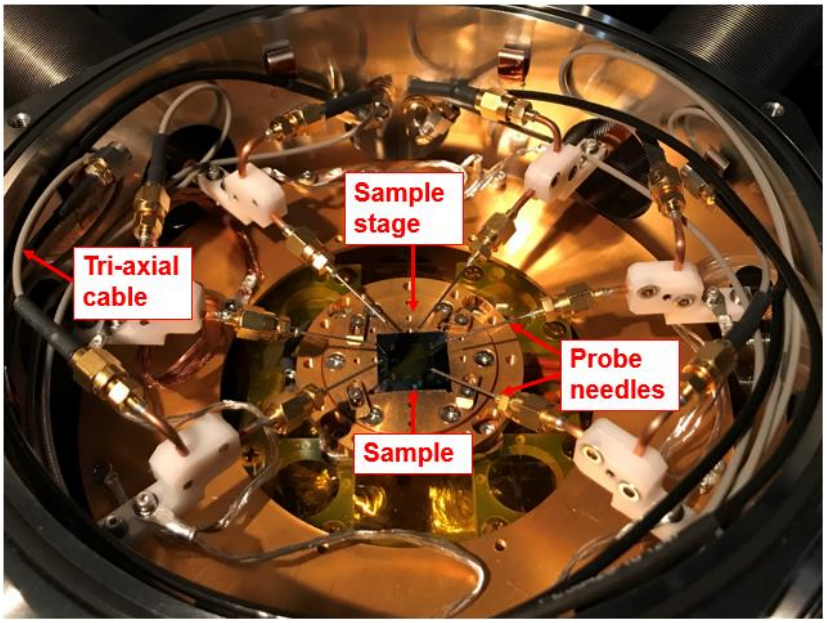

Fig. 3-5 Sample on stage with six needles probers. The sample stage is used not only as the sample holder but also as a back gate terminal.

The device is placed on the sample stage in the measurement chamber as shown in Fig. 3-5. The sample stage is also used as a substrate

(back gate) terminal. Through the quartz glass window, a monochromatic light in the visible wavelength is illuminated.

3.3 Experimental Result and Discussion

3.3.1 Cathode current dependence on Substrate Voltage

We measured dependence of cathode current (I_C) on V_{SUB} at 300 K. Fig. 3-6 shows the I_C-V_{SUB} characteristics for photodiode with L_{ANT}, L_C and W_{Si} of 240, 40 and 150 nm, respectively under dark and illuminated conditions (illumination by 535 nm LED light, intensity was 2.9 mW/cm^2).

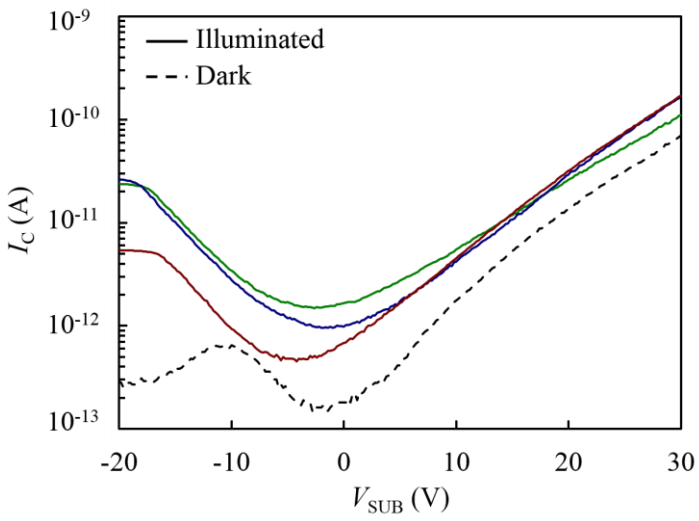

Fig. 3-6 I_C-V_{SUB} characteristics at V_C = 1V and V_G = 0 V. The solid lines represent illuminated condition. Green color is for green LED light source (λ = 535 nm), blue color for blue LED light source (λ = 475 nm), red color for red LED light source (λ

For all cases, I_C increases as V_{SUB} increases, because the inversion layer at the top silicon-buried SiO_2 interface extends from the n^+ cathode to the anode region. At the same time, depletion region above the inversion layer becomes wider, resulting in the larger photocurrent (I_C under illumination minus dark I_C). Although the net photocurrent is smaller for negative V_{SUB}'s, the illuminated-dark current ratio is large, due to the cutoff of the dark current. Under this condition, enhancement of the photocurrent by the presence of the antenna is appreciable.

3.3.2 Nanogap Formation in Bow-Tie Nanoantenna

Fig. 3-7 (a) shows the circuit diagram of breaking bow-tie nanoantenna by controlled passage of current for formation of nanogap. The current flowing through the bow-tie nanoantenna is monitored. As shown in Fig. 3-7 (b) the resistance at the onset of current flow (before breaking) is calculated to be around 60 GΩ at 40 mV. As the voltage across the antenna increases, the current also increases. At sufficiently high voltage, the current suddenly drops indicating the breaking of junction by electromigration. The resistance calculated after breaking the bow-tie nanoantenna is more than 2 TΩ.

The change in tunnel resistance reflects the change in the nanogap size. Quantitatively, the tunnel conductance G_t is exponentially dependent

on the size of the nanogap *s* formed at the center of the bow tie, and can be calculated by the equation $G_t = G_{t0} \exp -\alpha\sqrt{\Phi_S}$, where α is a characteristic length of tunneling (=1.025 $Å^{-1}$ $eV^{-1/2}$), Φ is the woork function of Au (=4 eV), and G_{t0} is typically 0.8 S [3]. For tunnel resistances of 60 GΩ and 2TΩ, the nanogap sizes are 1.2 and 1.4 nm, respectively.

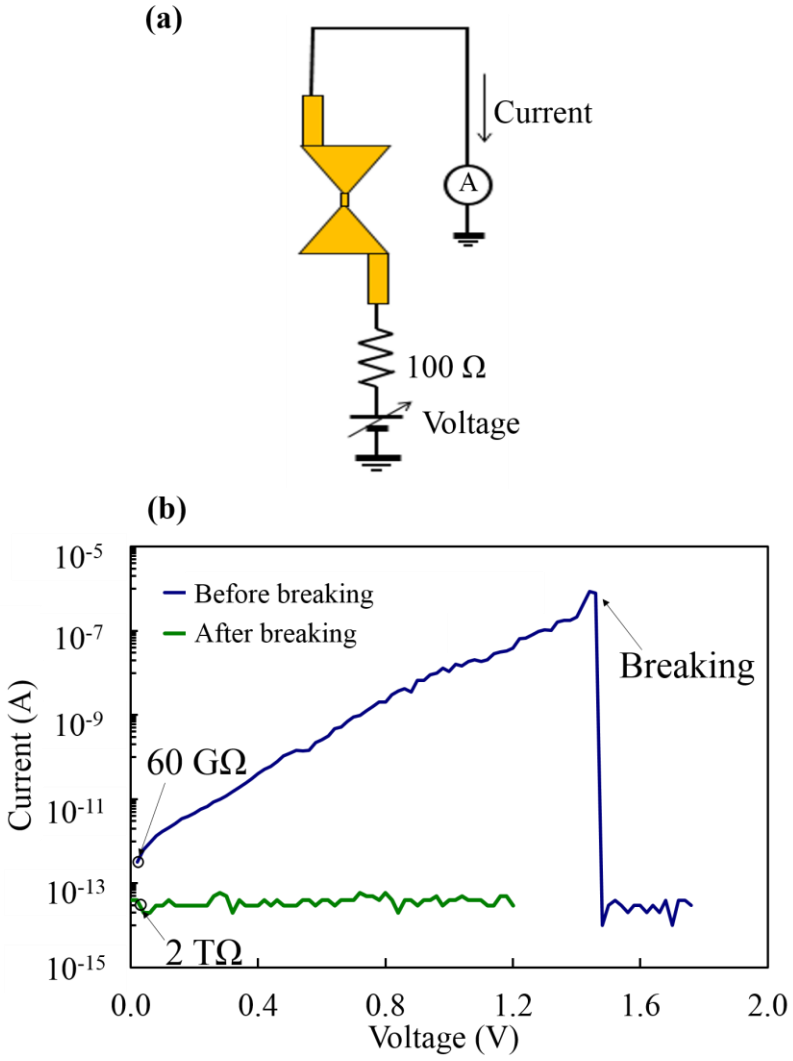

Fig. 3-7 Break junction for nanogap formation, (a) Circuit diagram of break junction (b) Current vs. voltage curves before and after nanogap formation.

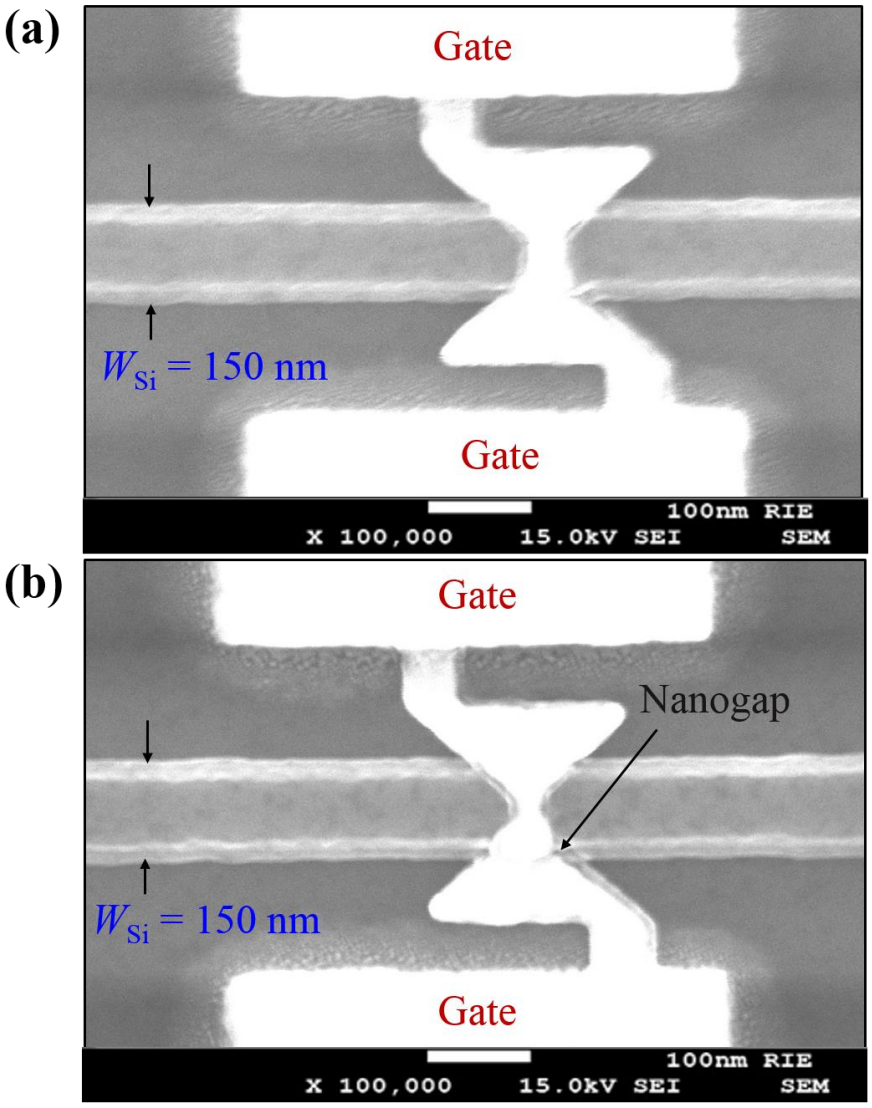

Fig. 3-8 FESEM images, (a) Before breaking junction L_{ANT} = 240 nm, L_C = 52 nm, (b) After breaking junction L_{ANT} = 240 nm, L_C = 40 nm.

FESEM images before and after junction breaking in bow-tie nanoantenna is shown in Fig. 3-8. From Fig. 3-8 (b) it can be observed that the nanogap is formed at the junction of the bow-tie antenna since the current density will be higher at the junction in comparison to the rest of

the nanoantenna. However, the nanogap is far from the nanowire and not directly above the nanowire.

3.3.3 Effective Detector Area of Photodiode

Fig. 3-9 shows the effective detector area (A_{Eff}) of the SOI PD with respect to the wavelength, before and after breaking the bow-tie nanoantenna to create nanogap. A_{Eff} is given by equation (1).

$$AEff = \frac{IPh}{e} \Big/ \frac{POpt}{hv} \qquad (1)$$

Where, I_{Ph}, P_{Opt}, e, h, and v are photocurrent, optical power per unit area, electron charge, Plank's constant, and light frequency, respectively.

A_{Eff} shows some change after the junction breaking, probably because the nanogap is not properly formed. However, 50 % enhancement of A_{Eff} is observed for longer wavelengths. The nanoantenna effect is usually localized, however the effective detector area of the SOI nanowire PD includes the contribution of the depleted area. Since in the device the depleted area extends all over the device, the localized antenna effect is not showing and distinct effect in the measurement results.

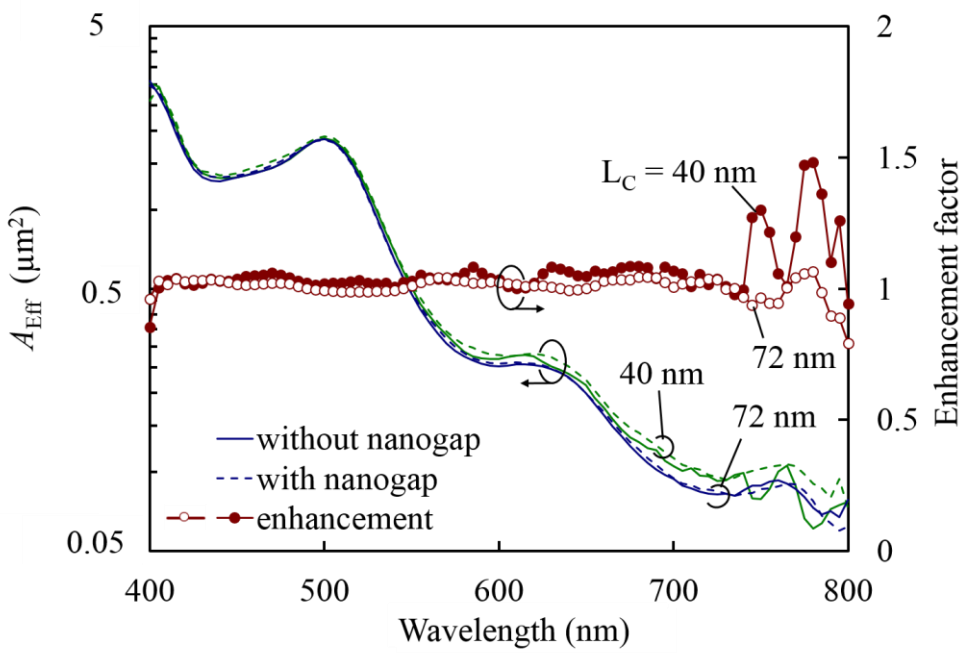

Fig. 3-9 Effective detector area vs. wavelength. W_{Si}= 150 nm.

3.4 Simulation Results and Discussion

Using the three-dimensional (3D) finite difference time domain (FDTD) method, the near-field profile in the gold bow-tie antenna had been simulated. It is a concrete method of calculating and estimating Maxwell's equations in dispersive media. Silicon, gold, and titanium were specified by frequency-dependent permittivity ε (ω) [4].

The FDTD simulations were carried out using the FullWAVE (RSOFT, Inc). The quasi-plane wave irradiates the bowtie antenna on the SOI PD.

The incident plane wave is linearly polarized light along the antenna length direction with wavelength of λ = 720 nm, and propagates along the depth direction of SOI PD. In this paper, the results in the cases with and without the gap are compared to clarify the field concentration effect of surface plasmon mode at the gap. The calculation domain with 1000 x 1000 x 630 nm^3 (2-nm-grid) was considered, but the length of SOI channel and the planar size of BOX/Si substrate are infinite using perfectly matched layer (PML) as an absorbing boundary condition.

Fig. 3-10 shows the calculated electric field profile, $|E|^2$, of the gold bow-tie with L_{ANT} = 240 nm, without and with nanogap of 10 nm at the incident wavelength of 720 nm. The wavelength is near to surface plasmon resonance wavelength of the bow-tie nanoantenna with L_{ANT} = 240 nm. As seen from Fig. 3-10 (a) electric field is concentrated at the neck of the bow-tie. By creating a nanogap the concentration of electric field is increased, and the electric field with higher intensity is distributed inside the nanoantenna shown in Fig. 3-10 (c). Comparing the cross-sectional views in Fig. 3-10 (b, d) the intensity of electric field in the case with gap is much larger resulting in the enhancement of quantum efficiency. Eventually, the cathode current would be increased as a result.

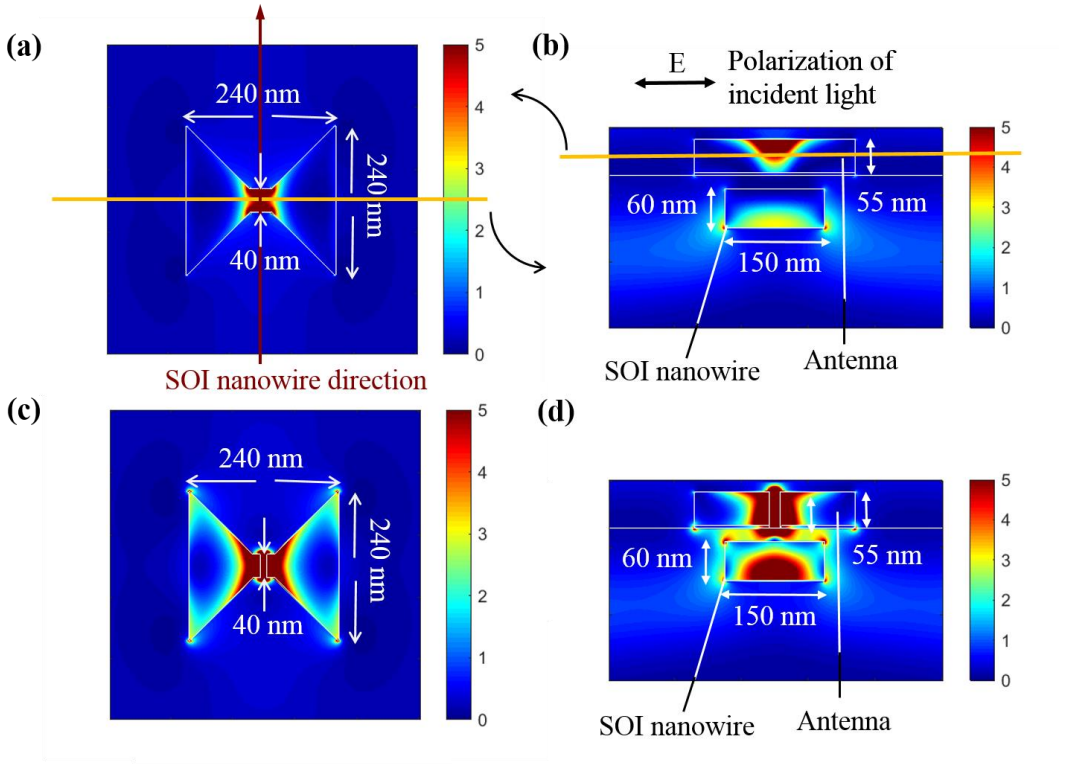

Fig. 3-10 Simulated electric field profile, $|E|^2$, on gold bow-tie nanoantenna L_{ANT} = 240 nm, L_C = 40 nm, W_{Si} = 150 nm illuminated by incident light with the wavelength of 720 nm, (a) top view without nanogap, (b) cross-sectional view without nanogap, (c) top view with nanogap = 10 nm (d) cross-sectional view with nanogap = 10 nm.

The presence of nanogap of 10 nm in the neck of bow-tie nanoantenna increases the quantum efficiency in the specified region with 200 x 150 x 60 nm^3 (length x width x depth) in SOI nanowire by 50%. The presence of nanogap of 10 nm in the neck of bow-tie nanoantenna increases the quantum efficiency (QE) in the specified region with 200 x 150 x 60 nm^3 (length x width x depth) in SOI nanowire by more than 50% as shown in Fig. 3-11. It shows the simulated effective detector area of the SOI PD with

bow-tie nanoantenna with and without 10 nm nanogap versus wavelength. In Fig. 3-9 there are two peaks compared to one peak in FDTD simulation (Fig. 3-11) because in FDTD simulation ideal bow-tie structure is simulated. However, in fabricated bow-tie structure, fabrication process variability may have resulted in two peaks.

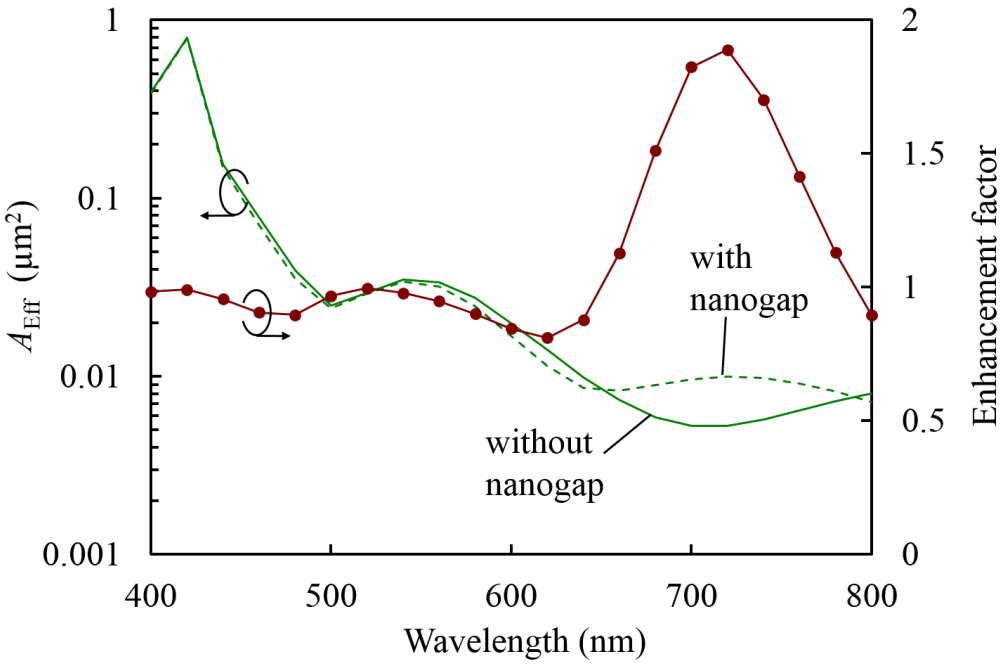

Fig. 3-11 A_{Eff} vs incident wavelength with and without nanogap in bow-tie nanoantenna. L_{ANT} = 240 nm and W_{Si} = 150 nm.

The position of nanogap also affects the electric field profile generated inside the nanowire and as the nanogap is shifted from the center of the bow-tie, A_{Eff} is decreased as shown in Fig. 3-12. Fig. 3-13 shows Ag bow-tie antenna has a higher sensitivity compared to Au, however, Au is selected for its low toxicity and being less prone to oxidation.

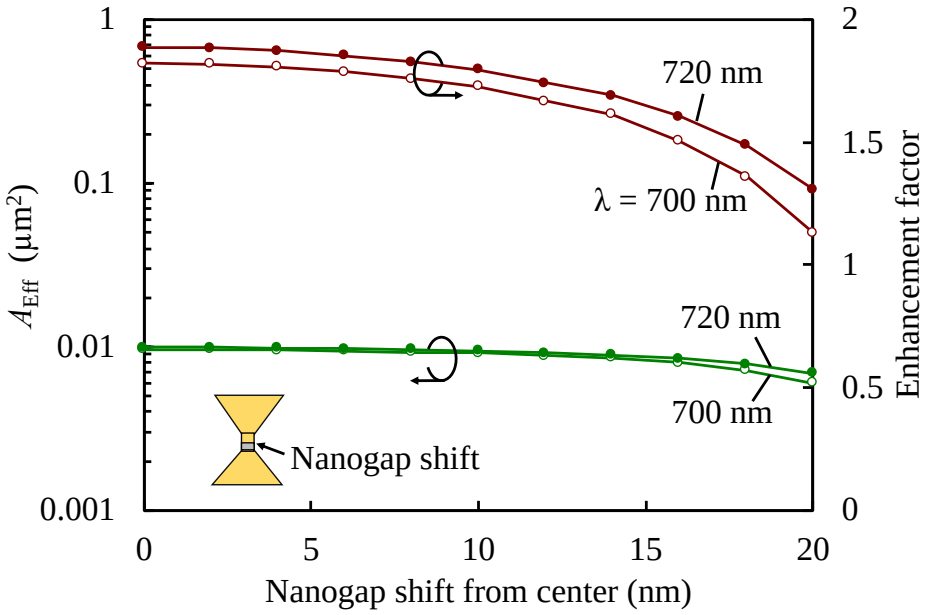

Fig. 3-12 Effect of nanogap shift from the center of bow-tie antenna on the A_{Eff} of SOI PD at incident wavelengths of 700 and 720 nm.

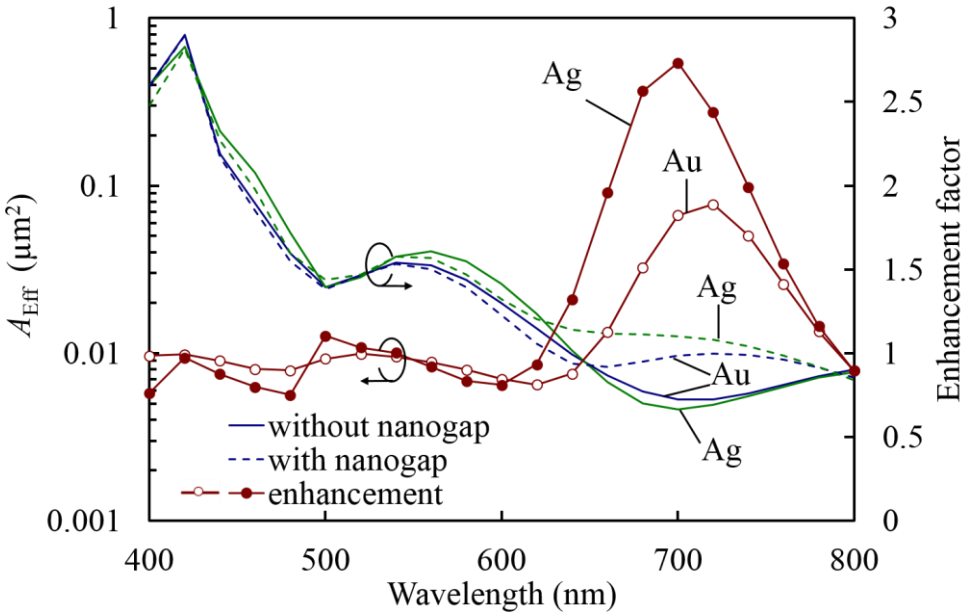

Fig. 3-13 A_{Eff} vs incident wavelength with and without nanogap for Au and Ag bow-tie nanoantenna. L_{ANT} = 240 nm and W_{Si} = 150 nm

3.5 Conclusion

The spectroscopic response of SOI nanowire photodiode with gold bow-tie nanoantenna has been measured *for the first time.* The nanogap in the bow-tie nanoantenna was successfully created by the process of electromigration. High current density at the junction of the bow-tie by controlled passage of external current resulted in drifting of gold atoms to create a nanogap of size ~ 1.4 nm. Subsequently, the effect of nanogap on the effective detector area of the SOI nanowire PD was investigated. It is observed that at incident $\lambda > 750$ nm there is enhancement of detector area (upto 50 %). Simulation was done to show the confinement of electric field due to the presence of nanogap (size = 10 nm) in bowtie antenna. The electric field is confined at the edges and around the nanogap of the antenna. The resulting external quantum efficiency was calculated and 50 % enhancement is observed at resonant $\lambda = 720$ nm in comparison to without nanogap bow-tie antenna.

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Chapter 4

CHARACTERIZATION OF NANOWIRE MOSFET PHOTON DETECTORS

As mentioned in previous chapter, in-order to detect the weak light in scientific instruments and measuring devices, single-photon detectors like photomultiplier tubes (PMT) and avalanche photodiode (APD) are widely used. However, they have some disadvantages like high operational voltages and high dark counts [1].

Recently, it has been reported that the silicon-on-insulator (SOI) metal-oxide-semiconductor (MOS) field-effect transistor (FET) could function as a single-photon detector at room temperature, performing photon-number resolution, dark counts (~10^{-2} s^{-1}) many orders of scale lesser than that of traditional APD and smaller operating voltage less than few volts [2-4]. In this device, when light is incident carriers are generated in the channel and holes are stored below the negatively biased gate. The electrons drift to the back channel and modulate the bottom-channel electron current, stepwise reflecting the number of stored holes. However, the quantum efficiency of the SOI MOSFET photon detector is low compared to the APDs due to the unavailability of larger silicon volume

for light absorption. The quantum efficiency and effective light receiving area can be improved by use of an optical antenna [5]. In this chapter we present the measurement of SOI MOSFET photon detector with metal gate in shape of metal strip and bow-tie nanoantenna.

4.1 Device Structure of Nanowire MOSFET with Upper and Lower Gates

Fig. 4-1 shows the cross-section of an SOI MOSFET which shows single photon sensitivity. The SOI MOSFET photon detector has a double-gate structure with a short lower gate (LG) and a long upper

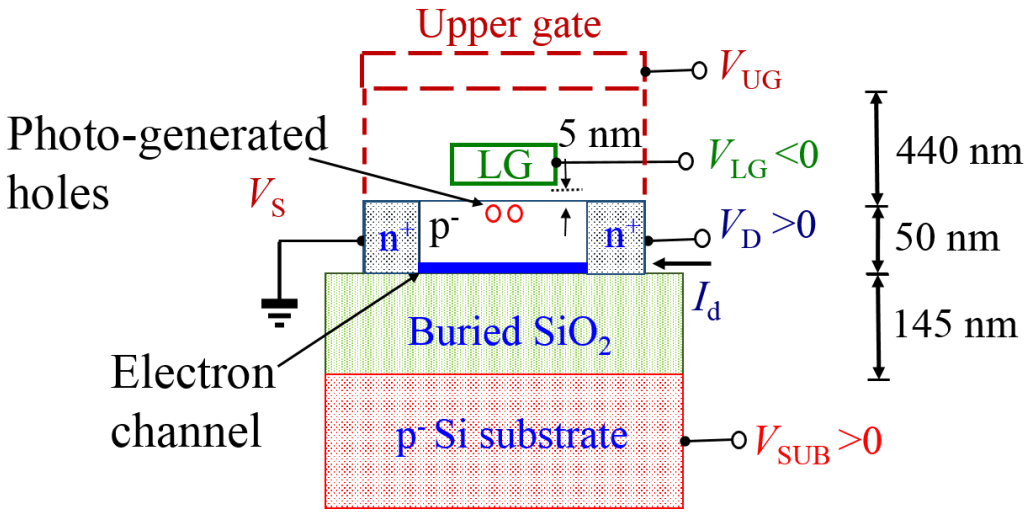

Fig. 4-1 Cross-sectional view of SOI MOSFET with UG and LG. The thicknesses of the buried oxide, SOI, LG oxide, and insulator below the UG are 145, 50, 5 and 440 nm, respectively.

gate (UG) covering the p^--doped offset area between LG and n^+-doped source/drain. The channel length of the device is 80 nm and channel width is 120 nm. In the present design, photo-generated holes are stored below the lower gate (LG) when $V_{LG} < 0$ is biased. A back electron channel, can be formed which can be applied as an electrometer, by applying a higher substrate voltage ($V_{SUB} > 0$). Photogeneration of holes and their recombination will modify the electron current resulting in pulses that can be detected.

4.2 Measurement Setup

The equipment used for measurement is explained in Chapter 3, section 3.2, however lock-in amplifier and current pre-amplifier are also used in these measurements. A comprehensive setup is shown in Fig. 4-2. Instead of using monochromator with wavelength range from 400 to 700 nm, fixed incident LED light source with $\lambda = 535$ nm is used with varying light intensities.

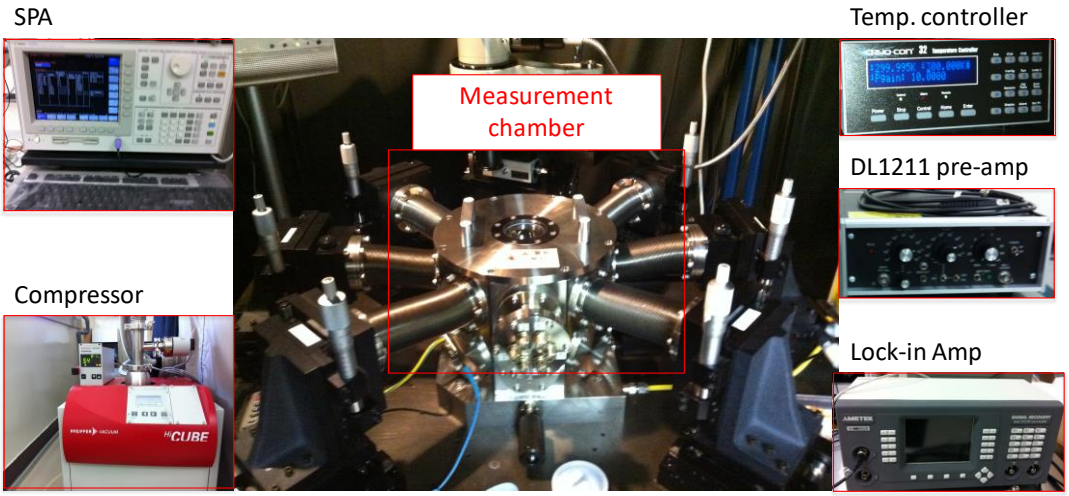

Fig. 4-2 Measurement system consisting of a low-temperature prober, light source, semiconductor parametric analyzer, lock-in amplifier and current pre-amplifier

4.3 Experimental Result and Discussion of SOI MOSFET with Upper and Lower Gate

Fig. 4-3 shows usual drain current waveforms for distinctive quantities of light intensity at the wavelength of 535 nm. Reference current is attuned to 1 nA by appropriate biasing of $V_{G.}$ Every resultant waveform is altered for clearness. The various bias, such as $V_{LG,}$ V_{SUB}, V_{UG} and V_D are -1, 1, 2.05 and 0.05 V respectively. It can be observed that the photo-generated holes modify the drain current forming pulses of distinct levels. Each level corresponds to the number of collected holes below the upper

gate, keeping the functioning state biased to V_{LG}< 0 and V_{SUB}> 0, so that the electrons drift in the bottom channel.

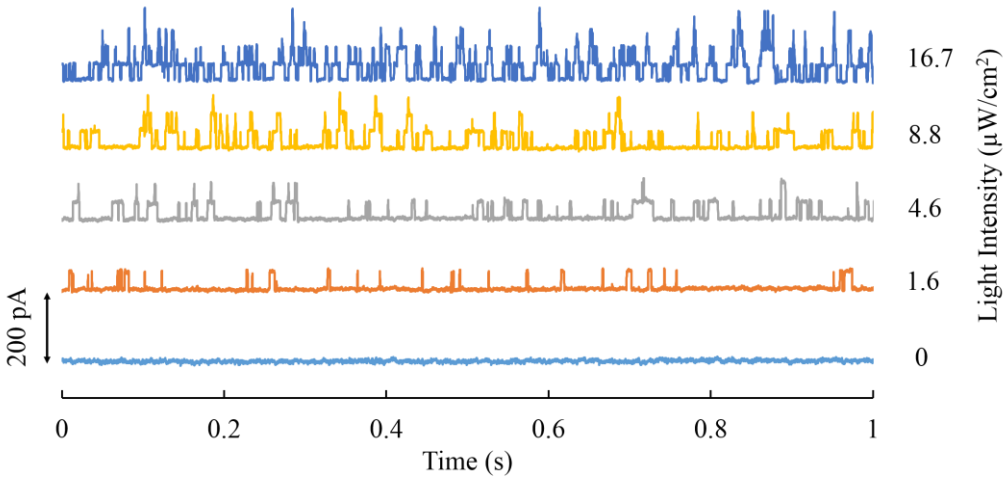

Fig. 4-3 Typical drain current waveforms at 300 K for different levels of light intensity at a wavelength of 535 nm. Baseline current is about 1 nA and each waveform is shifted for visual clarity. V_{LG}, V_{SUB}, V_{UG} and V_D are -1, 1, 2.05 and 0.05 V, respectively.

It displays that the pulse count rises as the light intensity rises. Furthermore, distinctive pulses can be seen clearly, suggesting that a distinctive number of holes are accumulated under the LG. The first, second, third, and fourth levels correspond to 0, 1, 2 and 3 stored holes, respectively. The bias voltages are < 1 V, much below than that of PMTs and APDs.

Fig. 4-4 displays the histograms of drain current for various light intensities (a) Dark, (b) 1.6 μW/cm^2, (c) 4.6 μW/cm^2, (d) 8.8 μW/cm^2 and (e) 16.7 μW/cm^2 with different V_G to maintain the reference drain current at 1 nA. The dotted symbols are obtained data and solid red lines are fitting

curves with Gaussian distribution. The peaks starting from left to right in each graph relate to zero, one, two, and three trapped holes.

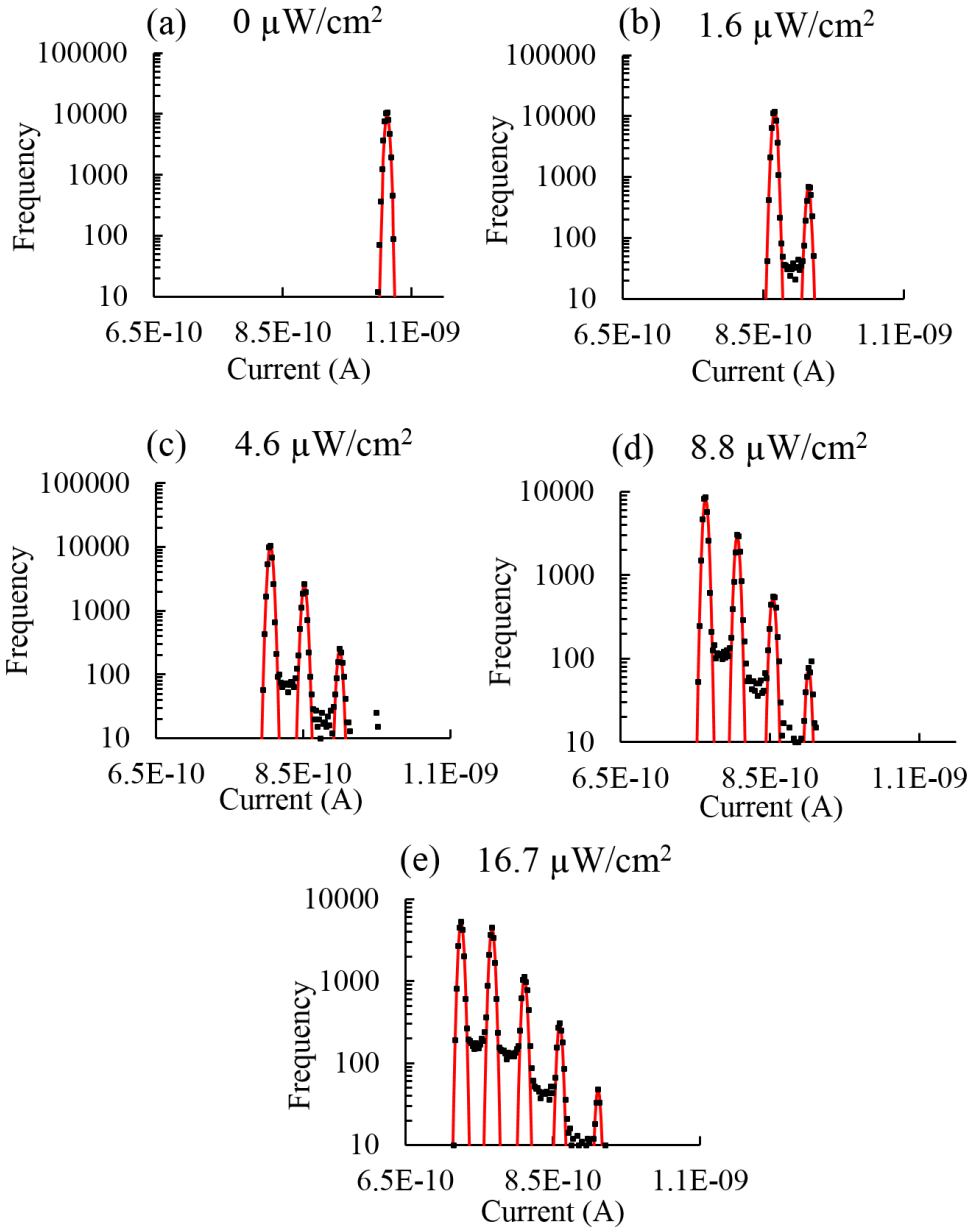

Fig. 4-4 Histograms of digitized drain currents corresponding to Fig. 4-3. The first, second, third, and fourth peaks from left in each graph correspond to zero, one, two, and three trapped holes, respectively. Data acquisition time period and time step are 2.45 s and 49 μs, respectively, and 50000 (2.45 s/49 μs) data points (current values) are classified into bins with a width of 2 pA.

Note that the frequency in y-axis is the count of data points in a bin width of 2 pA out of 50000 points in the entire current range and time period as explained in the caption of Fig. 4-4. When the intensity of light falling on the photodetector rises, it results into enhanced creation of holes. Consequently, the likelihood of holes getting stored under the LG surges, ensuing in larger peaks (more peak height) for extra trapped holes. These peaks are visibly separated from each other, which indicates that the sensor is able to determine the number of stored holes even before the recombination takes place. It can be observed that the SOI MOSFET is operating like single photon detector at normal temperature.

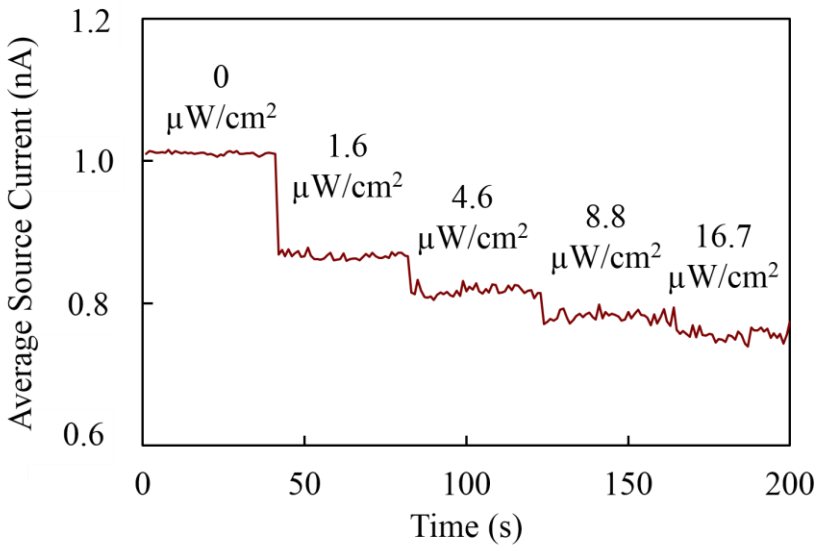

Fig. 4-5 Average source current at different light intensities. Incident wavelength is 535 nm.

The change of average source current at different light intensities is shown in Fig. 4-5. As light intensity is increased the average source current is decreased probably due to the change of effective V_{SUB}.

It can be clearly understood by the energy band diagram shown in Fig. 4-6. In the p-type substrate, large relative increase in electrons causes the diffusion to the deep substrate, then electrons recombine with holes there. This diffusion is balanced by the internal potential difference, resulting in the reduction of the effective V_{sub}. The change is effective V_{sub} affects the drain current.

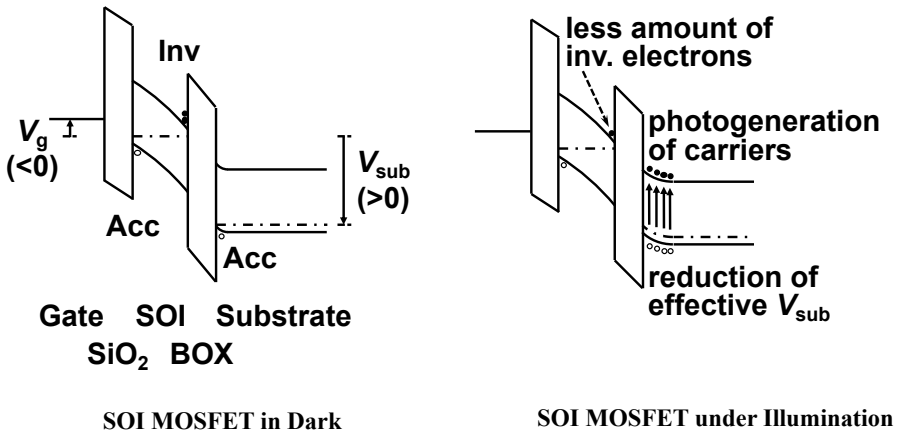

Fig. 4-6 Energy band diagram of SOI MOSFET under dark and illumination condition.

In general the QE of such photon detector is less mainly because the gold upper gate (UG) is concealing the whole working area of the device. The device is only able to obtain the dispersed light from lines for electrical

connection and probing pads which are placed on equal level with the UG, and perhaps can be increased by changing the UG with a see-through type.

Also, the operational area and QE may get increased by the application of a surface plasmon antenna. It will increase the functional area, on the other hand the narrowing of Si channel (i.e., small L and W) should be done to increase the lone hole sensitivity. However, as a result the efficiency and the transit rate of these photo-generated holes might be of some concern.

4.4 Device Structure of Nanowire MOSFET with Gold Bow-tie Antenna

A representative diagram of the SOI nanowire MOSFET is shown in Fig. 4-7. The device has designed nanowire width (W_{Si}), antenna length (L_{ANT}) and channel length (L_C) of 150, 240 and 40 nm, respectively. The thicknesses of buried oxide, SOI and gate oxide are 400, 60 and 20 nm, respectively. The doping concentration in source/drain (n^+) is > 2 x 10^{19} cm^{-3} and the doping concentration in substrate (p^-) is 1 x 10^{15} cm^{-3}. The gate electrode which is in shape of a bow-tie nanoantenna is fabricated by deposition of 5 nm of titanium and 50 nm of gold.

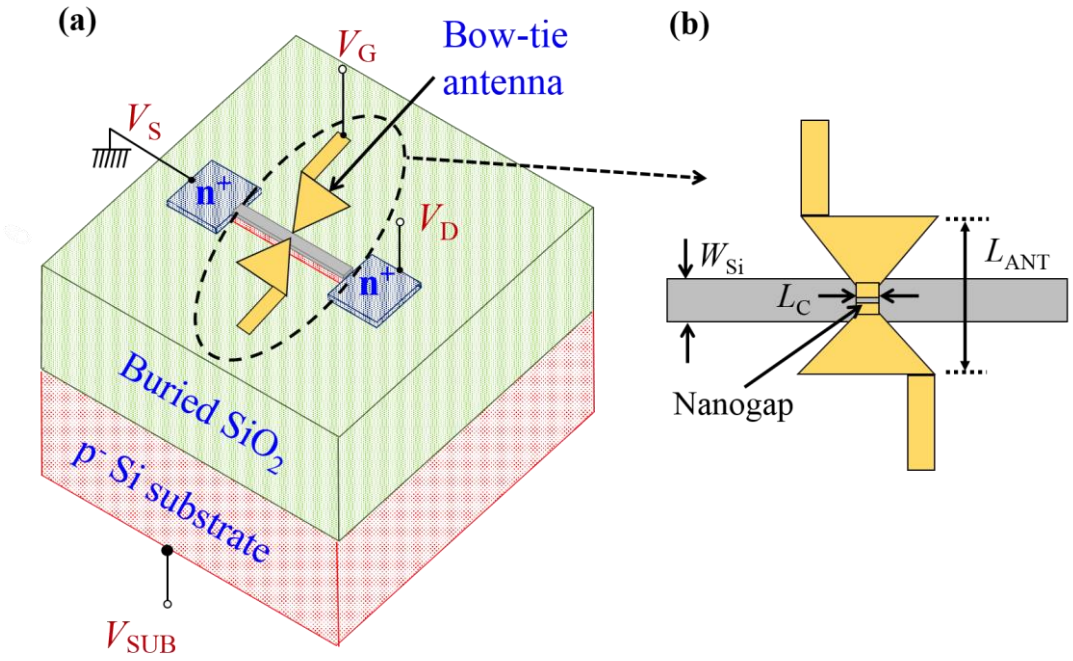

Fig. 4-7 (a) Schematic diagram of SOI nanowire MOSFET with gold bow-tie nanoantenna. Thicknesses of buried oxide, SOI and gate oxide are 400, 60 and 20 nm, respectively, (b) Enlarged image of bow-tie nanoantenna.

There is a lightly doped offset region present among gate and the n^+ source/drain to allow the current control by the short gate in this device.

4.5 Experimental Result and Discussion of Nanowire MOSFET with Bow-tie Antenna

4.5.1 Nanowire width dependence on Threshold Voltage of the SOI Nanowire MOSFET

The threshold voltage (V_{TH}) is a essential factor for MOSFET developing and classification [6–12]. This factor, shows the beginning of substantial drain current flowing between the source and drain. It can be defined in various ways [13, 14], however it can be defined as the gate voltage bias that brings conversion of weak inversion to strong inversion inside the channel of MOSFET. Various formulae and ways can be used to estimate the value of V_{TH} [15-23]. Majority of the current methodologies to estimate the value of V_{TH} rely mainly on measuring the fixed drain current vs gate voltage (I_D–V_g) behavior of transistor. Majority of such I_D–V_g techniques employ strong inversion area, on the other hand just few techniques take in account the weak inverted area of the channel. Estimation is generally carried out by biasing at small V_D because the MOSFET should be functioning in the linear region.

The method used in our characterization to calculate V_{TH} is known as ‘extrapolation in the linear region method’ (ELR). ELR is possibly one of the famous technique to estimate V_{TH}. It entails calculation of V_g intercept (i.e., $I_D = 0$) of the extrapolation of I_D–V_g curve at its highest first derivative (slope) point (i.e. the point of maximum transconductance, g_m) [15]. The effect of nanowire widths (W_{Si}) and channel length (L_C) on V_{TH} of the devices is shown in Fig. 4-8. The devices have L_{ANT} = 240 nm, are operated in linear region with drain voltage, V_D= 50 mV. V_{SUB}= 10 V, source is ground and V_G is swept from 0 to -3 V. It can be observed that as

the W_{Si} is reduced the gate voltage required to invert the SOI channel is increased. This is due to the quantum confinement effect. The potential well created due to reduced W_{Si} and electrical bias can cause sub-band splitting (between 2- fold and 4-fold valleys of the conduction band, light and heavy hole bands of the valence band) when the quantum confinement happens [24, 25]. The sub-band splitting results in a smaller density of states so that more energy-band bending is required to attain a desired inversion-charge density as compared to a thicker body device. The increase in threshold voltage has been observed in thin-body structure device [26].

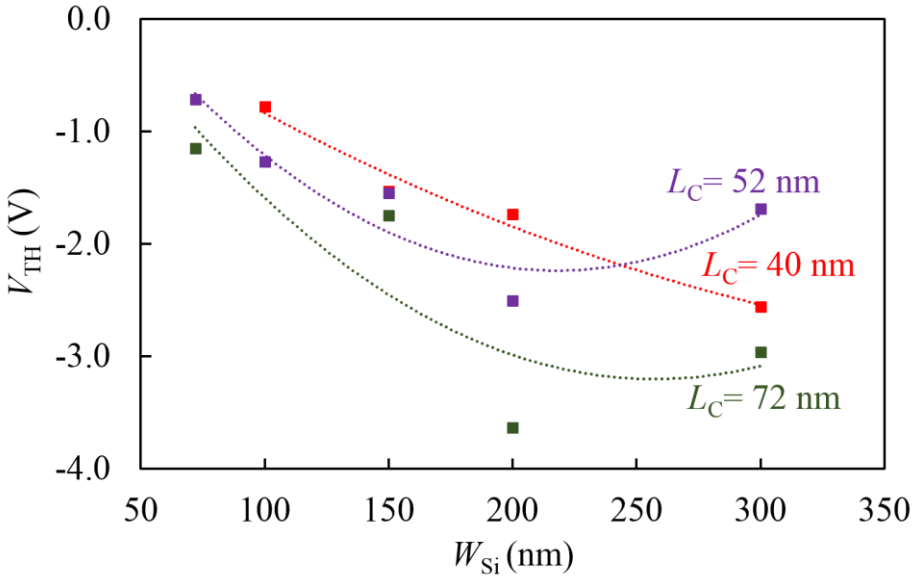

Fig. 4-8 SOI MOSFET threshold voltage vs nanowire width characteristics. L_{ANT}= 240 nm, V_{SUB}= 10 V and V_D= 50 mV, T= 300 K.

4.5.2 Optical measurements at T = 300 K

The drain current waveforms is shown in Fig. 4-9 for several values of light strengths at incident wavelength of 535 nm. Standard I_D is regulated to be around 1 nA by V_G. Every resulting waveform has been moved for easy understanding.

The device dimensions are W_{Si}, L_{ANT} and L_C of 150, 240 and 40 nm, respectively. The various bias, such as V_G, V_{SUB}, and V_D are 0.9, 20, and 0.05 V respectively. We can observe that no discrete levels which correspond to the photo-generated holes stored under the bow-tie antenna are present. This shows that the typical single photon detector characteristics are not observed from the drain current waveforms.

Fig. 4-10 displays the histograms of drain current for various light intensities (a) Dark, (b) 32 μW/cm^2, (c) 265 μW/cm^2 and (d) 2540 μW/cm^2. The closed dots are acquired data and solid lines are suitable curves fitted with Gaussian distribution. The histograms show only one peak unlike the typical single photon detector characteristics. In the fabricated devices we do not observe single photon sensitivity. The change of average source current at different light intensities is shown in Fig. 4-11. As light intensity is increased the average source current is also increased contrary to the photon detector behavior.

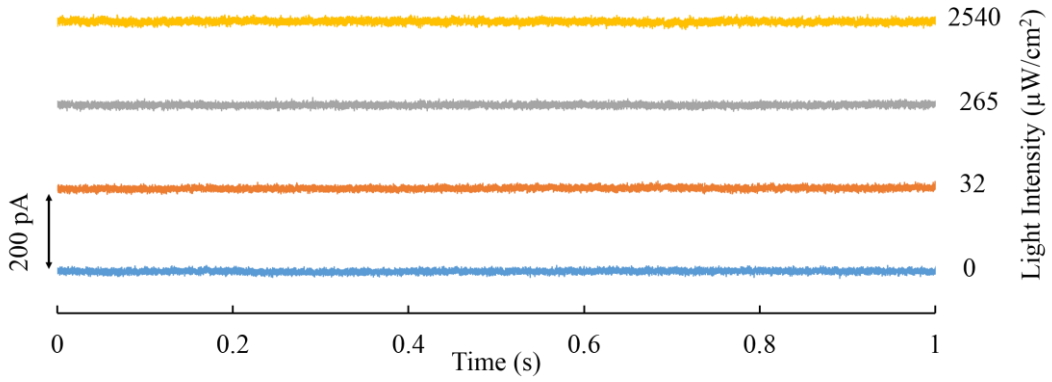

Fig. 4-9 Representative I_D waveforms at 300 K for several values of light intensity at wavelength = 535 nm. Standard I_D is regulated to 1 nA by V_G and every waveform is moved for visual clearness. V_G, V_{SUB}, and V_D are 0.9, 20, and 0.05 V, respectively.

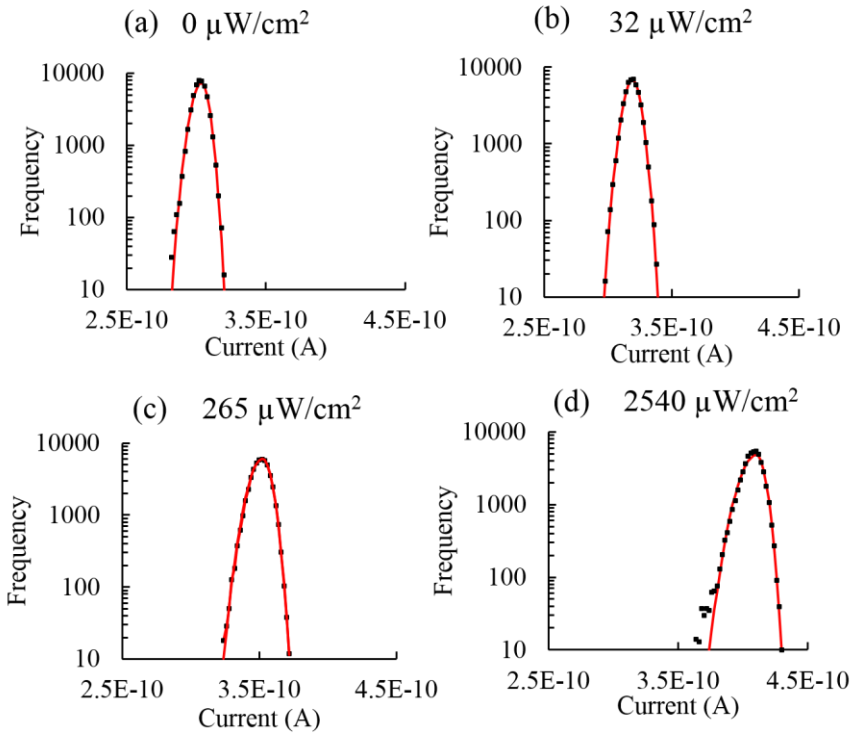

Fig. 4-10 Histograms of digitized drain currents corresponding to Fig. 4-8. Data acquisition time period and time step are 2.45 s and 49 μs, respectively, and 50000 (2.45 s/49 μs) data points (current values) are classified into bins with a width of 2 pA.

The increase of source current with light intensity suggests that the device is behaving as a photoconductor. The relative widths of the histograms shown in Fig. 4-10 was calculated and plotted at different light intensities as shown in Fig. 4-12. There is slight change in relative widths at different light intensities which can be presumed as not typical behavior of a photon detector.

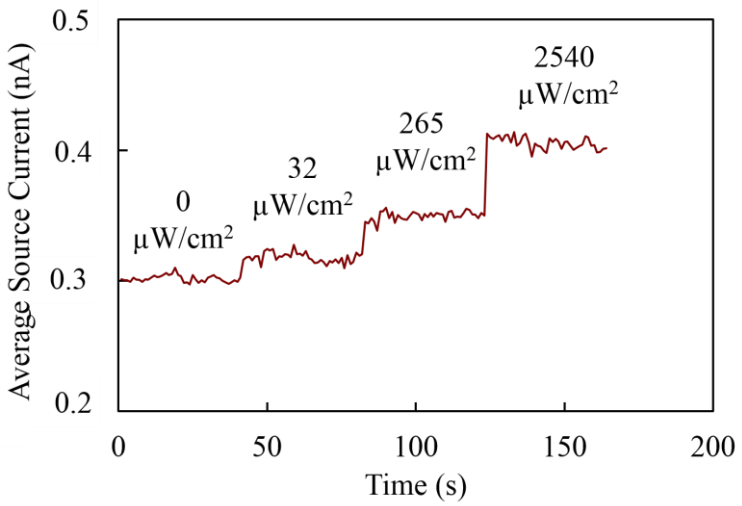

Fig. 4-11 Average source current at different light intensities. Incident wavelength is 535 nm.

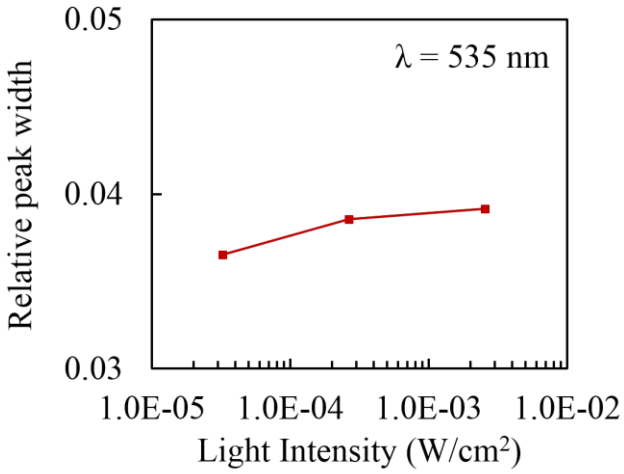

Fig. 4-12 Average source current at different light intensities.

4.5.3 Optical measurements at T = 100 K

By reducing the temperature to 100 K, it is expected that the hole lifetime can be increased. The I_D waveforms is displayed in Fig. 4-13 for several levels of light intensities at incident wavelength of 535 nm. Baseline current is attuned to 1 nA by V_G, and every waveform is shifted for clarity. The device dimensions are W_{Si}, L_{ANT} and L_C of 150, 240 and 40 nm, respectively. The various bias, such as V_G, V_{SUB}, and V_D are 0.8, 40, and 0.05 V respectively. We can observe that no discrete levels which correspond to the photo-generated holes stored under the bow-tie antenna are present. This shows that the typical single photon detector characteristics are not observed from the drain current waveforms.

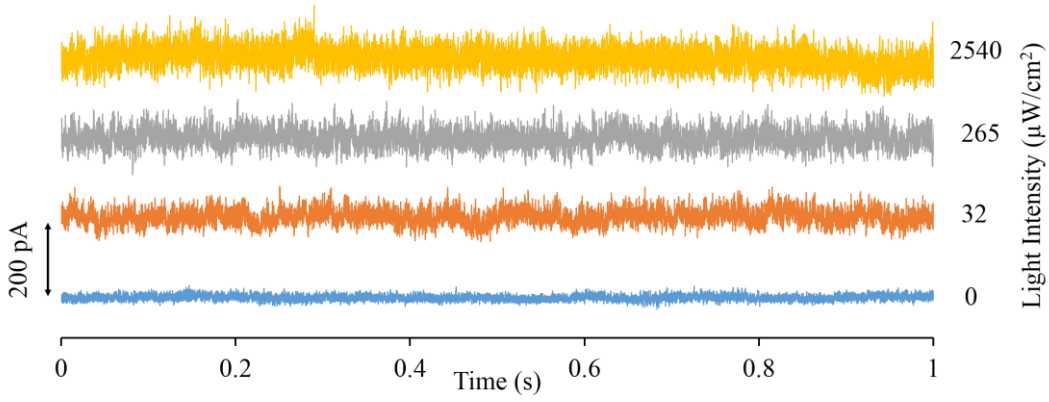

Fig. 4-13 Typical drain current waveforms at 100 K for different levels of light intensity at wavelength = 535 nm. Baseline current is adjusted to 1 nA by V_G and each waveform is shifted for visual clarity. V_G, V_{SUB}, and V_D are 0.8, 40, and 0.05 V, respectively.

Fig. 4-14 displays the histograms of drain current for various light intensities (a) Dark, (b) 32 μW/cm^2, (c) 265 μW/cm^2 and (d) 2540 μW/cm^2. The dotted symbols are obtained data and solid lines are fitting curves with Gaussian distribution. The histograms show only one peak unlike the typical single photon detector characteristics. In the fabricated devices we do not observe single photon sensitivity. The change of average source current at different light intensities is shown in Fig. 4-15. As light intensity is increased the average source current is also increased contrary to the photon detector behavior.

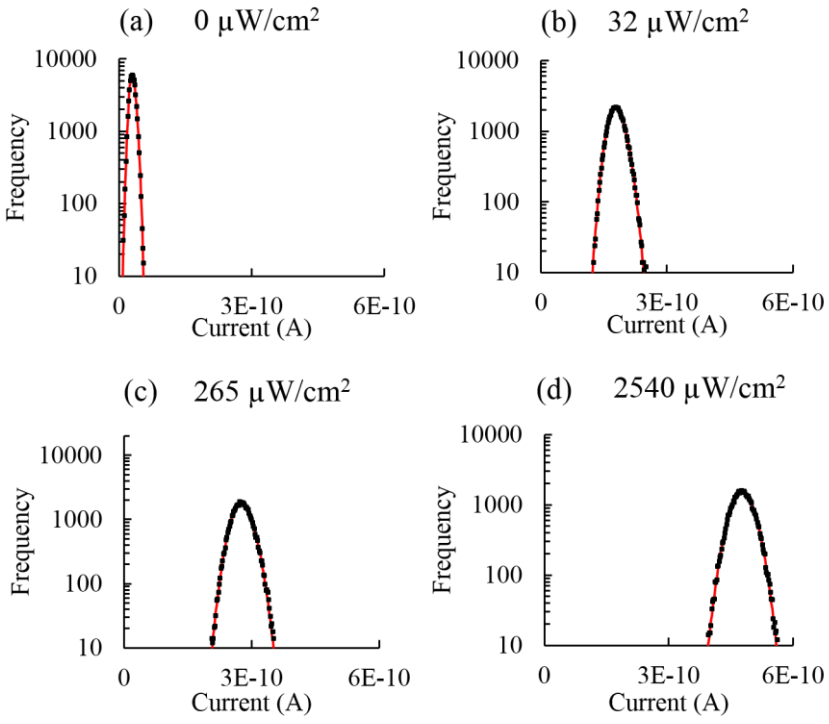

Fig. 4-14 Histograms of digitized drain currents corresponding to Fig. 4-12. Data acquisition time period and time step are 2.45 s and 49 μs, respectively, and 50000 (2.45 s/49 μs) data points (current values) are classified into bins with a width of 2 pA.

The increase of source current with light intensity suggests that the device is behaving as a photoconductor. The relative widths of the histograms shown in Fig. 4-14 was calculated and plotted at different light intensities as shown in Fig. 4-16. There is slight change in relative widths at different light intensities which can be presumed as not typical behavior of a photon detector.

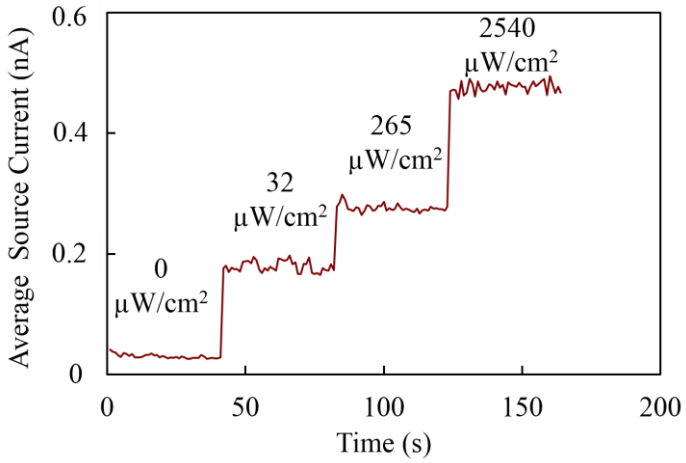

Fig. 4-15 Average source current at different light intensities.

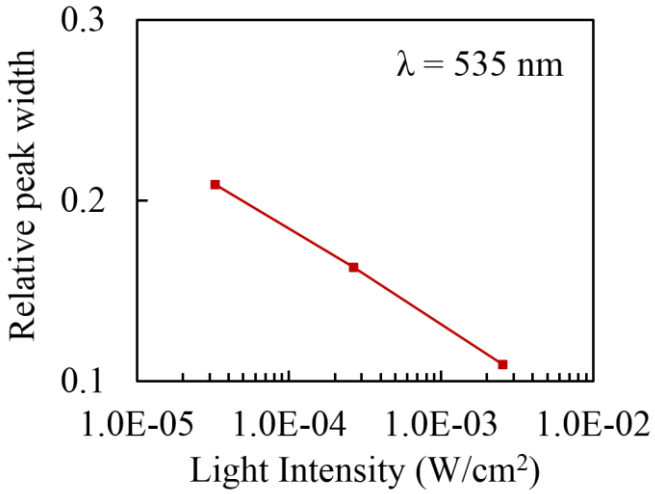

Fig. 4-16 Average source current at different light intensities.

4.6 Conclusion

Characterization of SOI MOSFET with single photon sensitivity has been shown. In the SOI nanowire MOSFET with upper and lower gates, holes are successfully stored under the negatively biased lower gate. Drain current waveforms show the creation and recombination of each holes and the peaks of histograms correspond to each hole stored under various light intensities. The single hole counting operation of SOI nanowire MOSFET was successfully demonstrated. Electrical and optical characterization of fabricated SOI nanowire MOSFET with bow-tie antenna was performed. It is observed that as the nanowire width of the MOSFET is reduced the absolute threshold voltage required to just invert the MOSFET channel also reduces. Since, less silicon channel area has to be inverted due to reduced wire width. However, in the optical measurements the fabricated device was not showing typical photon detector characteristics rather the device is behaving as a photoconductor.

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Chapter 5

SUMMARY AND FINAL CONCLUSION

5.1 Summary

The main objective of this work is to put forward a novel idea of incorporating an optical nanoantenna in shape of a bow-tie to photodetectors viz. SOI nanowire pn photodiode and SOI nanowire n-type MOSFET. It is expected that when the light enters the nanoantenna, it resonantly excites the surface plasmons on the surface of gold bow-tie structure. Initially, the bow tie is closed, but a nanogap can be created at the junction. The excited surface plasmons can lead to the improvement of the electric field near the nanogap. As a result, the optical near field will generate extra carriers within the depleted Si nanowire.

SOI MOSFET has been recently characterized to be used as a single photon detector based on single-hole counting, it has various advantages and can outperform the conventional single-photon detectors. However, it suffers from low quantum efficiency. A bow-tie nanoantenna can be used as a gate electrode of the SOI MOSFET and can possibly enhance the electric field near the nanogap generating extra carriers in the SOI.

Eventually, increasing the quantum efficiency of the SOI MOSFET. Similarly bow-tie antenna can increase the cathode current in SOI pn photodiode.

In this thesis at first, we fabricate the SOI nanowire MOSFET and SOI nanowire pn photodiode with bow-tie nanoantenna. Then we do the electrical and optical characterization on the devices in the visible incident light. FDTD simulations were also done to observe the electric field generated in the bow-tie structure. The scope of each chapter covering detailed information is summarized in following paragraphs.

Chapter 1, presented the research background related to various photon counting technologies, covering the conventional and state of the art photodetectors based on, photon detection by carrier multiplication or by detecting single carriers. Important advances that set the grounds for photon detection by SOI MOSFET and reports on conventional single-photon detectors including ones based on single-charge counting are summarized. The motivation behind current research is explained and synopsis of each chapter is provided.

In **Chapter 2**, the fabrication process of SOI nanowire devices with gold bow-tie surface plasmon antenna is described in detail. The devices are fabricated in a top-down approach on a commercially available SOI wafer from Soitec™ in a clean room facility with state of the art equipment.

The fabrication process is compatible with CMOS fabrication done in semiconductor industry.

Chapter 3, provides detailed methodology of characterization of SOI nanowire pn photodiode with gold bow-tie surface plasmon antenna. The measurement setup to measure the spectroscopic response of the device is explained. Creation of nanogap in the junction of bow-tie by process of electromigration is explained and the size of nanogap is calculated. In ideal case the creation of nanogap in the bow-tie structure was expected to be just on top of the silicon nanowire, however in reality it is far from the nanowire. The position of nanogap is difficult to be controlled. 3D finite difference time domain method was used to simulate the near-file profile in the bow-tie antenna without and with nanogap (size = 10 nm) at an incident wavelength of 720 nm. As our expectations by creating a nanogap the concentration of electric field is increased, and the electric field with higher intensity is distributed inside the nanoantenna. The presence of nanogap of 10 nm in the neck of bow-tie nanoantenna increases the quantum efficiency in the specified region with 200 x 150 x 60 nm^3 (length x width x depth) in SOI nanowire by 50%.

In **Chapter 4**, we successfully confirmed the single photon detection by SOI MOSFET with upper and lower gates. The incident light photons generate holes and electrons in the top silicon and the holes are stored under the negatively biased gate of SOI MOSFET. The generated electrons drift

to the bottom electron channel creating a spike in the drain current waveform. Each rising pulse in the drain current waveform is a hole stored under the gate. It was observed that the hole generation rate is directly proportional to the incident light intensity. However, the quantum efficiency is low. To address this issue SOI nanowire MOSFET with bow-tie antenna was characterized. As per our expectations the absolute value of threshold voltage of the SOI MOSFETs was reduced with the reduction in nanowire width because the silicon channel required to invert was also reduced. The optical measurements were performed at T = 300 and 100 K. In both the measurements the device is not showing the typical single photon detector characteristics.

5.2 Unresolved Issues

We have successfully demonstrated the fabrication of the nanowire photodetectors with gold bow-tie nanoantenna. Optical and electrical characterization was also successfully done. However, number of issues, remain unresolved. Various issues that require further investigation are listed as below.

1. *Localization of photosensitive region*: The nanoantenna effect is usually localized, however the effective detector area of the SOI nanowire PD includes the contribution of the depleted area. Since

in the device the depleted area extends all over the device, the localized antenna effect can be further studied. Electrical biasing conditions for localization of photosensitive (depletion) region near nanogap needs to be further studied. Secondly, new device can be fabricated with reduction of insulator thickness between bow-tie antenna and SOI nanowire.

2. *Optical response of SOI nanowire MOSFET with bow-tie antenna:* The device can be measured at other low temperatures below besides 100 K to observe asymmetry in the drain current histogram. The asymmetry is a sign of photosensitivity of the SOI MOSFET, greater it is higher is the photosensitivity.

5.3 Recommendation for Future Work

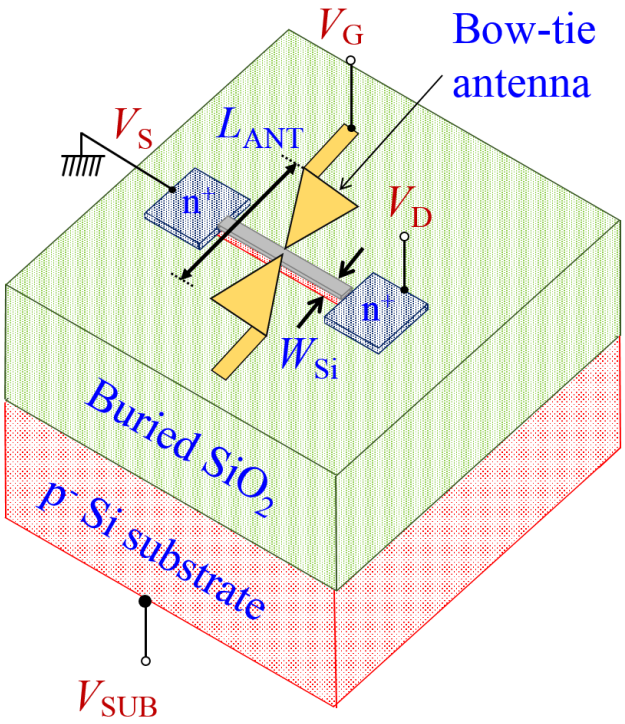
The research objective presented in this thesis was fabrication and characterization of novel photodetectors, viz. SOI nanowire pn photodiode and SOI MOSFET with bow-tie nanoantenna. The objective was successfully achieved. The effect of nanogap formation in bow-tie structure was evaluated by experiments and by simulations. This thesis is an attempt at proposing a novel structure for SOI MOSFET photodetectors

and SOI pn photodiode. As the results suggest, there are still some improvements that need to be done in the present structure.

The next goal will be to fabricate new devices with the proposed structural modifications to realize a more efficient SOI MOSFET photodetector.

Appendix A: Fabrication process of SOI Nanowire MOSFET

Device Structure:



Nanowire Dimensions:

Length = 1400 nm,

Width = 52 to 300 nm

Thickness = 60 nm

Bow-tie Antenna Dimensions:

Length = 240 to 400 nm

Channel length:

40, 52, 72 nm

Process Information (Etch Rates)

BHF63U SiO_2- 84.73 nm/min

Diluted HF 2.5% (HF (50%):H_2O = 1:20) SiO_2- 20 nm/min

Diluted HF 10% (HF (50%):H_2O = 1:4) SiO_2- 67.01 nm/min

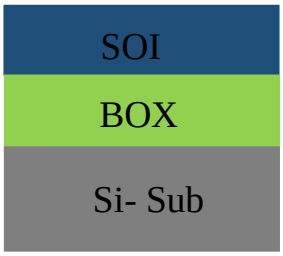
Reactive Ion Etch (#1: CHF3 20 sccm, RF Power 250W, Pressure 2 Pa)

Si (100)- 4.85 nm/min, SiO_2- 54.78 nm/min

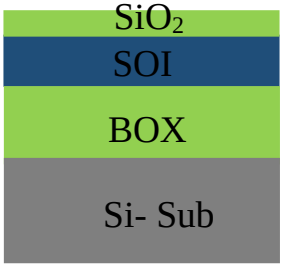
Reactive Ion Etch (#2: SF6 24 sccm, O2 6 sccm, RF Power 30W, Pressure 5 Pa)

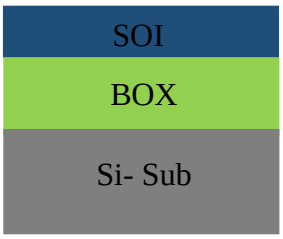
Si (100)- 3.06 nm/min, SiO_2- 0.10 nm/min

1. Wafer cut

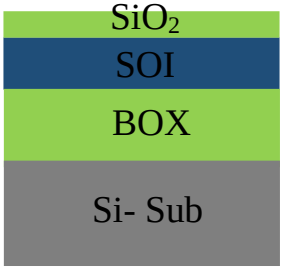
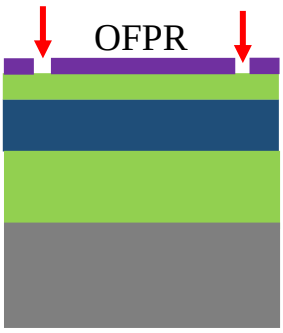
Process	Recipe	Cross section
Wafer Cut First Cleaning	SOI Wafer Cut: 2 x 2 cm Piranha (H_2O_2 20cc +H_2SO_4 60cc) 2 mins. Pure Water Rinse 5 mins. } x 2 2.5% Diluted HF 10 sec. (Check for hydrophobicity at the front surface) Pure Water Rinse 5 mins.	

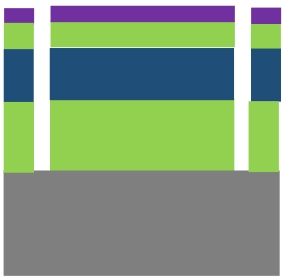
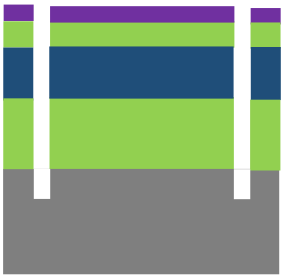
2. SOI thinning

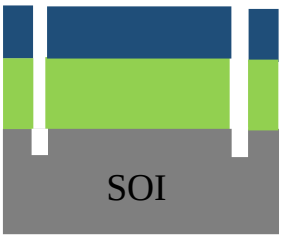
Process	Recipe	Cross section
Thermal Oxidation	<u>Wet Oxidation</u> 1000 degC 129 min. 20 sec. SiO_2 = 523 nm SOI Target (nm) = 110 nm <u>Dry Oxidation</u> 1000 degC 67 min. 36 sec. SiO_2 = 57 nm SOI Target (nm) = 85 nm <u>Dry Oxidation</u> 1000 degC 67 min. 36 sec. SiO_2 = 57 nm SOI Target (nm) = 60 nm	

Oxide Removal	10 % Diluted HF 57 sec + 10 sec. (over-etch) (Check for hydrophobicity at the front surface) Pure Water Rinse 5 mins	

3. Alignment Mark

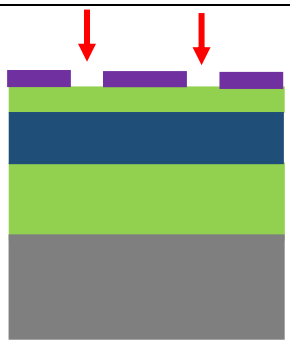
Process	Recipe	Cross section
Thermal Oxidation	<u>Dry Oxidation</u> 900 degC 68 min. 30 sec. Target SiO_2 = 20 nm Top Si consumed = ~9 nm	
Resist Coating	OFPR CP-34 (positive-tone) <u>Recipe:</u> ofprenew.rcp HMDS: 3000 rpm 60 sec. OFPR: 2600 rpm 16 sec. Pre Bake: 110º C, 90 sec.	
Patterning	UV Lithography <u>Mask:</u> HF1-MRK Hard Contact, Exposure Time: 4.5 sec. NMD-3 23º C 40 sec., (Water 30 sec. x 2) Post Bake: 135º C, 300 sec.	

Oxide Etching	Buffered Hydrofluoric Acid BHF63U (150%), 20 sec. Pure Water Rinse 5 mins (Check for hydrophobicity at the back surface)	OFPR 
SOI Etching	Reactive Ion Etching <u>Recipe:</u> #2 SF6 24 sccm + O2 6 sccm, 30W, 5Pa, 25 sec. (50% over-etch) Target Si etch: 60 nm	OFPR 
BOX Etching	Buffered Hydrofluoric Acid BHF63U (150%), 8 min. (20 % over-etch). Pure Water Rinse 5 mins	OFPR 
Si Etching	Reactive Ion Etching <u>Recipe:</u> #2 SF6 24 sccm + O2 6 sccm, 30W, 5Pa, 11 min. Target Si etch: 2020 nm	OFPR 

Resist (OFPR) Removal	Reactive Ion Etching Before OFPR removal, clean chamber of RIE by <u>Recipe #10</u> Then , <u>Recipe:</u> #4 O2 20 sccm, 100W, 50Pa, 10 min.	SiO_2 
Oxide Removal	Piranha (H_2O_2 20cc +H_2SO_4 60cc) 2 mins. Pure Water Rinse 5 mins. } x 2 2.5% Diluted HF 10 sec. (Check for hydrophobicity at the front surface) Pure Water Rinse 5 mins.	 SOI

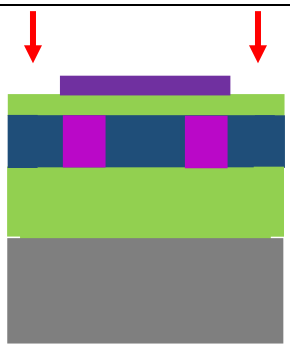
4. Phosphorus Doping

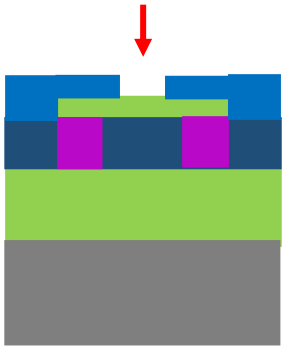
Process	Recipe	Cross section
Thermal Oxidation	<u>Dry Oxidation</u> 900 degC 68 min. 30 sec. Target SiO_2 = 20 nm Top Si consumed = ~9 nm	SiO_2 

Resist Coating	OFPR CP-34 (positive-tone) <u>Recipe:</u> ofprenew.rcp HMDS: 3000 rpm 60 sec. OFPR: 2600 rpm 16 sec. Pre Bake: 110º C, 90 sec.	OFPR 
Patterning	UV Lithography <u>Mask:</u> HF1-N Hard Contact, Exposure Time: 4.5 sec. NMD-3 23º C 40 sec., Water 30 sec. x 2 Post Bake: 135º C, 300 sec.	
Oxide Etching	Buffered Hydrofluoric Acid BHF63U (150%), 29 sec. Pure Water Rinse 5 mins (Check for hydrophobicity at the back surface)	
Resist Removal Natural SiO_2 removal	Piranha (H_2O_2 20cc +H_2SO_4 60cc) 2 mins. Pure Water Rinse 5 mins. } x 2 2.5% Diluted HF 10 sec. (Check for hydrophobicity at the front surface) Pure Water Rinse 5 mins.	

Protection Oxide	<u>Dry Oxidation</u> (Furnace B) 650 degC 10 min. Target SiO_2 = 1 nm Don't dip in H_2O after oxidation	
OCD Coating Pre-deposition Drive-In	Spin Coater <u>Recipe:</u> OCD59230 OCD P-59230 3000 rpm 15 sec. <u>Furnace D</u> N_2 (1.5L/min.) 600º C, 30 min. N_2 (1.5L/min.) 880º C, 20 min.	
OCD and SiO_2 Removal	2.5% Diluted HF 2 min. (Check for hydrophobicity at the front surface) Pure Water Rinse 5 mins Piranha (H_2O_2 20cc +H_2SO_4 60cc) 2 mins. Pure Water Rinse 5 mins. } x 5 SOI thickness measured at doped region:	

5. Silicon-on-insulator (SOI) Patterning

Process	Recipe	Cross section
Thermal Oxidation Thermal Annealing	<u>Dry Oxidation</u> (Furnace B) 900 degC 68 min. 30 sec. Target SiO_2 = 20 nm Top Si consumed = ~9 nm (Furnace B) 1000 degC 60 min. (N_2: 1.5L/min.) Keep samples at the furnace entrance when temperature is increasing from 900 to 1000 degC.	SiO_2 
Resist Coating	OFPR CP-34 (positive-tone) <u>Recipe:</u> ofprenew.rcp HMDS: 3000 rpm 60 sec. OFPR: 2600 rpm 16 sec. Pre Bake: 110º C, 90 sec.	
Patterning Resist Dvmnt.	UV Lithography <u>Mask:</u> HF1-AC Hard Contact, Exposure Time: 4.5 sec. NMD-3 23º C 40 sec., Water 30 sec. x 2 Post Bake: 135º C, 300 sec.	

Oxide Etching Resist Removal	Buffered Hydrofluoric Acid BHF63U (150%), 29 sec. Pure Water Rinse 5 mins Piranha (H_2O_2 20cc +H_2SO_4 60cc) 2 mins. Pure Water Rinse 5 mins. } x 2	 
Nanowire Fabrication Resist Coating	ZEP-520A=1:1 (positive-tone) Recipe: satoh-ZEP520A40_3000.rec HMDS: 3000 rpm 60 sec. ZEP-A=1:1 3000 rpm 70 sec. Pre Bake: 180º C, 120 sec.	
Electron Beam Exposure Resist Dvmnt.	Electron Beam Lithography JBX-6300SP Mask: HF1-AC Hard Contact, Exposure Time: 4.5 sec. o-xylene 23º C 2 mins., Iso-propyl alcohol 40 sec. Post Bake: 120º C, 300 sec.	

SiO_2 Etching	Reactive Ion Etching <u>Recipe:</u> #1 CHF3 20 sccm, 250W, 2Pa, 25 sec. (50% over-etch) Target Si etch: nm	
Resist (ZEP) Removal Cleaning and Natural Oxide Removal	Reactive Ion Etching Before ZEP removal, clean chamber of RIE by <u>Recipe #10</u> Then , <u>Recipe:</u> #4 O2 20 sccm, 100W, 50Pa, 10 min. Piranha (H_2O_2 20cc +H_2SO_4 60cc) 2 mins. Pure Water Rinse 5 mins. } x 2 2.5% Diluted HF 10 sec. (Check for hydrophobicity at the front surface) Pure Water Rinse 5 mins.	
Si Etching	Reactive Ion Etching <u>Recipe:</u> #2 SF6 24 sccm + O2 6 sccm, 30W, 5Pa, 31 sec. Target Si etch: 96 nm (20% over-etch)	

Resist Removal Natural SiO_2 removal	Piranha (H_2O_2 20cc +H_2SO_4 60cc) 2 mins. Pure Water Rinse 5 mins. x 2 2.5% Diluted HF 10 sec. (Check for hydrophobicity at the front surface) Pure Water Rinse 5 mins.	
Gate Dielectric Fabrication Thermal Oxidation SiNx Deposition	Dry Oxidation (Furnace B) 900 degC 68 min. 30 sec. Target SiO_2 = 20 nm Top Si consumed = ~9 nm (insert in O_2) Electron Cyclotron Sputtering Target thickness: 6.7 nm	

6. Antenna Fabrication

Process	Recipe	Cross section
Cleaning	Piranha (H_2O_2 20cc +H_2SO_4 60cc) 2 mins. Pure Water Rinse 5 mins. x 2	

Resist Coating	ZEP-520A=1:1 (positive-tone) Recipe: satoh-ZEP520A40_3000.rec HMDS: 3000 rpm 60 sec. ZEP-A=1:1 3000 rpm 70 sec. Pre Bake: 180º C, 120 sec.	
Electron Beam Exposure Resist Dvmnt.	Electron Beam Lithography JBX-6300SP ANT(L29), 5th lens mode, BC: 100 pA, 50 µm field, 2 nm shot step, AP: 25 µm (#3), Dose: 160 µC/cm^2 o-xylene 23º C 2 mins., Iso-propyl alcohol 40 sec. Post Bake: 120º C, 300 sec.	
Titanium/ Gold Deposition Resist Lift-off	Electron Beam Evaporation Titanium thickness: 5 nm, Gold thickness: 50 nm Organic Remover 1165 half day, Ultrasonic agitation 1-2 mins. CHECK the condition of metal film removal, Prepare new REM1165 in the other beaker. Introduce the samples in new REM1165. Ultrasonic agitation 40min	

Cleaning	Hand Agitation Ethanol: 1 min. Ethanol spraying } x 2 Pure Water Rinse 5 mins.	

7. Backside Etching

Process	Recipe	Cross section
Cleaning	Acetone 3 min. x 3 times Ethanol 3 min. x 1 time Pure Water Rinse 5 mins.	
Resist Coating	OFPR CP- 34 (positive-tone) <u>Recipe:</u> ofprnew.rcp HMDS: 3000 rpm 60 sec. OFPR CP-34: 2600 rpm 70 sec. Pre Bake: 135° C, 300 sec.	
Backside SiO_2 Etching	Buffered Hydrofluoric Acid BHF63U (150%), 55 sec. Pure Water Rinse 5 mins (Check for hydrophobicity at the back surface)	

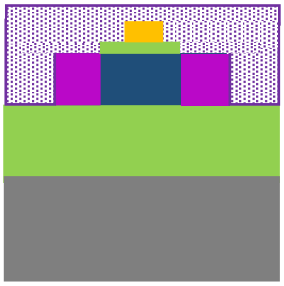
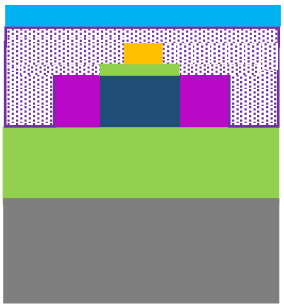
Resist Removal	Acetone 3 min. x 3 times Ethanol 3 min. x 1 time Pure Water Rinse 5 mins.	

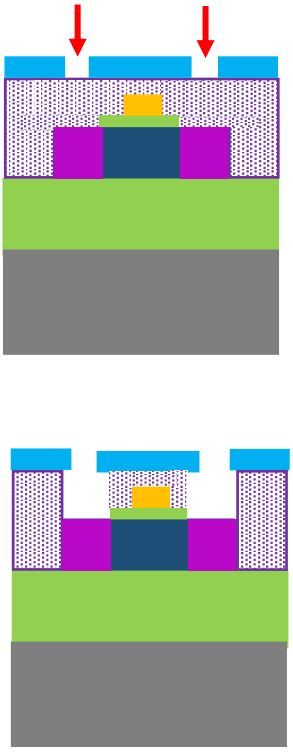
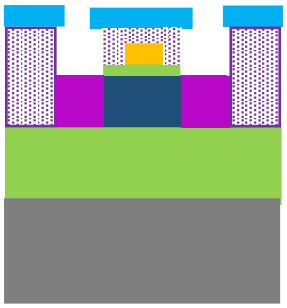
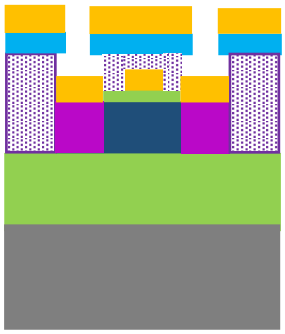
8. Contact Hole Fabrication

Process	Recipe	Cross section
Resist Coating	OFPR CP- 34 (positive-tone) <u>Recipe:</u> ofprnew.rcp HMDS: 3000 rpm 60 sec. OFPR CP-34: 2600 rpm 16 sec. Pre Bake: 110º C, 90 sec.	
Patterning Resist Dvmnt.	UV Lithography <u>Mask:</u> HF1-CON Hard Contact, Exposure Time: 4.5 sec. NMD-3 23º C 40 sec., (Water 30 sec. x 2) Post Bake: 135º C, 300 sec.	

SiO_2 and SiNx Etching	Buffered Hydrofluoric Acid BHF63U (150%), 4 min. 10 sec. Pure Water Rinse 5 mins	
Resist Removal	Acetone 3 min. x 3 times Ethanol 3 min. x 1 time Pure Water Rinse 5 mins.	

9. Contact Pads Fabrication

Process	Recipe	Cross section
Resist Coating (lower resist)	PMGI SF8S (positive-tone) Recipe: satoh__PMGI 4500.rec PMGI SF8S: 4500 rpm 60 sec. Pre Bake: 190º C, 120 sec.	
Resist Coating (upper resist)	ZEP520A/ZEP-A= 1:1 (positive-tone) Recipe: satoh__ZEP520A_PMGI_ 3000.rec 3000 rpm 70 sec. Pre Bake: 180º C, 120 sec.	

Electron Beam Exposure Resist Dvmnt. (upper resist) Resist Dvmnt. (lower resist)	Electron Beam Lithography JBX-6300SP M1(L13), 4th lens mode, BC: 100 pA, 400 µm field, 10 nm shot step, AP: 60 µm (#5), Dose: 160 µC/cm^2 o-xylene 23º C 2 mins., Iso-propyl alcohol 40 sec. Post Bake: 120º C, 300 sec. NMD-3 23º C 55 sec., (Water 30 sec. x 2) Post Bake: 120º C, 300 sec.	
Contact holes clean before final metal deposition	Buffered Hydrofluoric Acid NH4F 200cc + 50% wt. dil. HF 6cc (100:3) 10 sec. Pure Water Rinse 5 mins	
Titanium/ Gold Deposition	Electron Beam Evaporation Titanium thickness: 20 nm, Gold thickness: 300 nm Organic Remover 1165 half day, Ultrasonic agitation 1-2 mins. CHECK the condition of metal film removal, Prepare	

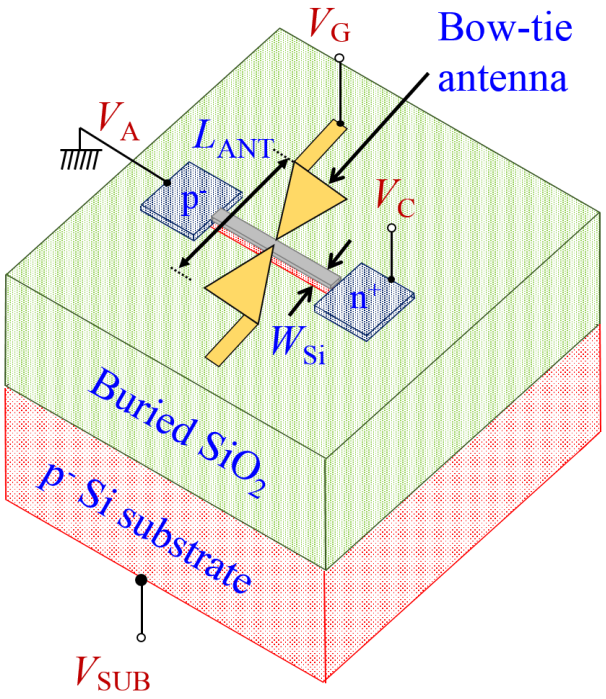
	new REM1165 in the other beaker. REM1165. Ultrasonic agitation 40min	
Cleaning	Hand Agitation Ethanol: 1 min. Ethanol spraying } x 2 Pure Water Rinse 5 mins.	

Fabrication process of SOI Nanowire PN Photodiode

The SOI Nanowire PN Photodiode is fabricated on the same chip along with SOI Nanowire MOSFET.

The fabrication steps of SOI thinning, alignment mark fabrication, etc. are same as displayed above however, during phosphorus doping instead of fabricating two n+ region in MOSFET, there is only one region for n+ doping to form cathode in photodiode.

Device Structure:



Nanowire Dimensions:

Length = 1400 nm,

Width = 52 to 300 nm

Thickness = 60 nm

Bow-tie Antenna Dimensions:

Length = 240 to 400 nm

Channel length:

40, 52, 72 nm

1. Phosphorus Doping

Process	Recipe	Cross section
Thermal Oxidation	<u>Dry Oxidation</u> 900 degC 68 min. 30 sec. Target SiO_2 = 20 nm Top Si consumed = ~9 nm	SiO_2 
Resist Coating	OFPR CP-34 (positive-tone) <u>Recipe:</u> ofprenew.rcp HMDS: 3000 rpm 60 sec. OFPR: 2600 rpm 16 sec. Pre Bake: 110º C, 90 sec.	OFPR 
Patterning	UV Lithography <u>Mask:</u> HF1-N Hard Contact, Exposure Time: 4.5 sec. NMD-3 23º C 40 sec., Water 30 sec. x 2 Post Bake: 135º C, 300 sec.	
Oxide Etching	Buffered Hydrofluoric Acid BHF63U (150%), 29 sec. Pure Water Rinse 5 mins (Check for hydrophobicity at the back surface)	

Resist Removal Natural SiO_2 removal	Piranha (H_2O_2 20cc +H_2SO_4 60cc) 2 mins. Pure Water Rinse 5 mins. } x 2 2.5% Diluted HF 10 sec. (Check for hydrophobicity at the front surface) Pure Water Rinse 5 mins.	
Protection Oxide	<u>Dry Oxidation</u> (Furnace B) 650 degC 10 min. Target SiO_2 = 1 nm Don't dip in H_2O after oxidation	
OCD Coating Pre-deposition Drive-In	Spin Coater <u>Recipe:</u> OCD59230 OCD P-59230 3000 rpm 15 sec. <u>Furnace D</u> N_2 (1.5L/min.) 600º C, 30 min. N_2 (1.5L/min.) 880º C, 20 min.	

OCD and SiO_2 Removal	2.5% Diluted HF 2 min. (Check for hydrophobicity at the front surface) Pure Water Rinse 5 mins Piranha (H_2O_2 20cc +H_2SO_4 60cc) 2 mins. Pure Water Rinse 5 mins. x 5 SOI thickness measured at doped region:	

List of Publications

Journal Papers

1. Yash Sharma, Hiroaki Satoh, Hiroshi Inokawa, "Application of Bow-Tie Surface Plasmon Antenna to Silicon on Insulator Nanowire Photodiode for Enhanced Light Absorption," IEICE Electronics Express, Volume 15 (2018) Issue 11 pp. 20180328.
2. Amit Banerjee, Hiroaki Satoh, Yash Sharma, Norihisa Hiromoto, Hiroshi Inokawa, "Characterization of Platinum and Titanium Thermistors for Terahertz Antenna-Coupled Bolometer Applications", Sensors & Actuators: A Physical, Vol. 273, pp. 49-57, 2018.
3. Amit Banerjee, Hiroaki Satoh, Durgadevi Elamaran, Yash Sharma, Norihisa Hiromoto, Hiroshi Inokawa, "Optimization of narrow width effect on titatnium thermistor in uncooled antenna-coupled terahertz microbolometer", Jpn. J. Appl. Phys., Vol. 57, No. 4S, pp. 04FC09_1-7, 2018.

Conference Papers

1. Amit Banerjee, Hiroaki Satoh, Yash Sharma, Norihisa Hiromoto and Hiroshi Inokawa, "Fabrication of Room-Temperature Terahertz Microbolometer Arrays for Biomedical Imaging Applications," 70th Annual Session of Chemical Engineering Congress (CHEMCON-2017) (Haldia, India, Dec. 27-30, 2017).
2. Yash Sharma, Hiroaki Satoh, Amit Banerjee and Hiroshi Inokawa, "Fabrication Features of Novel Nanophotonic Devices for Imaging Applications: Single-Photon Detector and Thermal Detector," 19th Takayanagi Kenjiro Memorial Symposium, pp. 214-217 (Hamamatsu, Japan, Nov. 21-22, 2017).
3. Amit Banerjee, Hiroaki Satoh, Yash Sharma, Norihisa Hiromoto, and Hiroshi Inokawa, "Room-Temperature Terahertz Microbolometer Arrays for Biomedical Imaging Applications," Proc. 15th World Medical Nanotechnology Congress, p. 15 (Osaka, Japan, 2017.10. 18-19.
4. Yash Sharma, Hiroaki Satoh, Hiroshi Inokawa, “Silicon on Insulator Nanowire Photodiode with Nanoscale Bow-Tie Surface Plasmon Antenna for Light Detection Applications”, 2017 Int. Conf. Solid State Devices and Materials (SSDM) H-7-04, pp. 419-420 (Sendai, Japan, Sep. 19-22, 2017).

5. Amit Banerjee, Hiroaki Satoh, Yash Sharma, Norihisa Hiromoto, Hiroshi Inokawa, “Optimization of Platinum and Titanium Thermistor in Uncooled Antenna-Coupled Terahertz Microbolometer”, 2017 Int. Conf. Solid State Devices and Materials (SSDM) PS-2-02, pp. 729-730 (Sendai, Japan, Sep. 19-22, 2017).
6. Yash Sharma, Hiroaki Satoh, Hiroshi Inokawa, “Silicon on insulator nanowire photodiode with surface plasmon antenna”, 2017 International Symposium toward the Future of Advanced Researches in Shizuoka University, p. 96, (Hamamatsu, Japan, Mar. 8, 2017).
7. Yash Sharma, Hiroaki Satoh, Hiroshi Inokawa, “Fabrication of SOI MOSFET based Photon Detector with Surface Plasmon Antenna”, 6th Shizuoka University International Symposium 2016, p. 90, (Hamamatsu, Japan, Dec. 8-9, 2016).
8. Yash Sharma, Hiroaki Satoh, Hiroshi Inokawa, “SOI MOSFET Photon Detector with Surface Plasmon Antenna”, 18th Takayanagi Kenjiro Memorial Symposium, pp. 89-91 (Hamamatsu, Japan, Nov. 15-16, 2016).