An Optimum Design of Thermal Energy Transducers and Power Converters for Small Form-Factor Thermoelectric Energy Harvester

Kazuma Koketsu and Toru Tanzawa
Shizuoka University

1. Introduction In energy harvesting, environmental energy is converted into electric power. Thermoelectric generator (TEG) generates power from the flow of the heat. Because the output voltage of TEG is generally too small to directly drive integrated circuits, it is necessary to place boost converters between TEG and ICs for IoT [1]. To obtain sufficient power, TEG is composed of several units connected in series and in parallel [2]. Small form-factor TEG and booster circuits are required for low cost IoT edge devices. In [3], an optimum design of extremely low-voltage booster charge pumps (CPs) was proposed under the condition that the output voltage and current are given. In [4], a design of CP for TEG was proposed to determine the optimum number of stages for a desired output. In this paper, a method to minimize the TEG area is proposed.

2. Proposed optimum design Fig. 1 shows a system for IoT edge devices including TEG, CP and ICs for IoT. Parameters in this work are defined as follows; V_{PP}: output voltage of CP, I_{PP}: output current of CP, I_{DD}: input current of CP, V_{DD}: input voltage of CP (output voltage of TEG), I_{TEG}: output current of TEG, R_{TEG}: internal resistance of TEG, V_{OC}: open circuit voltage of TEG. One can design CP as a function of V_{DD} so as to have the largest power efficiency based on [3]. The input characteristics of the CP are shown by open circles in Fig. 2 when $V_{PP} = 3\text{V}, I_{PP} = 30\mu\text{A}$. The circuit system is in steady state at an operating point where $I_{DD} = I_{TEG} \equiv I_{OP}$ at $V_{DD} = V_{OP}$. The TEG area is proportional to the product of the serial number L of TEG elements and the parallel number M, $(L \times M)$. V_{OC} and R_{TEG} are proportional to L and L/M, respectively [2]. Thus, the TEG area can be evaluated with $V_{OC} \times V_{OC}/R_{TEG}$, which becomes (1) with $R_{TEG} = (V_{OC} - V_{OP})/I_{OP}$. Fig. 2 also shows the output characteristics of TEG. One can draw the lines which pass an operating point as A or B. Among them, only one line (A in this example) can have the minimum area when its V_{OC} is $2V_{OP}$. Eq.(1) can be minimized to be (2) with $V_{OC} = 2V_{OP}$ under power matching. Thus, when the upper bound of V_{OC} is V_{OC_MAX}, the TEG area is evaluated with P_{AV} defined with (1) or (2). As a result, the TEG area is proportional to the input power of the CP.

$$P_{AV} \equiv \begin{cases} \dfrac{V_{OC}^2 I_{OP}}{V_{OC} - V_{OP}} & \left(V_{OP} \geq \dfrac{V_{OC\_MAX}}{2}\right) \quad (1) \\ 4V_{OP}I_{OP} & \left(V_{OP} \leq \dfrac{V_{OC\_MAX}}{2}\right) \quad (2) \end{cases}$$

Following the above procedure, the TEG and CP areas are estimated under the condition of $V_{PP} = 3\text{V}, I_{PP} = 30\mu\text{A}$ and $V_{OC\_MAX} = 1.5\text{V}$, as shown in Fig. 3. The TEG area was calculated with (1) or (2) depending on a value of V_{OP}, which is normalized by the minimum value. The CP area was calculated based on the parameters used in [3] at each V_{OP} in Fig. 2.

As shown in Fig. 3, the CP area is not a smooth function of V_{DD} because the number of stages of CP is discrete. Moreover, the CP area increases as V_{DD} once the number of stages becomes one. This is because the efficiency decreases after the number of stages reaches one. The TEG area is close to the minimum between 0.2V and 1V in V_{DD}. For $V_{DD} = 1\text{V}$ or higher, the TEG area increases. This is because V_{OC} is fixed at V_{OC_MAX}. As a result, V_{DD} around 1V seems to be optimum in terms of the TEG and CP areas in this demonstration. The optimum values for $V_{OP} = 1\text{V}$ were the number of stages of 4, the capacitance per stage of 38pF and the clock frequency of 2.8MHz for CP and $V_{OC} = 1.5\text{V}$ and $R_{TEG} = 2.5\text{k}\Omega$ for TEG.

3. Validation To validate the proposed design procedure, SPICE simulation was done for the system of TEG and CP. The output characteristics of CP was also simulated, resulting in Fig. 4. Both the output impedance and maximum output voltage are in good agreement with the SPICE results with an error of $< 1\%$. The TEG and CP had an operating point V_{OP} of 1V.

4. Conclusion We proposed an optimum design for determining the minimum TEG area when the output voltage and current of CP are given. The demonstration showed that the TEG and CP areas were minimized around $V_{OP} = 1\text{V}$ under the condition of $V_{PP} = 3\text{V}, I_{PP} = 30\mu\text{A}$ and $V_{OC\_MAX} = 1.5\text{V}$.

5. References

[1] S. Priya, et al. “Energy Harvesting Technologies” p335, 2009.
[2] Y. Li, et al., IEEE Electron Device Letters, Vol. 32, No. 5, 2011.
[3] S. Tokuda, et al, IEICE general conference, 2018.
[4] T. Tanzawa, IEEE ICECS, pp. 327-330, Dec. 2014.

Acknowledgement
This work is supported by Zeon Corp., VDEC, Synopsys, Inc., Cadence Design Systems and Micron foundation, Inc.

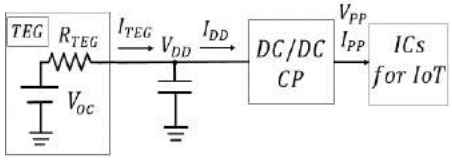

Fig. 1. Block diagram of IoT edge devices

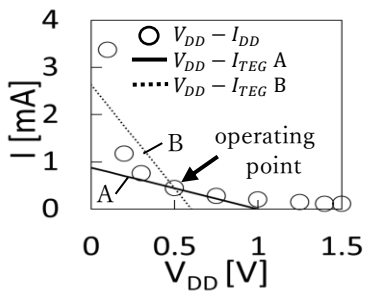

Fig. 2. $V_{DD} - I_{DD}$ and $V_{DD} - I_{TEG}$

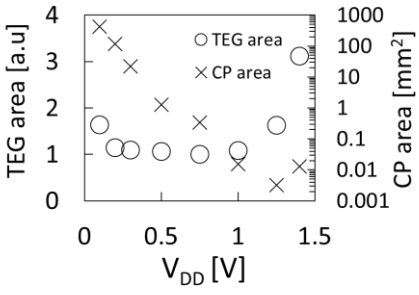

Fig. 3. V_{DD} − TEG area, CP area

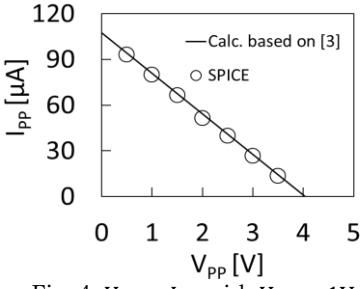

Fig. 4. $V_{PP} - I_{PP}$ with $V_{OP} = 1\text{V}$