Toward a Minimum-Operating-Voltage Design of DC-DC Charge Pump Circuits for Energy Harvesting

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Toward a Minimum-Operating-Voltage Design of DC-DC Charge Pump Circuits for Energy Harvesting

Shugo Tokuda, and Toru Tanzawa, *Fellow IEEE*
Shizuoka University, Hamamatsu 432-8011, Japan

***Abstract*— This paper expands upon the circuit model of DC-DC charge pump circuits to include the reverse leakage current which becomes significant at extremely low voltages in energy harvesting. The paper proposes a design flow to determine all the design parameters of charge pump circuits operating in sub-threshold region such as a clock frequency, stage capacitor size, rectifying device size and number of stages based on the model. The methodology is demonstrated and verified by SPICE simulation. By using the proposed flow under given conditions, circuit designers can numerically obtain trade-offs between power supply voltage, circuit area and power efficiency of DC-DC charge pump circuits to design energy harvesting systems**

***Index Terms*—DC-DC, Charge pump, Energy harvesting, Voltage multiplier, Reverse leakage, Schottky-barrier diode**

NOMENCLATURE

Parameter	Definition
A_{cap}	Capacitor area per stage
$A_{CP}{}^{INIT}$	Initial condition of A_{CP}
A_{CP}	Total area of a charge pump circuit
A_D	Area of the diode
C	Capacitance of a capacitor per stage
C_J	Junction capacitance of the diode
C_{OX}	Capacitance density of C
f	Clock frequency
I_{DD}	Input current
I_s	Diode saturation current
I_{OUT}	Average output current
I_{PP}	I_{OUT} at V_{PP}
I_{PP_TGT}	Target I_{PP} at V_{PP}
N	Number of stages or number of capacitors
N_D	Number of diodes connected in parallel per stage
R_{PMP}	Output resistance of the pump
S_F	Scaling factor
V_{DD}	Input DC voltage
V_{MAX}	Maximum attainable voltage
V_{OUT}	Output DC voltage
V_{PP}	Output voltage at an operating point
V_T	Thermal voltage
$V_{TH}{}^{EFF}$	Effective threshold voltage of switching diodes
$\alpha_{T(B)}C$	Parasitic capacitance on the upper (lower) side of capacitors
η	Power conversion efficiency of the pump

S. Tokuda is now with Nippon Ceramic Co. Ltd.

I. INTRODUCTION

Energy harvesting is becoming increasingly important for autonomous sensor networks and implantable electronic devices. Photovoltaic (PV) cells and thermoelectric generators (TEGs) are used as DC power sources. The DC voltages are not high enough to drive integrated circuits (ICs) directly. As a result, integrated switched-capacitor Dickson charge pump circuits [1] are used to boost the voltages generated by the energy transducers, especially in the applications where a small form factor is a primal concern, as shown in Fig. 1 [2-3]. DC-DC switched-capacitor charge pump circuits eliminate the need for an inductor. To minimize the operation current for control circuits and the oscillator, the switches are realized by simple diodes, e.g., p-n diodes, Schottky barrier diodes, or metal–oxide–semiconductor field-effect transistors (MOSFETs), whose gate terminals are connected with their drain terminals or with auxiliary sub-circuits.

Circuit models of charge pump circuits have been proposed [4-8]. In [4] and [5], dynamic models are proposed to estimate the rise time of the charge pump circuits in the slow switching limit where charges are fully transferred from one stage to the next with a relatively slow clock input. Steady state models representing wide frequency operations have been also shown in cases where the switching MOSFETs operate linear region [6-7] and where the diodes are used as the switching devices [8]. Rectifying switching circuits have been proposed to operate at extremely low voltages for UHF or RF energy harvesting in CMOS technology [9-11]. The aim is at compensating the threshold voltages of the switching transistors. Charge pump circuits need to be designed so as to have small circuit area and high power conversion efficiency. When one chooses the number of stages to be about 1.6 times larger than the minimum number of stages, both the circuit area and power efficiency are optimized in a balanced way [12]. One can determine all the circuit parameters including the clock frequency and the size of the switching MOS transistors based on the design flow shown in [13] where the reverse leakage current is not a matter. Design window was explored for DC-DC charge pump circuits in energy harvesting to find trade-offs between supply voltage, circuit area and power efficiency in [14]. But, the reverse leakage was not taken into consideration. Effects of the reverse leakage on the performance were discussed in [15], but it didn't show how the design parameters could be determined.

This paper expands upon the circuit model of DC-DC charge pump circuits to include the reverse leakage current

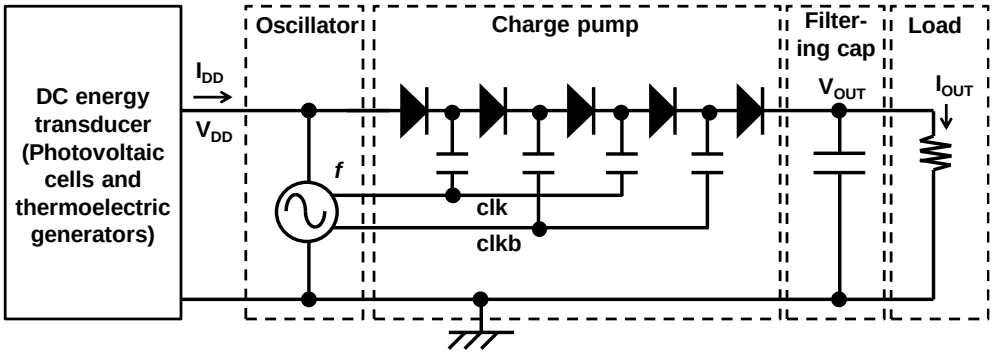

Fig. 1 Diagram of an EH system

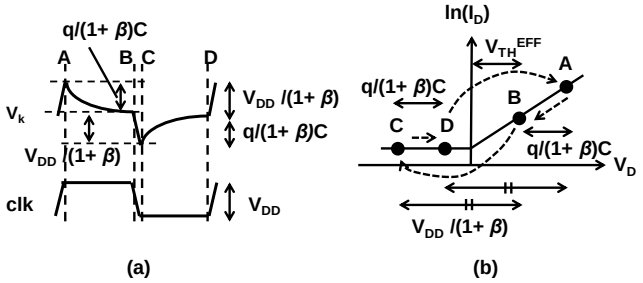

Fig. 2 Voltage waveform (a) and trajectory of a diode in I-V plane (b)

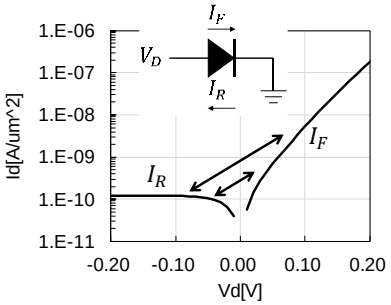

Fig. 3 I-V characteristics of a Shottky barrier diode

which becomes significant at extremely low voltages in energy harvesting. The paper proposes a design flow to determine all the design parameters of charge pump circuits operating in sub-threshold region such as a clock frequency, stage capacitor size, rectifying device size and number of stages based on the model. The methodology is demonstrated and verified by SPICE simulation.

II. Leakage Current Aware Circuit Model

Figs. 2 (a) and (b) respectively show the waveform of a *k*-th nodal voltage V_k and a trajectory of a switching diode in the I-V plane. The diode starts conducting at the clock rise edge as shown by point *A* [8]. According to (1), an amount of charges is transferred to a next stage. Even though a diode is assumed as switching devices, a MOSFET operating in subthreshold region is also valid in the below discussion because *I-V* curve is basically the same form as (1). The capacitor voltage decreases by $q/(1+\beta)C$, where q is the charge transferred to the output terminal in a period. At the falling edge *B*, one can have a finite residual potential as shown by V_{TH}^{EFF} which represents the effective threshold voltage. A voltage swing of V_{DD} in *clk* translates into that of the nodal voltage of $V_{DD}/(1+\beta)$ in the transition from point *B* to *C*. Charge transfer from the previous stage increases the capacitor voltage by $q/(1+\beta)C$ in the transition from point *C* to *D*. Another voltage swing of V_{DD} in *clk* translates into that of the nodal voltage of $V_{DD}/(1+\beta)$ in the transition from point *D* to the original *A*. The diode flows a reverse leakage current when V_D is negative, which is considered to be significant in this paper, as shown in Fig. 3. *N* first-order differential equations for $V_k(t)$ were exactly solved to find the $I_{OUT}-V_{OUT}$ curve, which was approximated by (2) – (5). The first term of (5) indicates a residual voltage due to a limited drive capability of the switching diode per given capacitance [8]. The second term is newly added for taking the reverse leakage current into account, which was not considered in [14]. For example, when *2k*-th diodes of the charge pump circuit in Fig. 1 are operating in forward bias region, *(2k+1)*-th diodes are subjected in reverse bias region. A constant reverse bias current of I_S continues to flow during a half period of *1/(2f)*. Thus, a voltage loss due to the reverse leakage current is estimated by the second term of (5).

$$I_D = I_S \exp(V_D / V_T) \tag{1}$$

$$I_{OUT} = (V_{MAX} - V_{OUT}) / R_{PMP} \tag{2}$$

$$R_{PMP} = \frac{N}{(1+\alpha_T)Cf} \tag{3}$$

$$V_{MAX} = (\frac{N}{1+\alpha_T} + 1)V_{DD} - (N+1)V_{TH}^{EFF} \tag{4}$$

$$V_{TH}^{EFF} = V_T \ln(4^{\frac{1}{N+1}} \frac{(1+\alpha_T) fCV_T}{I_S}) + \frac{I_S}{2fC(1+\alpha_T)} \tag{5}$$

The input current of DC-DC charge pump circuits is given by the first two terms of (6) in [13]. The first term is associated with the charges input by the clock buffers and through the input terminal. The second term represents the currents for the parasitic capacitance of the capacitors. The third term corresponding to the reverse leakage through the switching diodes in a half cycle is newly added. The left most diode of the charge pump in Fig. 1 doesn't contribute to I_{DD} because the charges due to the reverse leakage return to V_{DD}. Thus, *N* diodes increase I_{DD} by the third term. Power efficiency is defined by (7).

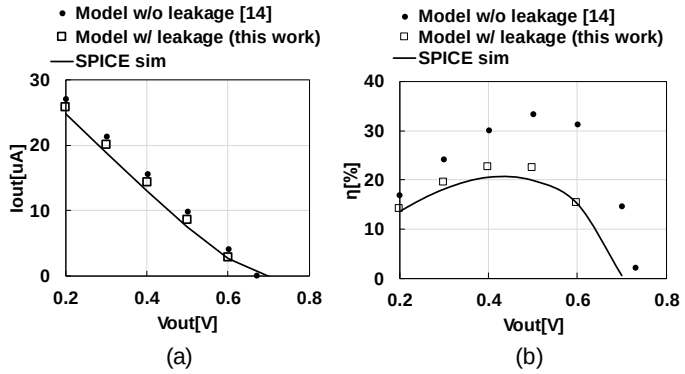

Fig. 4 I_{OUT} – V_{OUT} (a) and η – V_{OUT} (b) in case of V_{DD} = 0.1V, V_{PP} = 0.5V, N = 9, C = 2.2nF, f = 160k-Hz, N_D = 5k.

$$I_{DD} = (\frac{N}{1+\alpha_T} + 1)I_{PP} + (\frac{\alpha_T}{1+\alpha_T} + \alpha_B) fNCV_{DD} + NI_S / 2 \quad (6)$$

$$\eta = (I_{PP}V_{PP}) / (I_{IDD}V_{DD}) \quad (7)$$

To validate the above model, SPICE simulation was made based on the device parameters of a Shottky barrier diode in [15], I_S = 0.1nA/μm^2, V_T = 25mV, A_D = 10μm^2 and C_J = 3.5fF/μm^2. Figs. 4 (a) and (b) respectively show I_{OUT} – V_{OUT} and η – V_{OUT} in case of V_{DD} = 0.1V, V_{PP} = 0.5V, N = 9, C = 2.2nF, f = 160k-Hz, N_D = 5k. The characteristics calculated by the proposed model including the reverse leakage current is in good agreement with SPICE simulation results.

III. PROPOSED DESIGN FLOW

In this section, a design flow is proposed to provide trade-off between the circuit area and power efficiency under the condition that the charge pump outputs a target current at given input and output voltages. Design starts with a given circuit area A_{CP}^{INIT}. The other design parameters are figured out under the condition where the values of V_{TH}^{EFF} and N_D are assumed, as follows. One can pick up the best set of design parameters per one's criteria such as circuit area is minimal, power efficiency is maximal, or circuit area and power efficiency are optimal in a balanced way.

The minimum number of stages to generate V_{PP} at I_{PP} = 0 is given by (8) from (2) and (4). The optimum number of stages to make a balance between circuit area and power efficiency is given by (9) [12], where [X] indicates a rounded integer number of X. At the initial design stage, one cannot help setting α_T be zero in (8) and determine N_{OPT} by (9). The capacitance value of each pump capacitor is calculated by (10). The number of capacitors is N_{OPT} while that of diodes is N_{OPT} +1. The top plate parasitic capacitance is then estimated by (11). In the second design stage, one can redo the flow from (8) through (10) with a finite α_T of (11). Then, one needs to find a solution for fC of (5) numerically because the other parameters are given or identified at this point. Finally, f is determined with (10). (2)-(4) provide I_{PP}. As a result, the circuit area required to output I_{PP_TGT} can be calculated by using (11) and (13). (7) and (13) are primal outputs in this design flow.

$$N_{MIN} = (V_{PP} - V_{DD} + V_{TH}^{EFF}) / (V_{DD} / (1+\alpha_T) - V_{TH}^{EFF}) \quad (8)$$

Table I design and device parameters for demonstration

Parameter	Values
V_{DD}	0.1-0.3V
α_B	0.1
V_T	25mV
I_S	0.1nA/μm^2
A_D	10μm^2
C_{OX}	10fF/μm^2
C_J	3.5fF per diode
V_{PP}	0.5V
I_{PP_TGT}	10μA

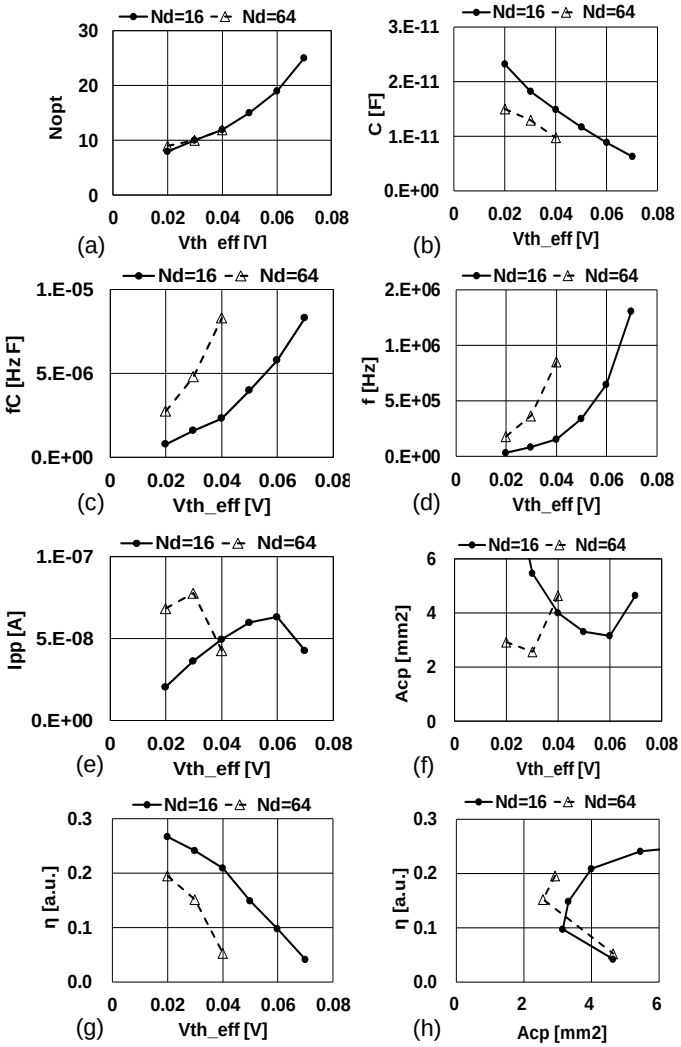

Fig. 5 Demonstrated dependence of design parameters on V_{TH}^{EFF} and N_D in case of V_{DD} = 0.1V, V_{PP} = 0.5V, A_{CP}^{INIT} = 2 x 10^4 μm^2 (a)-(e) and the resultant A_{CP}, η and A_{CP} – η curve for I_{PP_TGT} = 10μA (f)-(h).

$$N_{OPT} = [1.6N_{MIN}] \quad (9)$$

$$C = (A_{CP}^{INIT} / N_{OPT} - (1+1/N_{OPT})N_D A_D)C_{OX} \quad (10)$$

$$\alpha_T = N_D A_D C_J / C \quad (11)$$

$$S_F = I_{PP\_TGT} / I_{PP} \quad (12)$$

$$A_{CP} = S_F A_{CP}^{INIT} \quad (13)$$

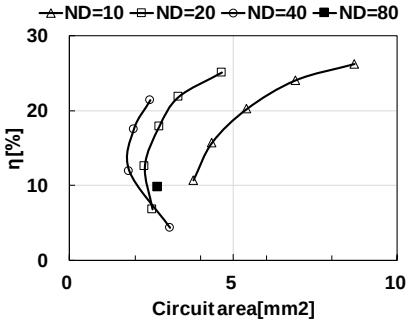

Fig. 6 $A_{CP}-\eta$ curves with various N_D values for V_{DD} = 0.1V, V_{PP} = 0.5V and I_{PP_TGT} = 10μA.

In energy harvesting, V_{DD} could be a design parameter rather than a given condition. One can run the above flow at different V_{DD} to provide trade-offs between V_{DD}, A_{CP} and η.

IV. DEMONSTRATION

Demonstration was performed with the parameters shown in Table I, where a Schottky barrier diode [16] and 1.8V CMOS are assumed. Figs. 5 (a)-(e) show N_{OPT}, C, fC, f and I_{PP} as a function of V_{TH}^{EFF} with N_D of 16 or 64 in case of V_{DD} = 0.1V, V_{PP} = 0.5V, A_{CP}^{INIT} = 2 x 10^4 μm^2. Then, A_{CP} and η are estimated to have I_{PP_TGT} of 10μA as shown in Figs. (f) and (g), respectively. Finally, one can plot $A_{CP}-\eta$ curve in Fig. 5(h). Fig. 6 shows $A_{CP}-\eta$ curves with various N_D values for V_{DD} = 0.1V, V_{PP} = 0.5V and I_{PP_TGT} = 10μA. Every point in Fig. 6 has a different design parameter set of N, C, N_D, and f. One can select a single design parameter set in the curves for each own criteria. For example, one prioritizes circuit area more than power efficiecny while another does power efficiency than circuit area. The third criteria might be the one which maximizes a value of η /A_{CP} indicating a balanced design on circuit area and power efficiecny. Fig. 7 plots balanced designs per V_{DD}. The model caluculations are in good agreement with SPICE simulation within an error of 13%. One can specify the minimum V_{DD} under one's constraint on circuit area and power efficiecny with such graphs.

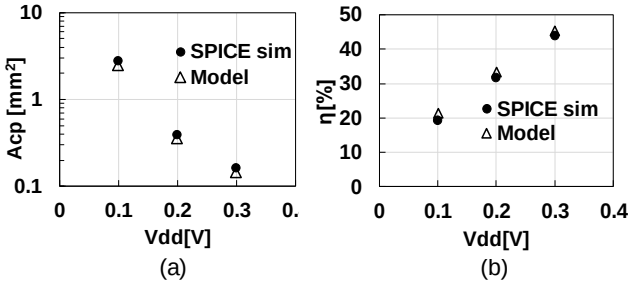

Fig. 7 Trade-offs between V_{DD} and A_{TOT} (a) and between V_{DD} and η (b).

V. CONCLUSION

A charge pump model was expanded to include the impact of the reverse leakage current for extremely low-voltage operation in energy harvesting. Based on the model, a design flow was proposed to provide the trade-off between supply voltage, circuit area and power efficiency to system designers.

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