Development of a two-tap time-resolved CMOS lock-in pixel image sensor with high charge storability and low temporal noise

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***Abstract*—A high charge storability and low noise performance are both of the significant parameters for the high sensitivity time-resolved (TR) CMOS image sensors (CISs). To achieve these, we have developed the high performance TR lock-in pixel CIS embedded with two in-pixel storage-diodes (SDs). For fast charge transfer from photodiode (PD) to SDs, a lateral electric field charge modulator (LEFM) is used for the developed lock-in pixel. As a result, the time-resolved CIS achieves a very large SD-FWC of approximately 7ke-, low temporal noise of 1.2e-rms at 20fps with true correlated double sampling (CDS) operation, and fast intrinsic response less than 500ps at 635nm. The proposed TR imager has an effective pixel array of 128(H)×256(V) and a pixel size of 11.2×11.2μm^2. The sensor chip is fabricated by Dongbu HiTek 1-poly 4-metal 0.11μm CIS process technology.**

Keywords—Time-resolved CMOS image sensor (CIS), lock-in pixel, large full well capacity (FWC), low temporal random noise, fluorescence lifetime imaging microscopy (FLIM), biomedical imaging

I. INTRODUCTION

A time-resolved (TR) imaging technique [1]-[9] is one of very effective analysis methods in the biomedical applications. Charge-coupled devices (CCDs) [3] and single-photon avalanche diodes (SPADs) [3], [4], [9] are the representative imaging devices for TR measurements. In particular, SPAD-based TR imagers have a high single-photon sensitivity and a good noise robustness as well as excellent time-resolution performance, normally less than 100ps. However, they typically consist of a SPAD array with a complex pixel circuitry, such as the time-to-digital converters (TDCs), digital integrators to amplify signals, and readout circuits. To implement the high photon-counting rate, a large number of TDCs and digital integrators are required. For this reason, the spatial resolution of the SPAD-based TR imagers is limited. A high performance two-tap TR CMOS image sensor (CIS) has been reported [7], [8], and it has the attractive sensor characteristics, e.g., a high time resolution, a relative low temporal noise, and a high signal utilization efficiency of almost 100%, which are achieved by the use of two time windows (TWs). However, this imager has a small full well capacity (FWC) of each storage diode (SD) and its noise performance is still not enough for the living cell imaging and other biomedical applications. A large FWC allows the TR imagers to attain a high signal-to-noise ratio (SNR), and it makes possible to achieve a higher time-resolution.

This paper presents a high charge storability, low temporal noise, TR CIS with two-tap lock-in pixel using lateral electric field charge modulator (LEFM) and two-stage charge transfer techniques. The FWC of the prototype TR CIS is 2.6 times larger than that of [8], and the noise performance is also much improved. As a result, the sensor's signal-detection-range is extended as well as the improvement of a SNR.

II. PIXEL STURCTURE AND OPERATION

To design the multi-tap CMOS lock-in pixel for the higher time resolving capability, several techniques are essential, such as a lock-in operation, fast charge transfer technique using LEFM, and two-stage charge transfer for achieving a true correlated double sampling (CDS) operation. In this section, the essential techniques for TR pixel design will be introduced, and then the detailed pixel architecture and its operation are explained.

A. Lock-in operation

A lock-in pixel operation [5]-[8], [10]-[12] is a very practical technique and fundamental to achieve a time-resolving imaging with CIS technologies. This makes it possible to extend the application in the fields of real-time biomedical imaging. A conventional lock-in pixel detects and transfers the photo-induced charges to one or more signal charge accumulation regions in synchronization with the modulated light through the channel generated by the gate of metal-oxide-semiconductor field-effect transistor (MOSFET).

Fig. 1 shows the function of the multi-tap lock-in pixel. Firstly, the photons arrive at the photodiode (PD). At that time, a photo-current (i_p) generated in the PD is modulated by operating the TWs (TW_1 to TW_n; n is the number of taps), and the modulated signals are stored in the integrators. Through these operations, a time-dependent component contained in the photo-induced signal charges is extracted from each pixel of the image sensor.

This work was supported in part by the Grant-in-Aid for Scientific Research (S) under Grant 25220905 through the Ministry of Education, Culture, Sports, Science and Technology (MEXT), in part by the MEXT/JST COI-STREAM program, in part by the Reginal-Innovation Ecosystem Program, and in part by the VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc. and Mentor Graphics, Inc. Also, authors appreciate Dongbu HiTek for CIS chip fabrication.

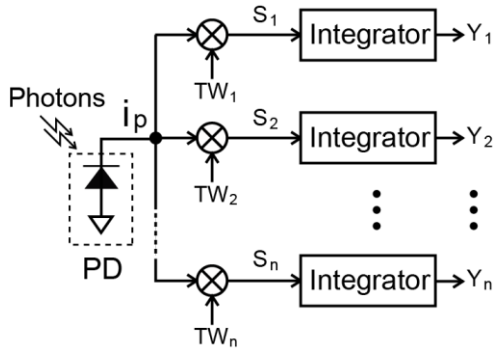
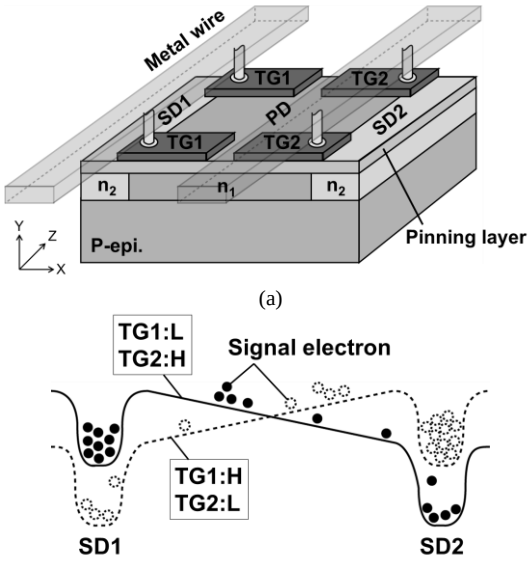


Fig. 1. Conceptual diagram of a lock-in pixel with multiple time-windows.



(a)

(b)

Fig. 2. Lateral electric field charge modulator. (a) Simplified two-tap lock-in pixel with LEFM structure. (b) X-directional potential diagram.

B. Fast charge transfer technique using LEFM

Despite the advantage of lock-in operation for extracting the temporal information, the conventional lock-in pixel image sensors with a direct gating modulation have some issues such as a relatively low speed charge transfer and gating-noise intrusion to final integrated photo-signal. For instance, in case of the charge transfer through a MOS poly-gate channel, it is difficult to modulate the electric field for high-speed directional charge transfer to charge storage, and a potential barrier may be generated at the edge of the MOS poly-gate in certain pixels that must be treated a defective because of the incongruity of single-electron transfer.

To solve these issues, we utilize the LEFM structure [13] as shown in Fig. 2. This shows the simplified two-tap lock-in pixel with LEFM and its x-directional potential diagrams with different gating conditions. The pixel has a PD (n_1 region), and two SDs (n_2 regions), two sets of transfer gates (TG1 and TG2) for generating the lateral electric field. Two different n-type layers (n_1 and n_2) and p+ pinning layer formed on a lightly doped p-type epitaxial layer to improve the modulation efficiency are used for two-tap lock-in pixel with true-CDS operation. To control the electric field in x-direction, a positive

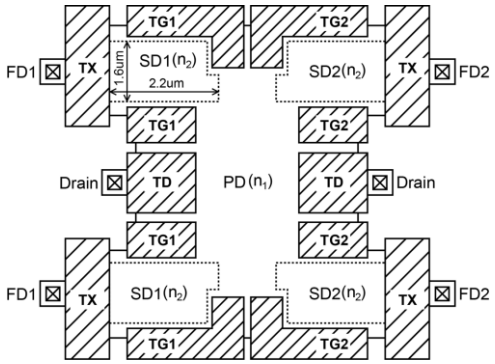


Fig. 3. Developed 2-tap lock-in pixel with LEFM.

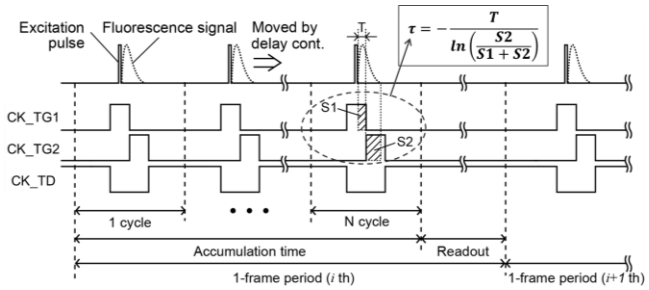


Fig. 4. Timing diagram for time-resolved measurement using developed 2-tap CMOS lock-in pixel.

voltage and a negative voltage are supplied for the charge modulation. By supplying these gate voltages, depleted potential can be modulated while maintaining the potential barrier between the edge of gates and channel on the PD. Fig. 2(b) shows the potential diagram along horizontal direction of pixel structure. As can be seen from Fig. 2(b), the signal electrons generated in the PD are transferred to SD2 when a negative voltage (L) and positive voltage (H) are used for TG1 and TG2, respectively. At this time, by using these gate supply voltages, a very steep potential slope is formed, and it allows the high-speed charge transfer in each pixel. In addition, thanks to the LEFM structure, the signal electrons can be transferred to the storages without going under poly-gates. This means that the signal is accumulated in the storages without the additional noise component generated by gating, even if a charge modulation process is repeated many times over within a one horizontal readout period.

C. Pixel operation

Fig. 3 shows the proposed pixel layout. The pixel comprises a PD, two SDs, and three set of gates (TG1, TG2, and TD). As mentioned above, TGs control the electric fields on channel of PD and TD is used for draining the undesirable signal generated in PD during the signal readout period.

Fig. 4 shows the simplified timing diagram for extracting the temporal information using the proposed lock-in pixel imager. The total timing is composed of two periods: 1) accumulation period for integrating the charge to SDs, and 2) readout period for reading out the accumulated signal in SDs through the CMS-based readout circuits [14], [15]. In the accumulation period, high levels are given to CK_TG1 and CK_TG2 for transferring the charge to SDs from the PD, and CK_TD is set to high value. To obtain a high SNR, many

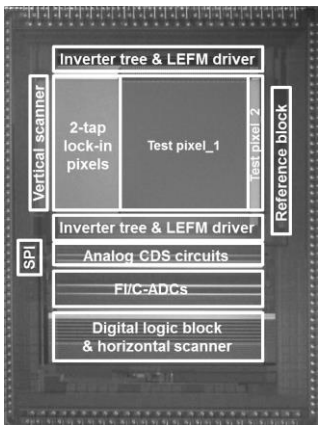


Fig. 5. Chip micrograph.

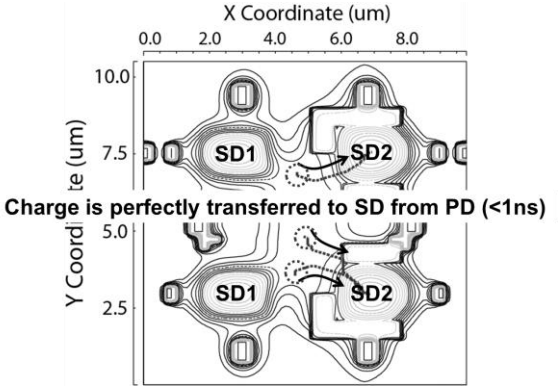


Fig. 6. Simulated signal charge travelling path on the pixel layout (@TG1=TD=-1V, TG2=2V).

cycles are repeated. Eventually, the accumulated signals in the SDs are read out through high performance column readout circuitry after finishing the accumulation period. During the readout period, CK_TD is always set to high; on the other hand, CK_TG1 and CK_TG2 are set to low.

In addition, the two-tap pixel structure can be used to realize the real-time lifetime measurement system [7]. As can be seen from Fig. 4, the lifetime is measured with the two TWs per single frame, resulting in two signals, S1 and S2, being stored in the SDs. Two TWs using clocks CK_TG1 and CK_TG2 control the capture timing of the accumulated signals, respectively. S2 is expressed as the time-integral of charge from 0 to T. S2 is expressed as the integral from T to infinity. Using these two signals, the lifetime of the specimen, which has mono-exponential decaying component, can be easily and quickly calculated in comparison with typical lifetime measurement method using a TW scanning.

III. Experimental Results

A time-resolved CIS with 128(H)×256(V) lock-in pixels is implemented by Dongbu HiTek 1-poly 4-metal 0.11μm CIS process. The chip micrograph of the developed CIS is shown in Fig. 5. It consists of a pixel array, inverter tree with LEFM driver array, low-noise column-parallel analog-to-digital converters (ADCs) based on CMS operation, a logic block for signal processing, scanners for pixel addressing.

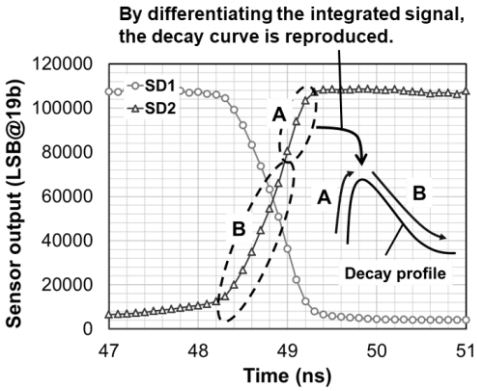


Fig. 7. Measurement results scanned by a pulse laser diode. (@374nm laser diode scanning).

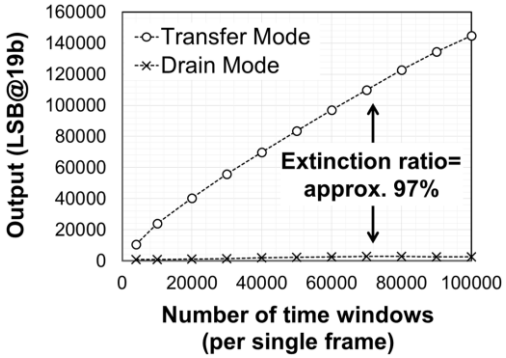


Fig. 8. Linearity graph of the prototype image sensor as a function of the number of TWs (@472nm LD, width of TW: 15ns).

The perfect and fast charge transfer performance is demonstrated by a two-dimensional device simulation. Fig. 6 shows the signal carrier travelling path on the designed pixel layout with equipotential lines during the charge transfer mode. The dotted circles denote the initial positions of signal carriers generated in the PD region and the dotted lines indicate the movement traces of each carrier. The transportation for all generated signal charges is completed in sub-nanosecond transfer time.

Fig. 7 shows the measurement result of the prototype two-tap TR CIS. This is an output signal of imager scanned by a pulse laser. As can be seen from the result, the time-gated pixel successfully worked and captured the signal by TWs. The time-dependent optical information can be extracted from these integrated signals.

The photo-electric conversion characteristic of the prototype image sensor is shown in Fig. 8. This is the linearity as a function of the number of TWs (width of TW: 15ns) at 472nm laser diode (pulse width: 120ps, maximum peak power: 48mW). In this measurement, the number of TWs increases from 4,000 to 100,000 with two conditions, transfer and drain modes. The result shows a very high extinction ratio (ER) of approximately 97%. A higher ER is the important performance of TR imagers for achieving the high time-resolution and the wide dynamic range. From the linearity plot, we can confirm a wide dynamic range (DR) and a large FWC at SD.

To demonstrate the time-resolving performance of the developed TR CIS, the fluorescence lifetime measurement is

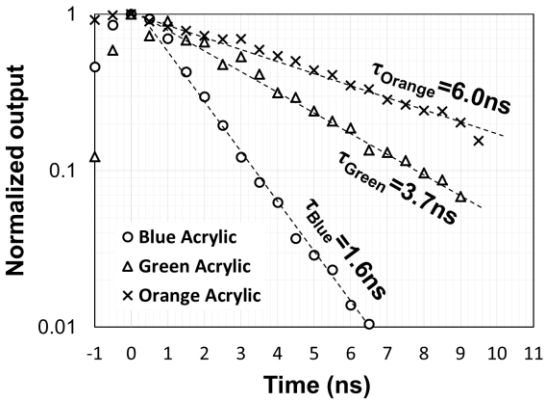


Fig. 9. Fluorescence lifetime measurement result with different types of fluorescent acrylic panels (@Ex. 374nm)

TABLE I
SENSOR PERFORMANCE

Parameter	Value
Process technology	0.11 μm 1P4M CIS process
Total area	7.0 (H) mm X 9.3 (V) mm
Number of effective pixels	128 (H) X 256 (V)
Pixel size	11.2 (H) μm X 11.2 (V) μm
Conversion gain	76.3 μV/e-
Full well capacity (@ SD)	6930 e-
Intrinsic response (@ 635nm)	460ps
Temporal random noise	1.17 e-rms (@ peak value, 20fps)
	1.20 e-rms (@ median value, 20fps)
Dynamic range	75.2 dB
Frame rate	20 fps

implemented with three different types of fluorescent acrylic panels as shown in Fig. 9. A 374nm laser diode (LD) is used for the excitation, and the optical band pass filter which is chosen for each acrylic panel is set in the fluorescence lifetime measurement system for filtering the excitation light and passing the emission light from the sample. The total exposure time for obtaining the one point is around 210ms. The measured lifetime of blue, green, and orange acrylic panels are 1.6ns, 3.7ns, and 6.0ns, respectively. These values are very close to the reference lifetimes, which were measured by a typical time-correlated single photon counting (TCSPC) system, without any compensation.

The sensor's specific performance is summarized in Table I. The size of the sensor chip including the TR lock-in pixels with two in-pixel storages is .7.0(H)×9.3(V)mm^2. The pixel size is 11.2×11.2μm^2 and the developed imager has a high conversion gain of 76.3V/e-, a large FWC of 6,930e-, and a wide DR of 75.2dB as well as a low temporal noise level of 1.2e-rms at median.

IV. CONCLUSION

We have developed and demonstrated a two-tap lock-in pixel CMOS image sensor which has a low temporal random noise and high charge storability. The proposed pixel has two output ports with the intermediate storages between PD and each FD node for cancelling the reset noise using a true-CDS operation and reducing the gating noise component. As a result, the time-resolved CMOS image sensor with single-electron noise level and extremely large in-pixel storage capacity are very effective and excellent candidate to apply in the life sciences and biological study.

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