A Pre-Emphasis Pulse Generator Insensitive to Process Variation for Driving Large Memory and Panel Display Arrays with Minimal Delay Time

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A Pre-Emphasis Pulse Generator Insensitive to Process Variation for Driving Large Memory and Panel Display Arrays with Minimal Delay Time

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***Abstract*— A pre-emphasis pulse generator is proposed which can provide minimal word-line or column-line delay time in a large memory array or panel display without calibration even under a large process variation. The optimum pre-emphasis pulse width is theoretically identified by monitoring the far-end of the delay line to reach a certain value which does not include the parasitic resistance and capacitance of the delay line but only includes an amount of overdrive. The circuit was fabricated together with the delay line in 0.18 µm 3V CMOS. Even with RC variation of 20%, the proposed circuit reduced the delay time by 60% with 60% overdrive in comparison with a fixed pre-emphasis pulse width without any calibration prior user operation or any special test sequence in die test. Sensitivity of a variation in a reference voltage and a comparator offset on the delay time is also discussed. Furthermore, the optimum detection level is presented in case that the resistance of driver and switch is as high as that of the delay line.**

Keywords*— *RC lines, Delay time, Pre-emphasis, Large memory, Panel display, Word-line, Column-line

NOMENCLATURE

c	Capacitance per unit length
$e(x,t)$	Voltage at a position x and a time t
E	Target voltage
r	Resistance per unit length
R_d	Total resistance of driver and switch
t_{delay}	Time for the slowest node voltage to reach βE
t_{delay_min}	Minimal t_{delay} when set by T_{opt}
T_{opt}	Optimum T_{pre} to minimize the delay time
T_{pre}	Pre-emphasis time
x	Delay line position (x = 0 for the nearest, x = l for the farthest)
α	Ratio of the pre-emphasis voltage to E
β	Error rate to E

I. Introduction

The delay time of word-lines (WLs) in a large memory array and column-lines (CLs) in a large panel display occupies a large part of the entire operation. It is a key to reduce the WL/CL delay time for high performance memory and panel display with large arrays. Therefore, pre-emphasis pulses are used in transmission line [1], display [2] and memory [3], to reduce the wiring RC delay time. In [4], it is shown that the delay time can be theoretically reduced to one-forth under the condition of α = 2 and β = 0.01. WL and CL are fabricated in a minimum pitch to maximize the capacity density. As a result, the variations in the parasitic resistance and capacitance can become as large as 10%. Since the optimum pre-emphasis pulse width depends on the parasitic resistance and capacitance values, a compensation circuit was required to compensate the process variation. In [2], after the test pre-emphasis pulse is input, the column line is floated and the voltage is measured after the charges are redistributed. Various pre-emphasis pulses are tested to find an optimum pre-emphasis voltage prior to user operation. A reduction in the setting time by 27% to 40% is realized for RC variation of ± 18%. In [3], test structures for measuring the WL resistance are placed in each of the top and bottom sides of the cell array. WL resistance is measured during die test and the pre-emphasis pulse is optimally adjusted depending on the measured value. A reduction in the setting time of about 45% is realized both lower and upper word lines. However, those design techniques require additional test cost and test structures to improve the performance.

In this paper, we propose a pre-emphasis pulse generator which does not require any calibration for performance improvement. In section II, a circuit theory for minimal delay time with a pre-emphasis pulse is proposed. It is also shown that the voltage at the farthest node of the delay line such as WL and CL does not depend on the parasitic resistance and capacitance when the pre-emphasis pulse is controlled to be an optimum. In section III, what building blocks will be required to realize the optimum pulse is discussed. Based on that, a pre-emphasis pulse driver circuit is proposed to be insensitive to process and temperature variation, which can eliminate addition calibration process and test. Measured

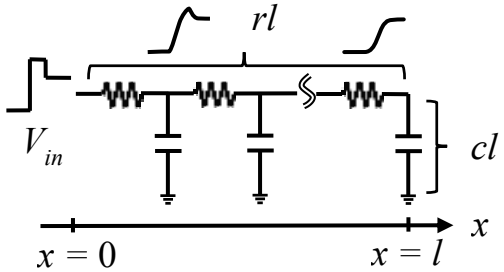

Fig. 1. Equivalent circuit of RC delay line (WL or CL)

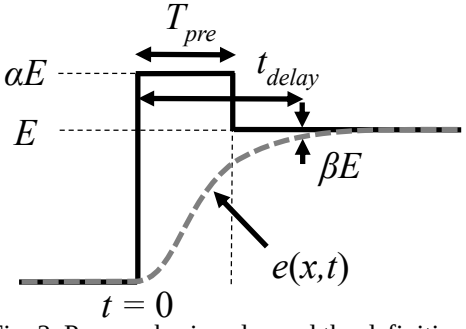

Fig. 2. Pre-emphasis pulse and the definition of the design parameters

results are shown in section IV. How the variation in the reference voltage or the input offset of the comparator can affect the delay time is also studied. Section V discusses the impact of the resistance of driver and switch on the delay time.

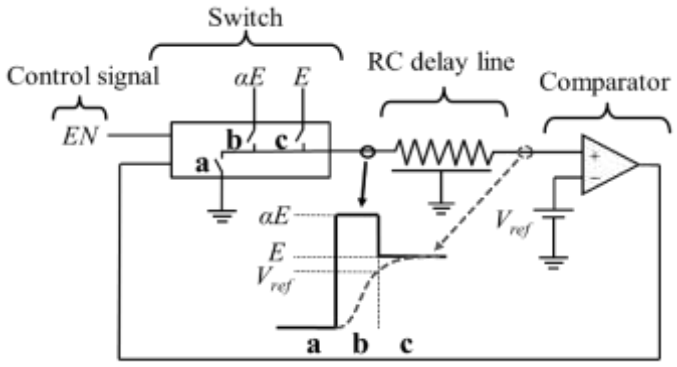

Fig. 3. Proposed circuit

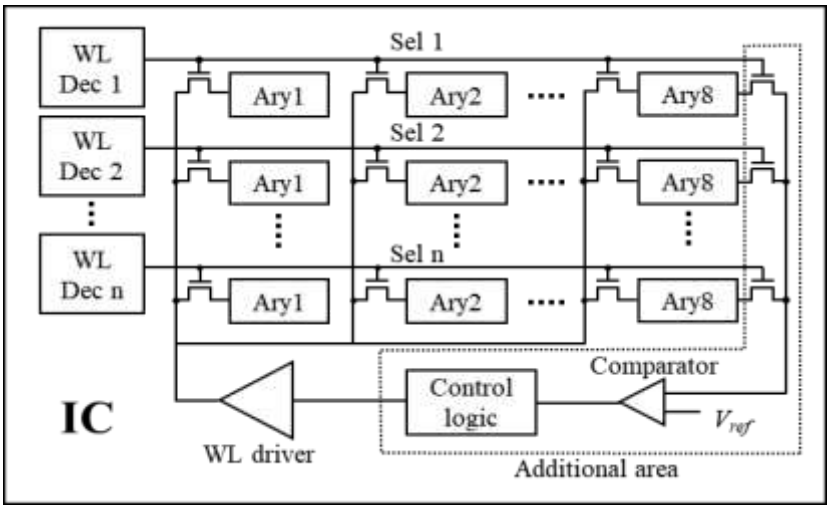

Fig. 4. Proposed circuit configuration on an IC

II. Theory for Minimal Delay Time

Fig. 1 shows an equivalent circuit of a delay line, i.e., WL in memory or CL in display. Fig. 2 shows a pre-emphasis pulse waveform and defines its design parameters. In [4], it is shown that the voltage at any position "x" during pre-emphasis period is exactly given by (1). Equation (1) is approximated with $k = 0$ to be (2). It is also shown in [4] that an optimum pre-emphasis pulse width which provides a minimal delay time is given by (3), where τ is a time constant given by $4rcl^2/\pi^2$. When one inputs (3) and $x = l$ into (2), one can have (4).

$$e(x,t) = \alpha E - \frac{4\alpha E}{\pi}\sum_{k=0}^{\infty}\frac{1}{2k+1}e^{\frac{-(2k+1)^2 t}{\tau}}\sin\frac{(2k+1)\pi x}{2l} \quad t \le T_{pre} \tag{1}$$

$$e(x,t) \approx \alpha E - \frac{4\alpha E}{\pi}e^{\frac{-t}{\tau}}\sin\frac{\pi x}{2l} \quad t \le T_{pre} \tag{2}$$

$$T_{opt} \approx \tau \ln\frac{\alpha}{\alpha - 1} \tag{3}$$

$$e(l, T_{opt}) \approx \left(1 - \frac{4(\alpha-1)}{\pi\alpha}\right)\alpha E \equiv V_{ref} \tag{4}$$

Equation (4) indicates that the delay time becomes minimal if the pre-emphasis pulse is switched to a target voltage when the voltage at the far-end reaches V_{ref}. Equation (4) does not include r and c. Therefore, even if the value of r or c changes due to process and temperature variation, V_{ref} does not need to be modified.

III. Proposed Driving Circuit

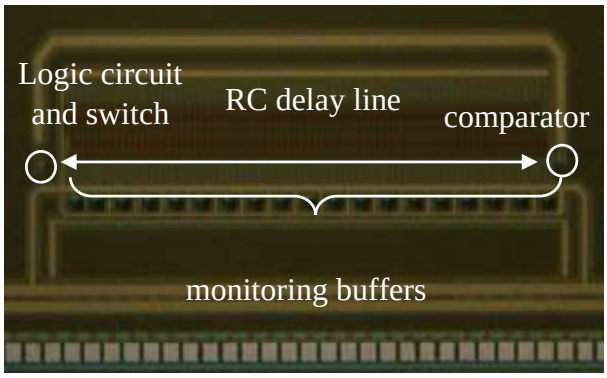

Fig. 5. Chip micrograph

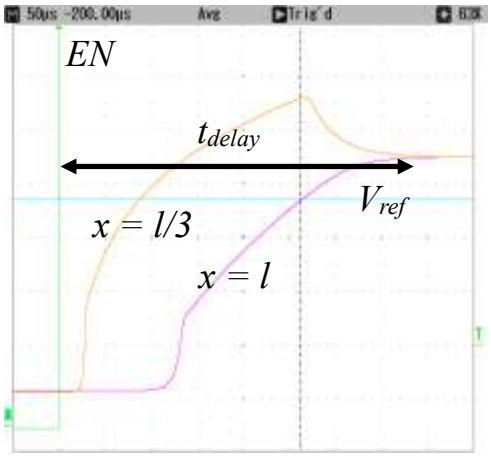

Fig. 6. Measured waveforms

The following building blocks will be required to design an optimal pre-emphasis pulse generator based on the above theory: (a) a voltage generator for generating DC voltages such as V_{ref} and αE, (b) a detector for detecting that the voltage at the far end has reached V_{ref} and (c) a switch for stopping overdrive when the detector detects V_{ref}. A block diagram of Fig. 3 meets the above requirement. The comparator monitors the far-end voltage to control the pre-emphasis pulse width without an additional process cost because the wiring from the comparator to the switch is realized with a metal layer outside of the array. A portion "a" of the switch turns on with *EN* low before operation. All the internal nodes of the delay line are grounded. Therefore, the comparator outputs 0. The pre-emphasis pulse is applied to the delay line with *EN* high. A portion "b" of the switch turns on. The near-end of the delay line is overdriven to αE, where E is a target voltage and α is an overdrive design parameter with >1. When the far-end of the delay line reaches V_{ref} given by (4), the comparator outputs 1 to determine the pre-emphasis pulse width. A portion "c" of the switch turns on. As a result, the delay time of the slowest nodes at $x = l/3$ and $x = l$ [4] can be minimal independently of r and c values, as shown in (4). Thus, the proposed circuit is insensitive to the process and temperature variation, even when the resistance varies as temperature. Fig. 4 proposes a circuit configuration in a large memory chip. In [5], one WL decoder shares an 8 sub-arrays. WL driver is connected to all array selection transistors. In the proposed memory die,

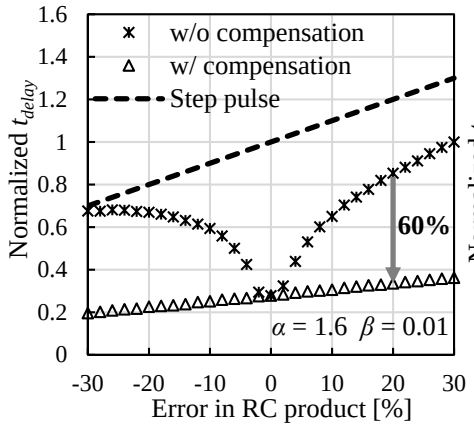

Fig. 7. Impact of errors in RC

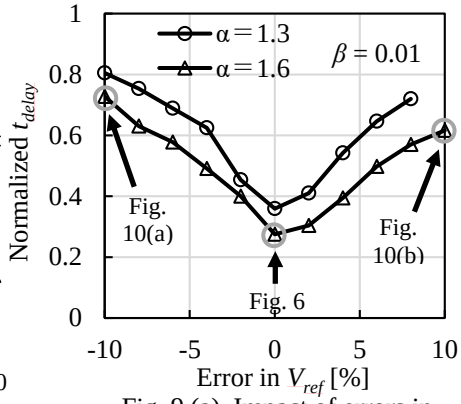

Fig. 9 (a). Impact of errors in V_{ref} on t_{delay} (β = 0.01)

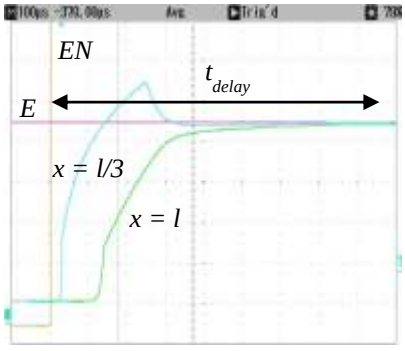

Fig. 10(a). Measured waveforms (-10%)

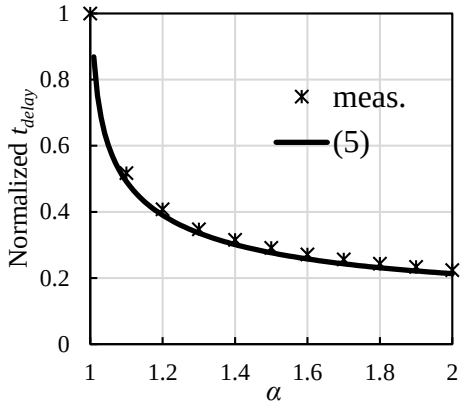

Fig. 8. α-t_{delay} (β = 0.01)

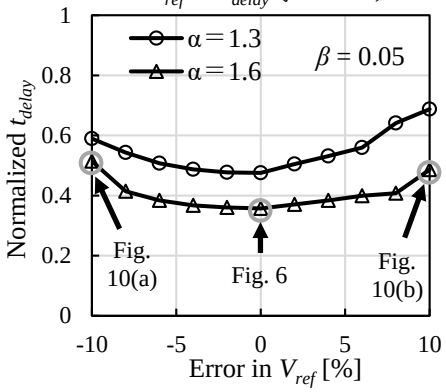

Fig. 9 (b). Impact of errors in V_{ref} on t_{delay} (β = 0.05)

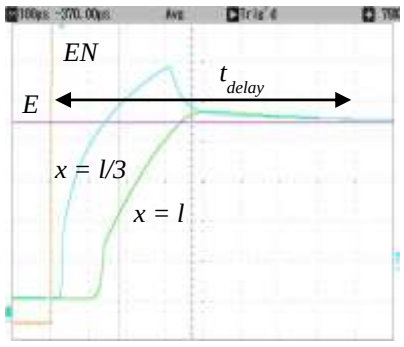

Fig. 10(b). Measured waveforms (+10%)

additional selection transistors are placed at the far-end of the sub-array "Ary8". When one of the additional select transistors is selected, the far-end of the WL is connected with the comparator. For example, when WL Dec 1 is selected, the select transistors of sub-arrays 1 to 8 of Sel 1 turn on. The voltage at the far end of "Ary8" is monitored and the WL driver outputs the optimal waveform for all the sub-arrays 1-8. Note that it is assumed that RC variation within a die can be neglected as done in [3]. With this configuration, overhead in area and power can be minimal.

IV. Measured Results

The test circuit was fabricated together with an RC line in 0.18 μm 3V CMOS, as shown in Fig. 5. The total area of the comparator, the logic and the switch circuit is 0.002 mm^2. Total capacitance and resistance of the RC line are 5.1MΩ and 130pF, respectively. The delay time was measured for each of various V_{ref} and α. Fig. 6 shows measured waveforms at $x = l/3$ and $x = l$. Note that a voltage below 0.7V is distorted due to the threshold of the monitoring buffers, which does not affect the pre-emphasis pulse operation itself. It was confirmed that the slowest two nodes at $x = l/3$ and $x = l$ had the same delay time with V_{ref} given by (4). Fig. 7 shows simulation results for delay time vs error in RC product, which is normalized by t_{delay} with α = 1 in case of a step pulse. The delay time has a significant dependence on RC variation when the pre-emphasis pulse width is not compensated against the process variation, as shown by "w/o compensation". On the other hand, the delay time can become less significant over the process variation when the proposed circuit is applied, as shown by "w/ compensation". This is because the proposed circuit self-consistently controls the pre-emphasis pulse width without calibration regardless of the RC time constant. As a result, even when the RC product varies by +20%, the delay time can be reduced by 60% with the proposed circuit in comparison with a fixed pre-emphasis pulse width when α = 1.6 and β = 0.01. Fig. 8 shows t_{delay} as a function of α for β = 0.01. Equation (5) is the theoretical value of the minimum delay time [4].

$$t_{delay\_min} \approx \frac{\tau}{9} \ln \frac{4\alpha}{3\pi\beta} \left(\frac{\alpha}{\alpha - 1} \right)^8 \quad (5)$$

Measured results are in good agreement with (5) within an error of 6% at most for β = 0.01 and $1.1 \le \alpha \le 2.0$. With α = 1.5, the delay time can be reduced by 70%. Figs. 9 show t_{delay} as a function of V_{ref} for β = 0.01 (a) and β = 0.05 (b). Figs. 10 show measured waveforms when $\alpha = 1.6$ and the errors in V_{ref} are respectively −10% (a) and +10% (b). One can notice that the smaller the β, the greater the influence of an error in V_{ref} on the delay time. V_{ref} needs to be controlled accurately because the delay time changes due to the error of V_{ref}. For example, if it is desired to reduce the delay time by 50% under the conditions of α = 1.6 and β = 0.01, V_{ref} must be controlled to be within ±5%. Equation (4) was validated only with no comparator offset. Because the delay time is very sensitive to V_{ref}, the comparator needs sufficiently small input offset.

Table I summarizes the comparison of the test cost and the area overhead between this work, [2] and [3]. References [2] and [3] require test operation to calibrate the pre-emphasis pulse against process variation, whereas the proposed circuit does not. The circuit controls the pre-emphasis pulse width to be optimal to realize the minimal delay time. The temperature variation is not compensated in [2] and [3], but is automatically compensated by the proposed circuit. The overhead of the circuit area was estimated. In [3], 2 of 2732 blocks are added as for a monitor circuit whose area overhead is estimated to be 0.06%. The area of the proposed die is 0.002 mm^2. If the proposed circuit is implemented in the circuit of [3], the area overhead is estimated to be 0.003%.

TABLE I. Comparison of test cost and area overhead

	Calibration against process variation	Calibration against temperature variation	Area overhead
[2]	Calibrating α prior to user operation	N.A.	N.A.
[3]	Calibrating α and T_{pre} in die test	N.A.	0.06%
This work	No calibration required. T_{pre} is controlled to make t_{delay} minimal		0.003%

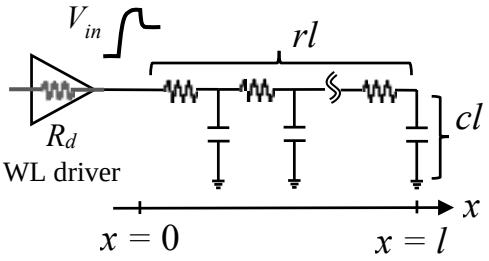

Fig. 11. Equivalent circuit with R_d

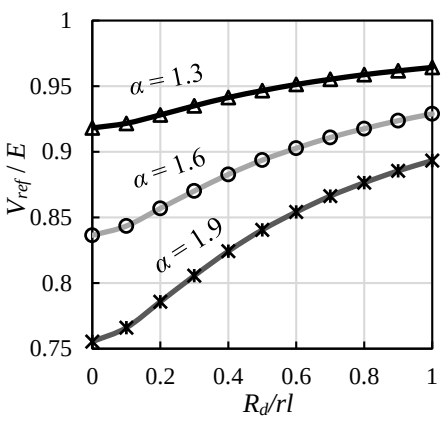

Fig. 12. Optimal vs. R_d/rl

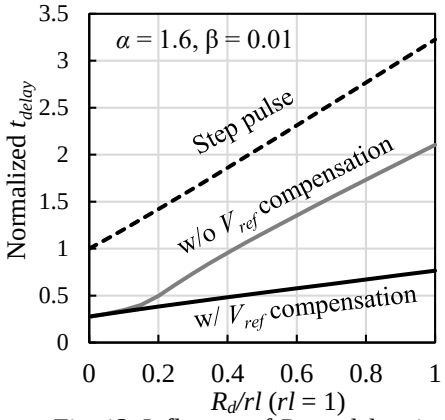

Fig. 13. Influence of R_d on delay time

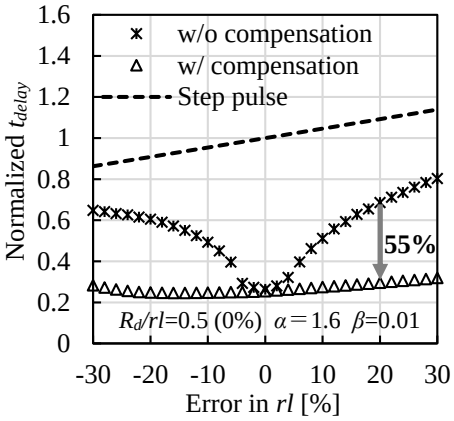

Fig. 14. Impact of errors in RC product on t_{delay}

V. Impact of the Resistance of Driver and Switch on the Detection Level

In this section, the impact of the resistance of driver and switch on the delay time is discussed. When the driver has a large output resistance (R_d), the input signal can be distorted, as shown in Fig. 11. In section II, it is shown that V_{ref} is made constant regardless of the delay line parasitic resistance rl and the delay line parasitic capacitance cl. However, when R_d is considered in design, the delay time should be affected by the ratio of R_d to rl. Fig. 12 shows the optimum value of V_{ref} as a function of the resistance ratio R_d/rl, which is determined by SPICE simulation. As the resistance of the driver increases, the optimum value of V_{ref} also needs to be increased. Fig. 13 compares the case where the value of V_{ref} is compensated according to Fig. 12 with the case where that is fixed by (4). The values are normalized by t_{delay} with Rd = 0 and α = 1 in case of a step pulse. Without V_{ref} compensation, the effectiveness of the pre-emphasis pulsing decreases as R_d/rl increases. On the other hand, with V_{ref} compensation, the delay time can be significantly reduced regardless of R_d/rl. Therefore, the proposed circuit can operate effectively by compensating V_{ref} even if R_d is as high as rl. However, when rl varies due to process variation, an initially determined V_{ref} could differ from the optimal value. To investigate the impact of the variation in rl on the delay time, the compensation effect of the proposed circuit was simulated, as shown in Fig. 14. Even with a large resistance of R_d/rl = 0.5, the compensation of V_{ref} given by Fig. 12 significantly reduces the effect of the variation in rl on the delay time. Even when rl varies by +20%, the delay time can be reduced by 55% with the proposed circuit in comparison with a fixed pre-emphasis pulse width when α = 1.6 and β = 0.01. As a result, the proposed circuit is still effective even when the resistance of the driver and switch is as high as that of the delay line.

VI. Conclusion

The proposed pre-emphasis generator optimally controls the pulse width without any calibration process both in die test and field. The theoretical optimum reference voltage given by (4) was validated by measurement. Operation performance of large memory arrays and panel display can be improved with reduction in WL/CL delay by 60% at α = 1.6 under an RC variation of 20%. The formulated minimum delay time (5) was in good agreement with measurement within an error of 6%. Simulation results show that the proposed circuit is effective even when the driver and switch resistances are included.

Acknowledgment

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