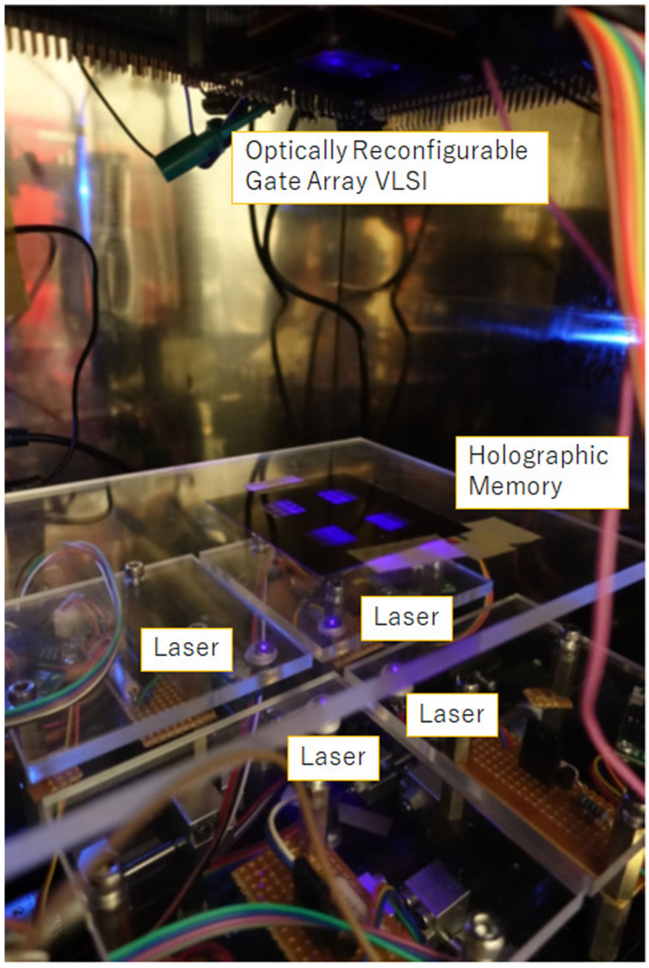
Optical Multi-Context Blind Scrubbing for Field Programmable Gate Arrays

IEEE Photonics Journal
An IEEE Photonics Society Publication

Optical Multi-Context Blind Scrubbing for Field Programmable Gate Arrays

Volume 12, Number 6, December 2020

Yusuke Takaki
Minoru Watanabe, ***Member, IEEE***



DOI: 10.1109/JPHOT.2020.3038900

IEEE photonics SOCIETY

IEEE

Optical Multi-Context Blind Scrubbing for Field Programmable Gate Arrays

Yusuke Takaki and Minoru Watanabe, *Member, IEEE*

Graduate School of Integrated Science and Technology, Shizuoka University, 3-5-1 Johoku, Hamamatsu, Shizuoka 432-8561, Japan

DOI:10.1109/JPHOT.2020.3038900

Manuscript received July 13, 2020; revised November 6, 2020; accepted November 11, 2020. Date of publication November 20, 2020; date of current version December 8, 2020. This work was supported in part by the Initiatives for Atomic Energy Basic and Generic Strategic Research JPJA19F19209710 and in part by the Ministry of Internal Affairs and Communications of Japan under the Strategic Information and Communications R & D Promotion Programme (SCOPE). Corresponding author: Minoru Watanabe (email: watanabe.minoru@shizuoka.ac.jp.)

Abstract: This paper presents a proposal of a new optical multi-context blind scrubbing that can not only increase the soft-error tolerance of the configuration memory of field programmable gate arrays (FPGAs) but also support high-speed dynamic reconfiguration suitable for accelerating FPGA operations. The optical multi-context blind scrubbing operation uses a holographic memory as a soft-error free radiation-hardened external memory. It exploits its two-dimensional large-bandwidth optical bus. Optical multi-context blind scrubbing operation was demonstrated with four configuration contexts. The soft-error tolerance of the scrubbing operation was evaluated using a radiation tolerance experiment using two 4-MBq Americium-241 alpha particle sources. Results show the worst case mean time to repair (MTTR) of the scrubbing operation as 560 ns, which can realize sufficient soft-error tolerance in radiation-rich space environments.

Index Terms: Field programmable gate array, holography, optical scrubbing, optoelectronic device.

1. Introduction

Recently, field programmable gate arrays (FPGAs) are used frequently for space embedded systems because of their reconfigurability [1]–[3]. Nevertheless, two difficulties persist for space embedded systems using an FPGA compared with those using an application specific integrated circuit (ASIC): the FPGA soft-error tolerance and performance are lower than those of ASICs.

Soft errors frequently occur on the configuration memory of FPGAs in a space radiation environment [4]–[6]. To decrease the soft-error frequency, various scrubbing methods have been proposed to refresh the configuration memory of an FPGA with a single configuration context [7]–[11]. A faster scrubbing operation can increase the soft-error tolerance.

With blind scrubbing methods for FPGAs, all data of the configuration memory are cyclically refreshed with a single configuration context on an external flash memory with no error detection mechanism. Although the flash memories are not perfectly robust for high-energy charged particles in terms of soft-error tolerance, the flash memories are more robust than static random access memories (SRAMs) against low-energy radiation [12], [13]. Blind scrubbing methods present important benefits: they have a simple architecture and simple control. Nevertheless, the mean

time to repair (MTTR) of the blind scrubbing methods is too long a period, over 100 ms. For that reason, the soft-error tolerance of such blind scrubbing methods is not good [7], [8].

An MTTR of tens of microseconds can be achieved with scrubbing operations by which a partial reconfiguration is executed based on a single configuration context on an external flash memory each time a soft error is detected using a soft-error detection mechanism [9]–[11]. However, the MTTR of conventional scrubbing methods remains inadequate to decrease the soft-error frequency under radiation-rich space environments. Unfortunately, the FPGA's serial configuration architecture cannot increase the scrubbing speed.

To improve the MTTR of scrubbing operations, an optical high-speed blind scrubbing operation exploiting a large bandwidth optical bus for configuration has been reported [14]. The optical high-speed blind scrubbing operation is executed based on a single configuration context stored on a holographic memory. The optical scrubbing operation achieved the fastest MTTR of 50 ns by exploiting a large-bandwidth optical bus. Moreover, the holographic memories are more robust against radiation than flash memories because no soft error occurs on holographic memories. Therefore, the soft-error issue of the configuration memory can be resolved completely. However, the optical blind scrubbing operation is also based on a single configuration context. No actual radiation experiment has ever been reported.

Here, for all conventional scrubbing operations, the FPGA configuration memory is assumed to be refreshed based on a single configuration context. We do not regard the single configuration context as a necessary condition for scrubbing operations. According to the latest FPGA accelerator studies, by exploiting dynamic reconfiguration, the FPGA performance can be enhanced drastically, which are called as multi-context operations [17]–[20]. In such cases, FPGAs must have two or more configuration contexts. If dynamic reconfiguration could be executed based on numerous configuration contexts with no overhead while doing a scrubbing operation, then both the performance and soft-error tolerance of FPGAs could be increased. Nevertheless, to date, no scrubbing operation exploiting numerous configuration contexts has ever been proposed. This paper therefore describes a proposal of a new multi-context scrubbing method [21] and results of a demonstration of the first Am241 alpha particle radiation tolerance experiment for an optical multi-context blind scrubbing operation.

2. Multi-Context Scrubbing

All conventional scrubbing methods were based on a single configuration context [7]–[11], [14]. Since the scrubbing operations are not useful for protecting any gate array operation on FPGAs from radiation, triple modular redundancy (TMR) has always been used to decrease the frequency of soft-errors arising on gate array operations along with the scrubbing operations [15], [16]. When a TMR is realized as hardware, the repair frequency can reach 1–100 MHz. Here, assuming the radiation incidence onto an FPGA as a low probability event, the probability follows a Poisson distribution. For triple modular redundancy (TMR), the system survival probability can be estimated as presented below.

$$P = \left(1 + \sum_{i=1}^{\infty} \left(\frac{1}{3}\right)^{i-1} \frac{\tilde{N}^i}{i!}\right) e^{-\tilde{N}} \tag{1}$$

where $\tilde{N}$ represents an average number of radiation incidents for a period T. Here, the system survival probability is defined as the probability that two or all three modules among three voting modules can work correctly inside a TMR system. When a TMR repair period T_{TMR} and scrubbing period T_{SCR} mutually differ, the respective survival probabilities P_{TMR} and P_{SCR} of a TMR operation and a scrubbing operation are estimated as shown below.

$$P_{TMR} = \left(1 + \sum_{i=1}^{\infty} \left(\frac{1}{3}\right)^{i-1} \frac{\left(\frac{T_{TMR}}{T}\tilde{N}\right)^i}{i!}\right) e^{-\left(\frac{T_{TMR}}{T}\tilde{N}\right)} \tag{2}$$

TABLE I
Mean Time Between Failures (MTBF) by Soft Errors on TMR

Scrubbing Period	100 ms	10 ms	1 ms	100 μs	10 μs	1 μs
MTBF (1 particles/s)	31.7 s	5.03 min	50.0 min	8.33 hr	83.3 hr	34.7 days

TABLE II
Mean Time Between Failures (MTBF) by Soft Errors on an FPGA When the Scrubbing Period is Fixed As 100 Ms

TMR repair period	100 ms	10 ms	1 ms	100 μs	10 μs	1 μs
MTBF	32.2 s	52.8 s	56.7 s	57.2 s	57.2 s	57.2 s

(Radiation incidence: 1 particles/s, Scrubbing period: 100 ms)

$$P_{SCR} = \left(1 + \sum_{i=1}^{\infty} \left(\frac{1}{3}\right)^{i-1} \frac{\left(\frac{T_{SCR}}{T}\tilde{N}\right)^{i}}{i!}\right) e^{-\left(\frac{T_{SCR}}{T}\tilde{N}\right)}. \tag{3}$$

The total survival probability P_{total} of a system on which a scrubbing operation and a TMR operation are executed can be estimated as

$$P_{total} = \frac{N_{gate}}{N_{gate} + N_{conf}} (P_{TMR})^{\frac{T}{T_{TMR}}} + \frac{N_{conf}}{N_{gate} + N_{conf}} (P_{SCR})^{\frac{T}{T_{SCR}}}, \tag{4}$$

where N_{gate} and N_{conf} respectively denote the number of transistors in the pure gate array and the configuration circuit on the FPGA that the system uses. The mean time between failures (MTBF) by soft errors of the total system is estimated as shown below.

$$MTBF = \frac{T}{1 - P_{total}}. \tag{5}$$

Results of the theoretical analysis of MTBF of an FPGA system for which the scrubbing period is the same as the repair period of a TMR operation are shown in Table I. If both periods could be decreased, then the MTBF by soft errors of the FPGA system could be improved. According to an our originally designed FPGA with 340,000 gates, the numbers of transistors of the pure gate array and the configuration circuit on the FPGA are, respectively, 23,406,626 and 30,062,592. When the scrubbing period is fixed to 100 ms and the TMR repair period is varied for the originally designed FPGA, the MTBF of P_{total} is evaluated as shown in Table II. Even if the TMR repair period is decreased, the MTBF cannot be improved when the scrubbing period is fixed to 100 ms. Therefore, high-speed scrubbing operations must be used to decrease the soft errors. Optical high-speed scrubbing [14] is useful for that purpose.

Fundamentally, scrubbing operations can be regarded as a reconfiguration operation. However, we regard the reconfiguration of the scrubbing operations as waste of resources because the reconfiguration is not useful except for soft-error mitigation. If the reconfiguration could be used for dynamic reconfiguration or function change, then the performance and the number of functions on FPGAs could be increased. This paper therefore presents a proposal of a new multi-context scrubbing operation. This scrubbing operation is executed using multiple contexts. Reconfiguration for the scrubbing operation is shared with dynamic reconfiguration for increasing the FPGA performance. If the configuration for a scrubbing operation could also be used for a function change of a programmable gate array, then a dynamic function change on a programmable gate array could be executed while executing a scrubbing operation. An example of multi-context scrubbing is presented in Fig. 1. In the Fig. 1, four configuration contexts are implemented cyclically onto a programmable gate array as a scrubbing operation and a dynamic function change of the programmable gate array. Although the soft-error tolerance of the multi-context scrubbing operations

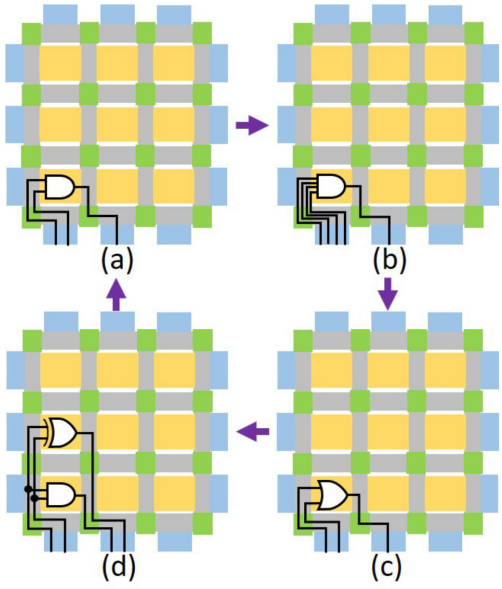


Fig. 1. An example of a multi-context scrubbing operation including four configuration contexts. The four circuits of panels (a), (b), (c), and (d) are implemented onto a programmable gate array by rotation as a scrubbing operation.

is equal to that of conventional single-context scrubbing operations, increased performance of a programmable gate array can be anticipated.

This paper demonstrates an optical high-speed multi-context blind scrubbing, which can simultaneously execute a high-speed dynamic function change of a programmable gate array during a high-speed scrubbing operation.

3. Optically Reconfigurable Gate Array (ORGA) Architecture

3.1 Optical Components

To demonstrate the proposed optical high-speed multi-context blind scrubbing, an ORGA system with four configuration contexts was constructed as depicted in Fig. 2. In earlier studies, ORGAs with a holographic memory including 4–9 configuration contexts have been demonstrated [22], [23]. Although the newly developed ORGA system was developed based on earlier work [22], [23], the ORGA system was modified for use under a vacuum condition for an Am241 radiation experiment. The ORGA consists of four semiconductor lasers (L462P1400 MM; Thorlabs Inc.), a holographic memory film (silver-halide photomask; Unno Giken Co. Ltd.) including four recording regions corresponding to four configuration contexts, and an ORGA very large scale integration (VLSI). The three components were constructed using a plastic plate framework. Since the ORGA system is used under a vacuum condition, eight servo motors were added to adjust the positions of four lasers and two servo motors were added for adjusting the position of the ORGA-VLSI. With this architecture, a blind scrubbing operation can be executed at any time based on a valid configuration context inside a holographic memory because soft errors never occur on holographic memories. Therefore, the soft-error tolerance of ORGAs becomes higher than conventional that of EEPROM-based FPGA scrubbing operations. Moreover, the ORGA's faster scrubbing can enhance the soft-error tolerance.

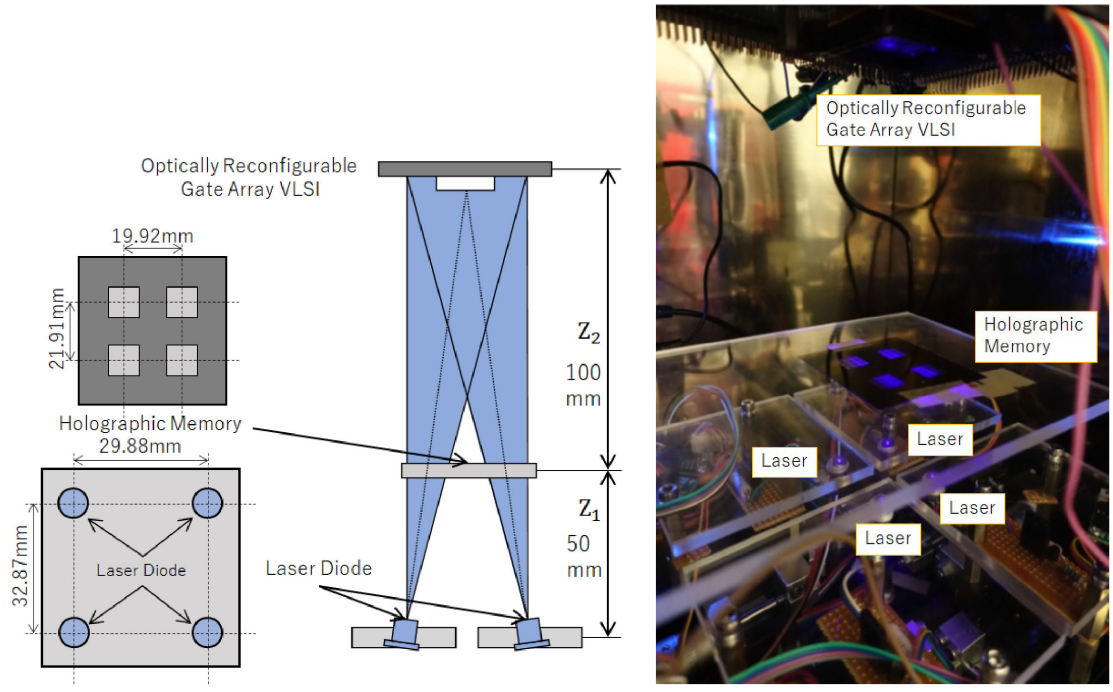


Fig. 2. Block diagram and photograph of a constructed ORGA system consisting of four semiconductor lasers, a holographic memory film including four recording regions corresponding to four configuration contexts, and an ORGA-VLSI.

3.2 Orga-Vlsi

An ORGA-VLSI was fabricated using a 0.18 μm standard complementary metal-oxide semiconductor (CMOS) process technology. The die is 5 mm $\times$ 5 mm. Block diagrams of an optically reconfigurable logic block, an optically reconfigurable I/O block, and an optically reconfigurable switching matrix are portrayed respectively in Figs. 3(a), 3(b), and 3(c). The ORGA-VLSI has a fine-grained programmable gate array consisting of 128 logic blocks, 144 switching matrices, and 64 input–output (I/O) bits. The functionality of the ORGA-VLSI, aside from configuration mechanism, is fundamentally identical to that of typical FPGAs. However, the ORGA-VLSI has a photodiode array for detecting optically applied configuration contexts. Each logic block consists of two 4-input look-up tables used for implementing Boolean functions and two delay-type flip-flops with a reset function. Each switching matrix consists of four selectors. An optically reconfigurable logic block can be reconfigured perfectly in parallel using 60 photodiodes. An optically reconfigurable switching matrix can be controlled perfectly in parallel using 64 photodiodes. The number of programming elements or photodiodes of all logic blocks, switching matrices, and I/O blocks is 17,664. The programmable gate array can be reconfigured optically and perfectly in parallel. The photodiodes were constructed using junctions between the P-substrate and N-wells. Each junction area is 4.40 $\times$ 4.45 μm. Horizontal and vertical intervals are, respectively, 30.08 μm and 30.24 μm. The total chip gate count is 8,704.

3.3 Holographic Memory

The ORGA was designed to have four optical two-dimensional binary configuration context patterns generated from a holographic memory film. Four holographic memory patterns H_1, H_2, H_3, and H_4 were calculated using a personal computer as shown respectively in Figs. 4(a), 4(b), 4(c), and

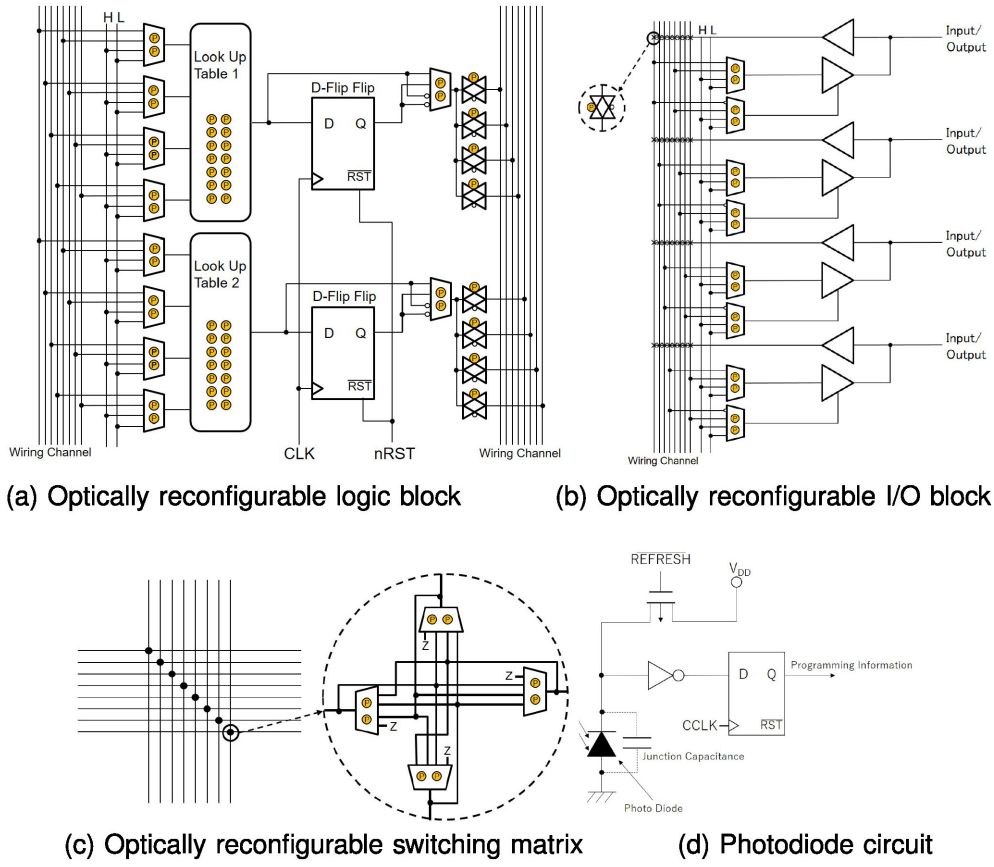


Fig. 3. Block diagrams of (a) an optically reconfigurable logic block, (b) an optically reconfigurable I/O block, (c) an optically reconfigurable switching matrix, and (d) a photodiode circuit.

4(d). They are recorded onto four recording regions of a holographic memory film as shown in Fig. 5 using the following theory. The four holographic memory regions are addressed by four semiconductor lasers. Each semiconductor laser beam can be considered as diffused light with no collimator. Spectral line width $\Delta\nu$ and the related coherent length of semiconductor lasers (L462P1400 MM; Thorlabs Inc.) are about 730 GHz and 0.41 mm, respectively. To satisfy the coherent length, only a 1.6 mm $\times$ 1.6 mm gate array region of the ORGA-VLSI was used for this experiment when about 70 % of each fringe pattern is effective. When using the full gate array region of the ORGA-VLSI, the lasers (L462P1400 MM; Thorlabs Inc.) must be replaced with lasers that have a smaller spectral line width of 312 GHz. After a binary configuration context is generated through logic synthesis, place, and route operations, the binary configuration context is converted to the corresponding optical two-dimensional binary configuration context pattern O(x, y) depending on the location of photodiodes of logic blocks, switching matrices, I/O blocks. Here, binary state highs and binary state lows on an optical two-dimensional binary configuration context pattern are represented respectively as bright points and a dark area. A holographic memory pattern that can generate such an optical configuration context pattern is calculable as

$$H(\alpha,\beta) = B\exp\left(-j\frac{2\pi}{\lambda}\sqrt{Z_1^2+(\alpha-u)^2+(\beta-v)^2}\right) + \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} O(x,y)\exp\left(j\frac{2\pi}{\lambda}\sqrt{Z_2^2+(\alpha-x)^2+(\beta-y)^2}\right)dxdy, \quad (6)$$

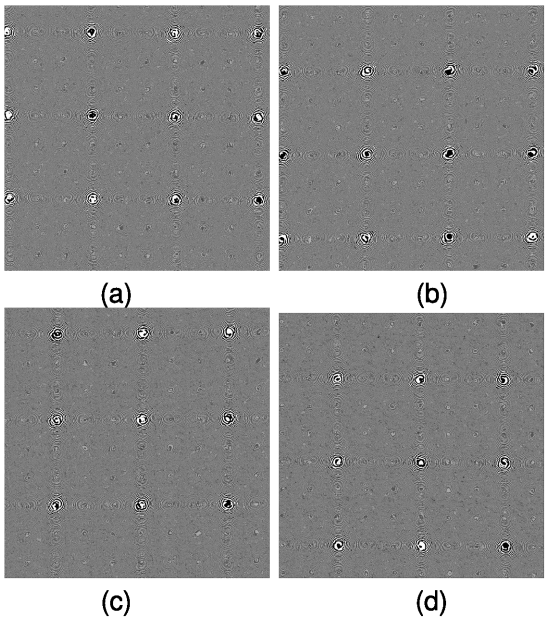


Fig. 4. Binary holographic memory patterns consisting of 2,000 × 2,000 pixels. The size of each region is 10 mm × 10 mm. Panels (a), (b), (c), and (d) respectively depict a 2-bit AND circuit, a 4-bit AND circuit, a 2-bit OR circuit, and a half-adder circuit.

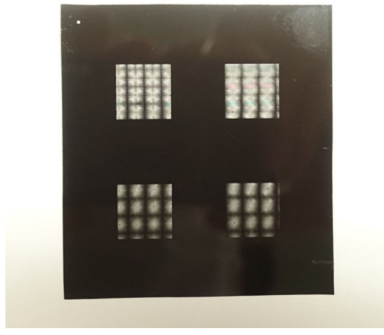


Fig. 5. Recorded silver-halide holographic memory film including the 2-bit AND circuit, the 4-bit AND circuit, the 2-bit OR circuit, and the half-adder circuit.

where λ denotes the wavelength of four lasers, α and β are the coordinates of a holographic memory region, u and v are the coordinates of a laser addressing the corresponding holographic memory region, Z_1 represents the distance between the holographic memory regions and the lasers, x and y are the coordinates on an ORGA-VLSI, and B is the coefficient of the reference laser beam amplitude which means the amplitude ratio of a reference beam to an object beam. The holographic memory equation shows an interference pattern between a reference laser beam and a configuration context pattern. Assuming that the i-th bright point on an optical configuration context pattern O(x, y) can be regarded as a delta function $\delta(x_i, y_i)$, then if the system satisfies the Fresnel region, Eq. 6 can be rewritten as

$$H(\alpha,\beta) = B\exp\left(-j\frac{2\pi}{\lambda}Z_1\right)\exp\left(-j\frac{\pi}{\lambda Z_1}\left\{(\alpha-u)^2+(\beta-v)^2\right\}\right) + \exp\left(j\frac{2\pi}{\lambda}Z_2\right)\sum_{i=1}^{B_N}\exp\left(j\frac{\pi}{\lambda Z_2}\left\{(\alpha-x_i)^2+(\beta-y_i)^2\right\}\right) \quad (7)$$

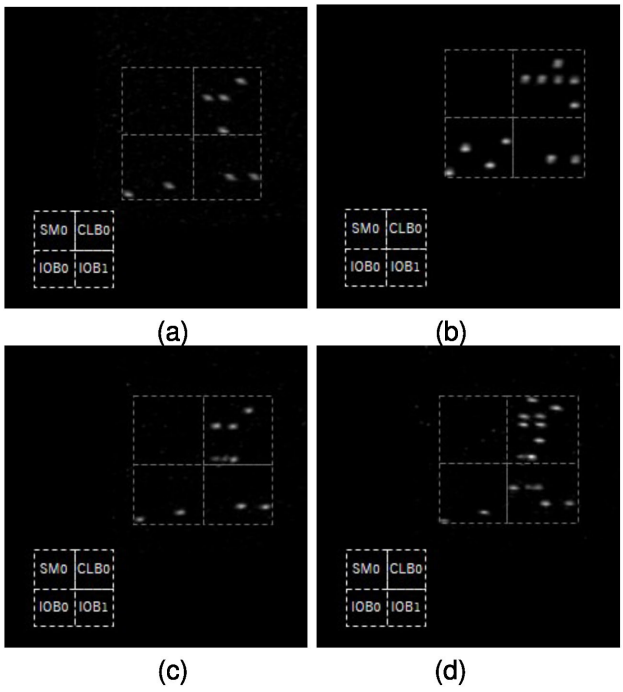


Fig. 6. CCD-captured diffraction patterns of the 2-bit AND circuit, the 4-bit AND circuit, the 2-bit OR circuit, and the half-adder circuit.

where B_N represents the number of bright bits included in a configuration context. The fringe pattern of a holographic memory is calculable as the product of H and the complex conjugate H^* of H. Finally, by removing the constant value included in HH^*, the fringe pattern is calculated as

$$H(\alpha,\beta)H^*(\alpha,\beta) \propto \sum_{i=1}^{B_N} \cos\left(\frac{\pi}{\lambda Z_1}\left\{(\alpha-u)^2+(\beta-v)^2\right\}+\frac{\pi}{\lambda Z_2}\left\{(\alpha-x_i)^2+(\beta-y_i)^2\right\}\right). \quad (8)$$

Defining the minimum intensity and the maximum intensity of $H(\alpha,\beta)H^*(\alpha,\beta)$ inside a holographic memory region as H_{min}, H_{max}, respectively, the equation above can be normalized as

$$H'(\alpha,\beta) = \frac{H(\alpha,\beta)H^*(\alpha,\beta) - H_{min}}{H_{max} - H_{min}} \quad . \quad (9)$$

Finally, four holographic memory patterns were calculated using the formulations as shown in Figs. 4 and 5.

3.4 Experiment System

In the ORGA system, Z_1 and Z_2 were defined respectively as 50 mm and 100 mm, as shown in Fig. 2. The coordinates (u_m, v_m) of four semiconductor lasers are, respectively, (14.94 mm, 16.435 mm), (-14.94 mm, 16.435 mm), (14.94 mm, -16.435 mm), and (-14.94 mm, -16.435 mm). The wavelength and power of the four semiconductor lasers are, respectively, 462 nm and 1400 mW. Although the current laser power is exactly high and must be increased as increasing the size of the programmable gate array, it is caused by the low diffraction efficiency of the current two-dimensional holographic memory. The diffraction efficiency of the current two-dimensional holographic memory is about 0.05 %. In the future, the introduction of a volume holographic memory with a diffraction efficiency of 70-95 % would drastically improve the laser power issue [24]. Figure 4 portrays four binary fringe patterns consisting of 2,000 $\times$ 2,000 pixels. Since the pixel size

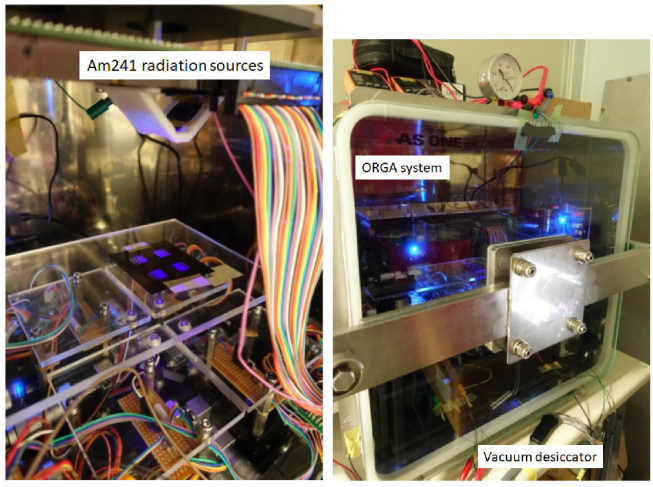


Fig. 7. Photographs of the ORGA system on which a radiation source mount was set and of a vacuum desiccator including the ORGA system.

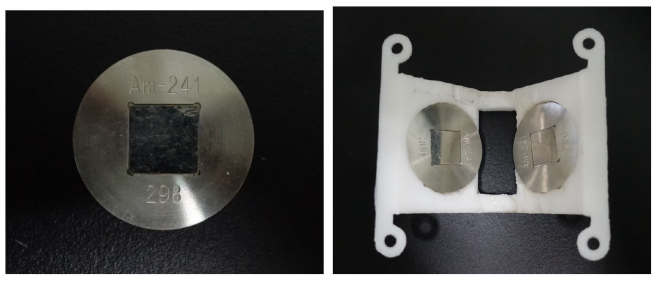


Fig. 8. Photographs of a 4 MBq AM241 radiation source and of a mount with two AM241 radiation sources.

is 5 μm, the holographic memory size is 10 mm $\times$ 10 mm. The horizontal and vertical distances between the centers of holographic memories are 19.92 mm and 21.91 mm, respectively. In this experiment, a 2-bit AND circuit, a 4-bit AND circuit, a 2-bit OR circuit, and a half-adder circuit were recorded to four recording regions of a silver-halide holographic memory film. The CCD-captured configuration context patterns generated from the four holographic memory regions are portrayed respectively in Figs. 6(a), 6(b), 6(c), and 6(d).

4. Radiation Experiment

Using the previously described ORGA system, optical multi-context blind scrubbing using a 2-bit AND circuit, a 4-bit AND circuit, a 2-bit OR circuit, and a half-adder circuit has been demonstrated under radiation conditions. Two 4 MBq Am241 americium radiation sources, which emit alpha particles, were used to produce the radiation conditions. Photographs of an Am241 radiation source and its mount including two Am241 radiation sources are presented in Fig. 8. Since the mount is set on the top of the ORGA-VLSI, the center of the mount has a hole to apply the optical configuration contexts. An optical configuration context passes through the hole. It eventually reaches the top of the ORGA-VLSI. Finally, to prevent alpha particle decay, the ORGA system is inserted to a vacuum desiccator as shown in Fig. 7. The atmospheric pressure inside the vacuum desiccator was decreased to 6 kPa. Under those conditions, the MTTR of the ORGA system was measured. Firstly, optical multi-context blind scrubbing was executed cyclically and the maximum period of the

optical multi-context blind scrubbing was set to 560 ns. Each time a soft-error happens, it has been confirmed whether the soft-error effect could be removed or not at the next cycle of the optical multi-context blind scrubbing. As a result, all soft-error effects could be removed correctly at the next cycle of the optical multi-context blind scrubbing. Results show that the worst-case MTTR was measured as 560 ns. The MTTR is sufficiently faster than that of scrubbing operations on FPGAs. For this radiation experiment, the scrubbing controller was implemented onto an external FPGA. It was never exposed to alpha particles. However, in future modifications, the scrubbing controller is expected to be implemented inside the ORGA-VLSI.

5. Conclusion

This paper has presented a proposal for optical high-speed multi-context scrubbing that can not only increase the soft-error tolerance of configuration memory on programmable gate arrays but also support high-speed dynamic reconfiguration suitable for accelerating operations on the programmable gate arrays. The optical high-speed multi-context blind scrubbing operation has been demonstrated experimentally on an ORGA. The soft-error tolerance, or MTTR, was evaluated as sufficiently higher than that of current FPGAs using a radiation experiment conducted with two 4-MBq Am241 alpha particle sources. The current system uses plastic plates to fix the positions of lasers, a holographic memory film, and an ORGA-VLSI. However, in the future, a reflection-type volume holographic memory and Vertical Cavity Surface Emitting LASERs (VCSELs) will be introduced and the VCSELs will be implemented on the same side as the ORGA-VLSI so that the system height will be decreased to 1-2 cm. Finally, the holographic memory, the VCSEL, and the ORGA-VLSI will be molded as a single package. At that time, thermal effect and vibration tolerance could be neglected. Also, VCSEL technology would increase the number of configuration contexts.

Acknowledgment

The VLSI chip in this study was fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Rohm Co. Ltd. and Toppan Printing Co. Ltd.

References

[1] T. Li, H. Liu, and H. Yang, "Design and characterization of SEU hardened circuits for SRAM-Based FPGA," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 27, no. 6, pp. 1276–1283, Jun. 2019.
[2] L. Santos, L. Berrojo, J. Moreno, J. F. Lopez, and R. Sarmiento, "Multispectral and hyperspectral lossless compressor for space applications (HyLoC): A low-complexity FPGA implementation of the CCSDS 123 standard," *IEEE J. Sel. Topics Appl. Earth Observ. Remote Sens.*, vol. 9, no. 2, pp. 757–770, Feb. 2016.
[3] X. Cai, M. Zhou, T. Xia, W. H. Fong, W. T. Lee, and X. Huang, "Low-power SDR design on an FPGA for intersatellite communications," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 11, pp. 2419–2430, Nov. 2018.
[4] S. Liu *et al.*, "Comparison of the susceptibility to soft errors of SRAM-Based FPGA error correction codes implementations," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 3, pp. 619–624, Jun. 2012.
[5] B. Du and L. Sterpone, "Online monitoring soft errors in reconfigurable FPGA during radiation test," in *Proc. IEEE Int. Instrum. Meas. Technol. Conf.*, 2017, pp. 1–5.
[6] A. Ramos, R. G. Toral, P. Reviriego, and J. A. Maestro, "An ALU protection methodology for soft processors on SRAM-based FPGAs," *IEEE Trans. Comput.*, vol. 68, no. 9, pp. 1404–1410, Sep. 2019.
[7] J. Heiner, B. Sellers, M. Wirthlin, and J. Kalb, "FPGA partial reconfiguration via configuration scrubbing," in *Proc. Int. Conf. Field Programmable Log. Appl.*, 2009, pp. 99–104.
[8] M. Kumar, D. Digdarsini, N. Misra, and T. V. S. Ram, "SEU mitigation of Rad-Tolerant Xilinx FPGA using external scrubbing for geostationary mission," in *Proc. Int. Conf. Signal Process. Integr. Netw.*, 2017, pp. 414–418.
[9] M. S. Reorda, L. Sterpone, and A. Ullah, "An error-detection and self-repairing method for dynamically and partially reconfigurable systems," in *Proc. IEEE Eur. Test Symp.*, 2013, pp. 1–7.
[10] A. Stoddard, A. Gruwell, P. Zabriskie, and M. J. Wirthlin, "A hybrid approach to FPGA configuration scrubbing," *IEEE Trans. Nucl. Sci.*, vol. 64, no. 1, pp. 497–503, Jan. 2017.
[11] M. Mousavi, H. R. Pourshaghaghi, H. Corporaal, and A. Kumar, "Scatter scrubbing: A method to reduce SEU repair time in FPGA configuration memory," in *Proc. IEEE Int. Symp. Defect Fault Tolerance VLSI Nanotechnol. Syst. (DFT)*, 2019, pp. 1–6.

[12] D. N. Nguyen, S. M. Guertin, and J. D. Patterson, "Radiation tests on 2Gb NAND flash memories," in *Proc. IEEE Radiat. Effects Data Workshop*, 2006, pp. 121–125.
[13] N. Gupta, B. Vermeire, H. Barnaby, M. Goksel, E. Li, and D. Czajkowski, "Design of a 1 Gb radiation hardened NAND flash memory," in *Proc. Non-Volatile Memory Technol. Symp.*, 2007, pp. 10–14.
[14] T. Fujimori and M. Watanabe, "High-speed scrubbing demonstration using an optically reconfigurable gate array," *Opt. Exp.*, vol. 25, no. 7, pp. 7807–7817, 2017.
[15] L. A. C. Benites *et al.*, "Reliability calculation with respect to functional failures induced by radiation in TMR Arm Cortex-M0 soft-core embedded into SRAM-Based FPGA," *IEEE Trans. Nucl. Sci.*, vol. 66, no. 7, pp. 1433–1440, Jul. 2019.
[16] J. A. Abraham and D. P. Siewiorek, "An algorithm for the accurate reliability evaluation of triple modular redundancy networks," *IEEE Trans. Comput.*, vol. C-23, no. 7, pp. 682–692, Jul. 1974.
[17] X. Zhao, A. T. Erdogan, and T. Arslan, "High-efficiency customized coarse-grained dynamically reconfigurable architecture for JPEG2000," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 21, no. 12, pp. 2343–2348, Dec. 2013.
[18] T. Kojima and H. Amano, "A configuration data multicasting method for coarse-grained reconfigurable architectures," in *Proc. Int. Conf. Field Programmable Log. Appl.*, 2018, pp. 239–242.
[19] H. Shinba and M. Watanabe, "Radiation-hardened configuration-context realization for field programmable gate arrays," *Appl. Opt.*, vol. 59, no. 19, pp. 5680–5686, 2020.
[20] T. Fujimori and M. Watanabe, "Optically reconfigurable gate array using a colored configuration," *Appl. Opt.*, vol. 57, no. 29, pp. 8625–8631, 2018.
[21] T. Fujimori and M. Watanabe, "Multi-context scrubbing method," in *Proc. IEEE Int. Midwest Symp. Circuits Syst.*, 2017, pp. 1548–1551.
[22] M. Nakajima and M. Watanabe, "Fast optical reconfiguration of a nine-context DORGA using a speed adjustment control," *ACM Trans. Reconfigurable Technol. Syst.*, vol. 4, no. 2, pp. 15:1–15:21, 2011.
[23] S. Kubota and M. Watanabe, "A four-context programmable optically reconfigurable gate array with a reflective silver-halide holographic memory," *IEEE Photon. J.*, vol. 3, no. 4, Aug. 2011.
[24] A. Tork, P. Pilot, and T. V. Galstian, "New photopolymer materials for holographic data storage," in *Proc. Opt. Data Storage Conf. Dig.*, 2000, pp. 138–140.