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Dynamic Single-Electron Transistor Modeling for High-Frequency Capacitance Characterization

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Abstract: Based on the time-dependent master equation and taking the dynamic gate current into account, a new single-electron transistor (SET) model is proposed, which can represent intrinsic terminal capacitances and transcapacitances. By using this model, bias, frequency and temperature dependences of these capacitances are evaluated. Since the model is implemented in the SPICE circuit simulator, it can be used to analyze the high-frequency behavior of circuits, including SETs and is applied to the characterization of a SET-based inverting amplifier this time.

Keywords: single-electron transistor model; time-dependent master equation; input capacitance; transcapacitance; SPICE circuit simulator

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1. Introduction

Thanks to the advances in nanofabrication technology, it is possible to make single-electron transistors (SETs) small enough to realize room-temperature operation [1–3]. As a result, the values of source, drain and gate capacitances can be in the order of attofarad, which leads to subpicosecond intrinsic time constant even though the tunnel junction resistance is lower bounded by the resistance quantum, h/e^2 about 25.8 kΩ. Such a possibility of high-speed or high-frequency operation of SETs has been discussed before simply based on this small intrinsic time constant [4,5], but now that the fabrication technology has advanced, it is worthwhile to analyze the high-frequency dynamic behavior of the SET in more detail.

For this purpose, an understanding of the capacitance components inside the SET is crucial. For example, the Miller effect caused by the feedback capacitance largely affects the frequency response of amplifiers [6]. Recently, charge detection for qubit readout is attempted by observing the gate input capacitance [7–10], which also requires SET models with capacitance analysis capability.

Historically, high-speed and high-frequency performance of SET-based circuits have been studied with models based on steady-state master equation [11–17], under the assumption that the external load capacitance is much larger than the internal one, but the intrinsic high-frequency response of SETs cannot be assessed by the steady-state models. Even with such a model, it is still possible to derive the capacitance components such as terminal capacitances and transcapacitances inside the SET [13], but the frequency dependence of capacitances cannot be evaluated.

Black-box models [18] and macro models [19] have similar features as long as they just provide an output current instantaneously as a function of terminal voltages.

Monte Carlo (MC) method [20–22] can simulate the dynamic or transient behavior of the intrinsic SET. Since the charges in the gate and source/drain tunnel capacitors are explicitly calculated, terminal capacitances and transcapacitances can also be derived from the simulation result. Actually, reference [23] discussed the input capacitance of SETs in conjunction with the electrometer sensitivity. However, MC method is usually

not compatible with the standard circuit simulator such as SPICE and has difficulties in analyzing frequency-dependent behavior of SET itself or circuits including SETs and other circuit elements.

SET models based on time-dependent master equations that are capable of analyzing the dynamic behavior have been developed by many researchers [11,24,25]. Since the source/drain current can be directly expressed, implementation of the models to SPICE circuit simulator [26,27] is also straightforward. Once the model is implemented to SPICE circuit simulator, it is possible to analyze the performance of SET circuits including FETs and other circuit elements. Moreover, the MC analysis capability of SPICE allows us to study the variability issue that has become serious in nanometer-scale devices including SETs [28]. However, to the best of our knowledge, there has been no model that can properly describe the terminal capacitances and transcapacitances.

Considering the above-mentioned background, we have proposed a SET model based on the time-dependent master equation, taking the gate current into account. Our model can not only analyze the high-frequency dynamic behavior of SETs, but also can represent terminal capacitances and transcapacitances. Since this model is implemented in the SPICE circuit simulator, it can be used to evaluate the high-frequency characteristics of various SET-based circuits such as amplifier, oscillator, detector, etc.

2. Method of Modeling

2.1. Proposed Model

The pictorial and symbolic schematics of the SETs are shown in Figure 1a,b, respectively. In the proposed model of Figure 1c, the gate current I_g and the drain current I_d is calculated based on the time-dependent master equation [29]. The I_g represents the contribution of the gate terminal (input) capacitance C_{gg} and gate-related transcapacitances C_{gd} and C_{gs}. The contribution of other capacitances is also included in I_d and $I_s = -(I_d + I_g)$. Although three-terminal configuration is considered at this time for simplicity, it is also possible to extend the model to four-terminal configuration [13] with the second gate (backgate), which is useful in some circuit applications [4,11] and the analysis of the background noise effect [30] that has a large impact on the SET-based circuit integrity.

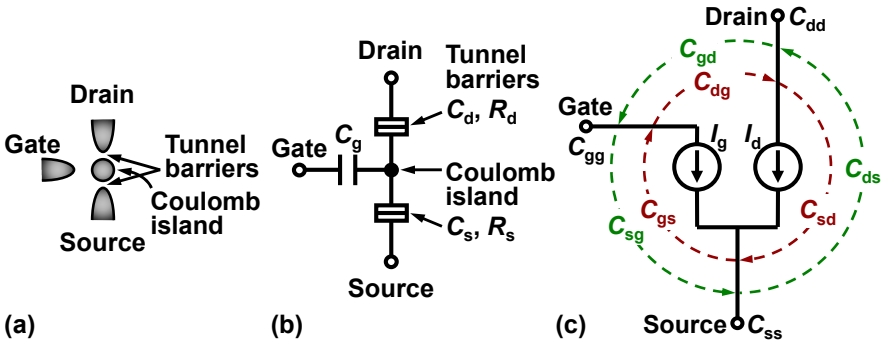


Figure 1. (**a**) SET pictorial schematic, (**b**) symbolic schematic, and (**c**) model schematic with capacitance components inside the SET.

When the master equation is solved, it is assumed that number of electrons (n) in the Coulomb island can be in four states, i.e., $n = -1$, 0, 1 or 2. The I_d is given by

$$I_d = e\sum P_n \{\Gamma_d(n-1, n) - \Gamma_d(n+1, n)\} \quad (1)$$

Here, P_n represents the probability that the number of electrons in the island is n whereas Γ_d $(n-1, n)$ and Γ_d $(n+1, n)$ are the tunneling rates of electrons from n to $n-1$ and n to $n+1$ at the drain junction, respectively.

To calculate the I_g, potential of the Coulomb island V_{isl} needs to be determined first by

$$V_{isl} = \frac{C_g V_g + C_s V_s + C_d V_d + Q_{isl}}{C_\Sigma} \tag{2}$$

Here, C_g, C_s, and C_d are the gate, source and drain capacitances, respectively, and $C_\Sigma = C_g + C_s + C_d$. Average charge Q_{isl} in the Coulomb island is given by

$$Q_{isl} = -e \sum nP_n \tag{3}$$

By substituting (3) in (2), V_{isl} can be rewritten as

$$V_{isl} = \frac{C_g V_g + C_s V_s + C_d V_d - e \sum nP_n}{C_\Sigma} \tag{4}$$

Here, V_g, V_s and V_d are gate, source and drain voltages, respectively. The I_g flowing from the gate terminal to the Coulomb island via gate capacitor can be expressed as the change in the charge Q_g in gate capacitor with respect to time.

$$\begin{aligned} I_g &= \tfrac{dQ_g}{dt} = \tfrac{d}{dt}\left(V_g - V_{isl}\right)C_g \\ &= \tfrac{d}{dt}\left\{V_g - \left(\tfrac{C_g V_g + C_d V_d + C_s V_s - e\sum nP_n}{C_\Sigma}\right)\right\}C_g \\ &= \tfrac{d}{dt}\left\{\tfrac{C_g}{C_\Sigma}\left(V_g C_\Sigma - C_g V_g - C_d V_d - C_s V_s + e\sum nP_n\right)\right\} \end{aligned} \tag{5}$$

The SPICE circuit simulator [27] is used as a solver for the simultaneous differential equation [31] of the master equation to obtain the P_n and Γ_d in (1) and (5).

In the following sections, the simulation results will be shown based on the parameters summarized in Table 1. These parameters are set rather arbitrarily to realize the cutoff frequency of 1 GHz where experimental verification is relatively easy and are also viable considering that the subattofarad capacitances have already been realized [1–3], and the tunneling resistance could be varied in a wide range by changing the insulator thickness. We also try to generalize the results by normalization, i.e., when the operation condition is described, temperature T, gate-source voltage V_{gs}, and drain-source voltage V_{ds} are normalized as $K_B T/(e^2/2C_\Sigma)$, $C_g V_{gs}/e$ and $C_\Sigma V_{ds}/e$, respectively, and enclosed in square brackets [...] if these are put down with raw values. The normalized V_{gs} ranges from 0 to 1 electron in the simulation since only n's from -1 to 2 are considered in solving the master equation. Two cases of small and moderate normalized V_{ds} of 0.01 and 0.5 are considered. The normalized temperature is set to 0.05 in most of the simulations in order not to thermally disturb the Coulomb blockade condition.

Table 1. The simulation parameters.

Gate, drain and source capacitances $C_g C_d = C_s$	1 aF
Tunneling resistances $R_d R_s = R_t$	25 MΩ
Cutoff frequency $f_c = 1/(2\pi R_\Sigma C_\Sigma)$	1 GHz
Gate—source voltage V_{gs}	0~162 mV [0~1]
Drain—source voltage V_{ds}	0.534 mV [0.01], 26.7 mV [0.5]
Temperature T	15.5 K [0.05] except for Figure 6.

Square brackets [...] indicate normalized values.

2.2. Accuracy of the Model

Since n can assume only four states, accuracy gets deteriorated if the temperature or the drain voltage becomes high. The deviation of the drain current from that of the reference MC simulator SIMON [22] is evaluated. It is found that the deviation is less than 0.5% for the normalized temperature up to 0.5 and the normalized V_{ds} up to 2.1 with various V_{gs}'s around 0.5 e/C_g (data not shown).

2.3. Extraction of Capacitance Components

As shown in Figure 1, a three-terminal SET has in total 9 terminal capacitances and transcapacitances. Since the I_g current source is newly added to the proposed model, the gate input capacitance C_{gg}, the drain-to-gate feedback capacitance C_{gd}, and source-to-gate capacitance C_{gs} can be extracted from the simulation.

The C_{gg} is evaluated by the circuit shown in Figure 2a where small sinusoidal fluctuation with amplitude ΔV_{gs} (= $e/C_g/1000$) is added to the gate bias voltage V_{gs}, and then the amplitude ΔI_g of the gate current fluctuation is measured by the simulation. The C_{gg} is calculated by

$$C_{gg} = \frac{\Delta I_g}{\omega \Delta V_{gs}} \tag{6}$$

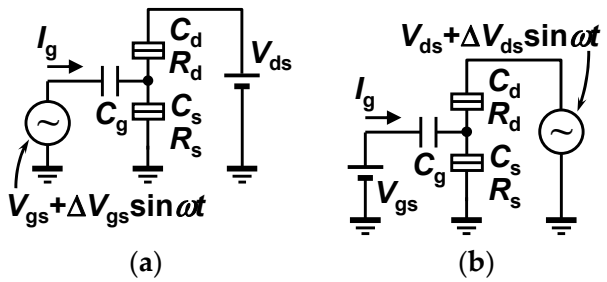


Figure 2. Circuit diagrams for the measurement of (**a**) C_{gg} and (**b**) C_{gd}.

As shown in Figure 2b, the C_{gd} is measured by adding small sinusoidal fluctuation with amplitude ΔV_{ds} (= $e/C_{\sum}/1000$) to the drain bias voltage V_{ds}, and the amplitude ΔI_g of the gate current fluctuation is observed. Similarly, the C_{gd} is obtained by

$$C_{gd} = \frac{\Delta I_g}{\omega \Delta V_{ds}} \tag{7}$$

Considering that the sum of C_{gd} and C_{gs} is equal to C_{gg} based on charge conservation of the C_{gs} is given by

$$C_{gs} = C_{gg} - C_{gd} \tag{8}$$

3. Simulation Results

3.1. Gate Bias Dependence of Capacitances

Figure 3a–c represent the C_{gg}, C_{gd}, and C_{gs}, respectively, as a function of gate voltage V_{gs} for a low drain voltage of $e/C_{\sum}/100$ at three different frequencies. The solid line shows the result of the steady-state model [13], which coincides well with the data points (square) of the proposed model at a low frequency (10 kHz).

The C_{gg} shows a sharp peak at V_{gs} = 0.5 e/C_g, where Coulomb blockade is lifted. The peak C_{gd} and C_{gs} are almost equal to each other, and are a half of the peak C_{gg}, indicating that the gate is equally coupled to the drain and source at this low drain voltage.

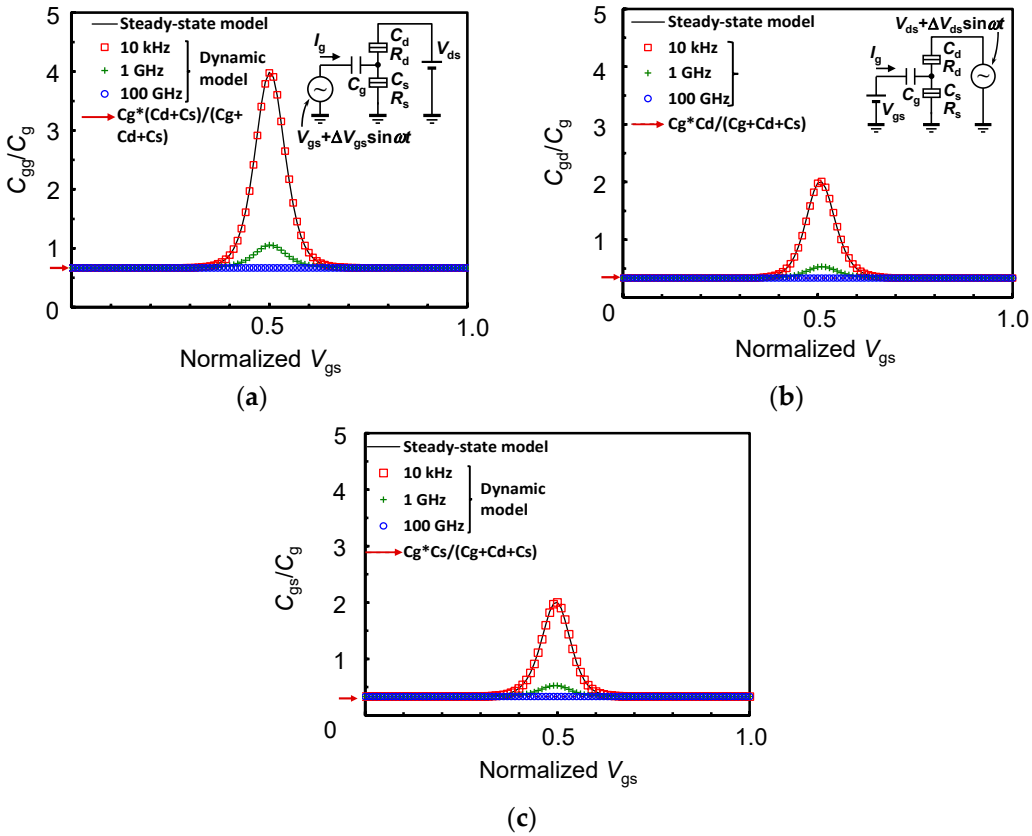


Figure 3. (**a**) SET input capacitance C_{gg} (**b**) drain-to-gate capacitance C_{gd} and (**c**) source-to-gate capacitance C_{gs} as a function of gate voltage V_{gs} for a low drain voltage V_{ds} = 0.534 mV [0.01] at T = 15.5 K [0.05].

At the cutoff frequency (1 GHz), the peak height is largely reduced, and levels off at 100 GHz due to the disappearance of the transistor action of the SET, i.e., the charge state of the Coulomb island cannot follow the rapid change of the signal. The baseline values of the C_{gg}, C_{gd}, and C_{gs} are C_g*(C_d + C_s)/C_Σ, C_g*C_d/C_Σ and C_g*C_s/C_Σ, respectively, which can be understood by considering the SET as a passive capacitance circuit consisting of C_g, C_d and C_s.

Figure 4a–c represent the C_{gg}, C_{gd}, and C_{gs}, respectively, as a function of gate voltage V_{gs} for a high drain voltage of $e/C_\Sigma/2$ at three different frequencies. The proposed model at a low frequency (square) and the steady-state model (solid line) [13] give the same result even at this large drain voltage.

The C_{gg} shows lower and wider plateau compared to the case with the low drain voltage (Figure 3a) reflecting the gentler change in the island charge with respect to V_{gs}, and wider V_{gs} area where the Coulomb blockade is lifted. In view of the behavior of the C_{gd} and C_{gs}, it is found that the gate is strongly coupled to the source at low V_{gs}'s, and to the drain at high V_{gs}'s due to the large asymmetry in applied voltages to the source and the drain.

When the frequency is increased to the cutoff frequency (1 GHz), the capacitances come close to the baselines, then level off at 100 GHz due to the loss of the transistor action. The baseline values of the capacitances are the same as those for the low drain voltage (Figure 3) and can be also explained based on the passive capacitance circuit.

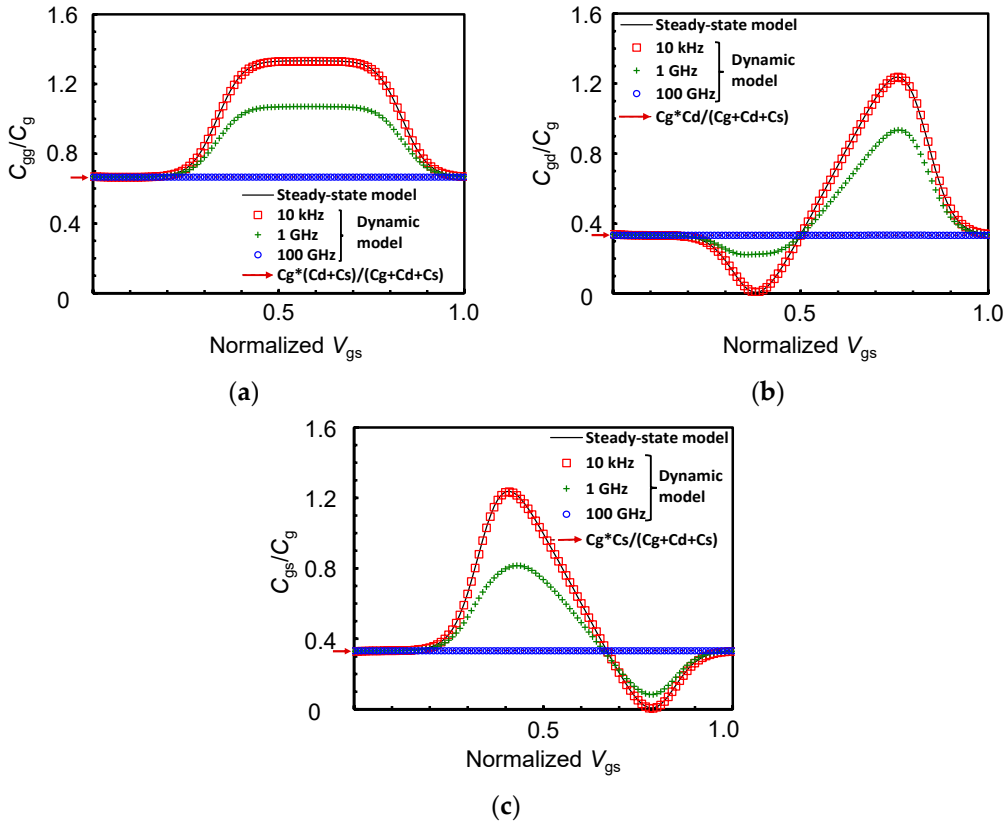


Figure 4. (**a**) SET input capacitance C_{gg} (**b**) drain-to-gate capacitance C_{gd} and (**c**) source-to-gate capacitance C_{gs} as a function of gate voltage V_{gs} for a high drain voltage V_{ds} = 26.7 mV [0.5] at T = 15.5 K [0.05].

3.2. Frequency Dependence of Capacitances

Figure 5 shows the gate input capacitance C_{gg} as a function of frequency at low and high drain voltages of $e/C_{\Sigma}/100$ and $e/C_{\Sigma}/2$, respectively. It can be seen that the C_{gg} starts to decrease at a frequency about an order of magnitude lower than the cutoff frequency (1 GHz) and approaches the dashed line at higher frequencies, which can be explained again as the approach to the condition of passive capacitance circuit consisting of C_g, C_d and C_s. From such an analysis, we can quantitatively understand the frequency-dependent behaviors of the capacitances inside the SET.

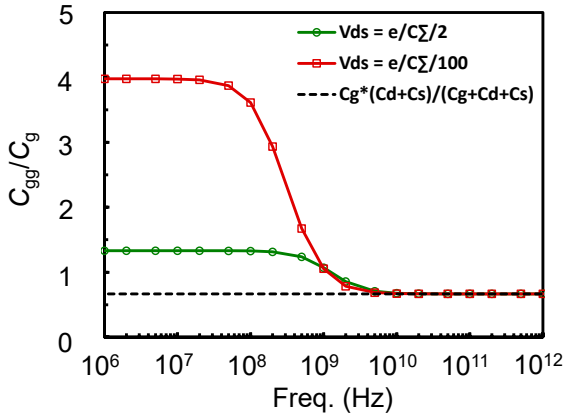


Figure 5. SET input capacitance C_{gg} as a function of frequency at drain voltages V_{ds} = 0.534 mV [0.01] and 26.7 mV [0.5], gate voltages V_{gs} = 80.1 mV [0.5] and 93.5 mV [0.6] and T = 15.5 K [0.05].

3.3. Temperature Dependence of Capacitances

Figure 6 shows the gate input capacitance C_{gg} as a function of temperature at low and high drain voltages of $e/C_{\Sigma}/100$ and $e/C_{\Sigma}/2$, respectively. The simulation is performed up to the temperature of 15.5 K [0.5] because the proposed model is accurate up to this temperature, as was previously discussed.

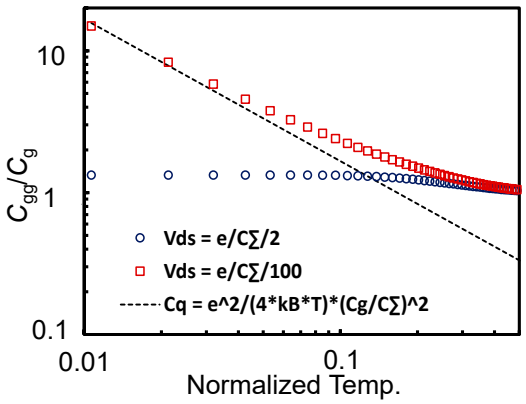


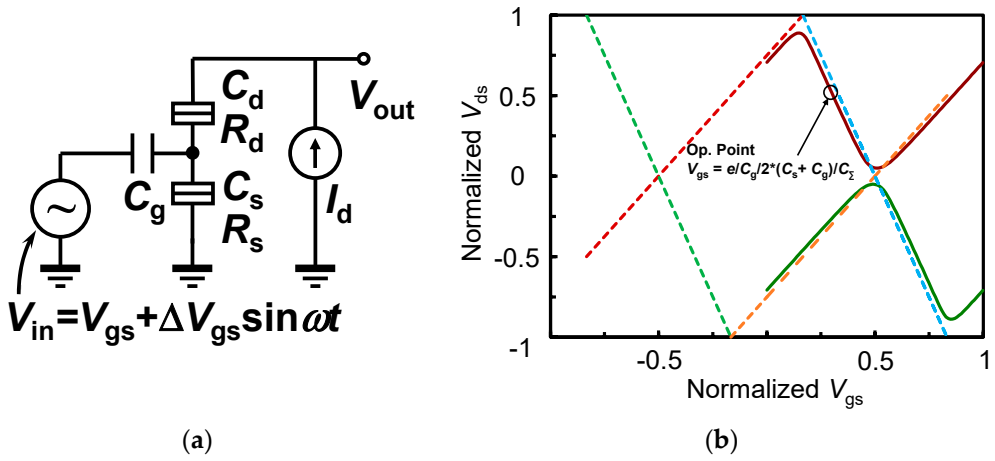
Figure 6. SET input capacitance C_{gg} as a function of temperature at drain voltages V_{ds} = 0.534 mV [0.01] and 26.7 mV [0.5], and gate voltages V_{gs} = 80.1 mV [0.5] and 93.5 mV [0.6], respectively.

For a small V_{ds}, C_{gg} increases as the temperature decreases almost inversely proportional to the temperature as predicted by the quantum capacitance C_q (dashed line) [7]. This is due to the steeper change of the island charge with respect to the V_{gs} at lower temperatures. For a large V_{ds}, the change of the island charge is gentle due to the wider transition region between n = 0 and 1, and thus the C_{gg} is small and insensitive to the temperature.

At higher temperatures, the C_{gg} assumes the common and nearly constant value as the Coulomb blockade is lifted, and the proposed model can describe the behavior up to the normalized temperature of 0.5 in contrast to the simplified equation of C_q.

3.4. Characteristics of the SET-Based Amplifier

Figure 7a shows the circuit diagram of the SET-based inverting amplifier with a constant-current load, and Figure 7b describes the operation point in the Coulomb diamond (CD) plot. The operation point is set at the center of the descending side in the input-output (V_{ds}-V_{gs}) characteristics for the I_d = ±26.7 pA [=(V_{ds}/4 R_t)/10 with V_{ds} = e/C_{Σ}/2].



(**a**) (**b**)

Figure 7. (**a**) A circuit diagram of the SET-based inverting amplifier with constant-current load, and (**b**) Coulomb diamond (CD) plot with V_{ds}-V_{gs} curves for I_d = ±26.7 pA at T = 15.5 K [0.05]. The operation point of the amplifier is set at the center of the descending side.

To evaluate the frequency response of the amplifier, small sinusoidal fluctuation with amplitude ΔV_{gs} (=$e/C_g/1000$) is added to the gate bias V_{gs}, and the fluctuation in V_{out} is observed by the simulation.

Figure 8 depicts the frequency response of the SET-based amplifier. At low frequencies, the voltage gain close to the slope of the descending side of the CD (=C_g/C_d) is obtained, and the phase is inverted. At high frequencies, the transistor action is lifted, the gain becomes that of passive capacitive divider consisting of the C_g and C_s, and the output is in phase with the input. Interestingly, the gain and phase start to change at higher frequency compared to the case in Figure 5 probably due to the high-impedance condition at the output terminal.

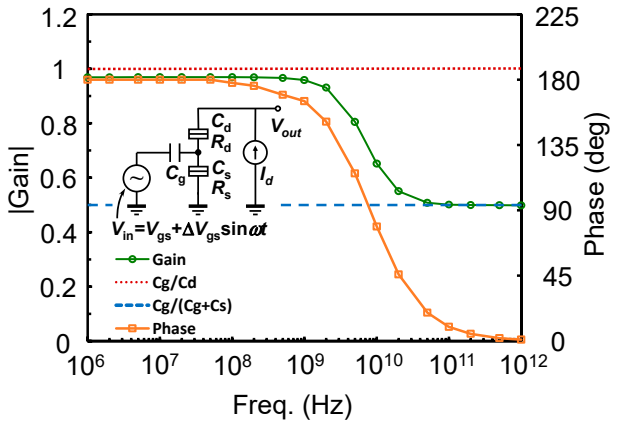


Figure 8. Frequency response of the SET inverting amplifier operating at a drain current I_d = 26.4 pA, gate voltage V_{gs} = 53.4 mV [0.33] (center of the descending side of the CD) and T = 15.5 K [0.05].

The input capacitance C_{gg} is also simulated as a function of the gate voltage V_{gs} at three different frequencies and shown in Figure 9.

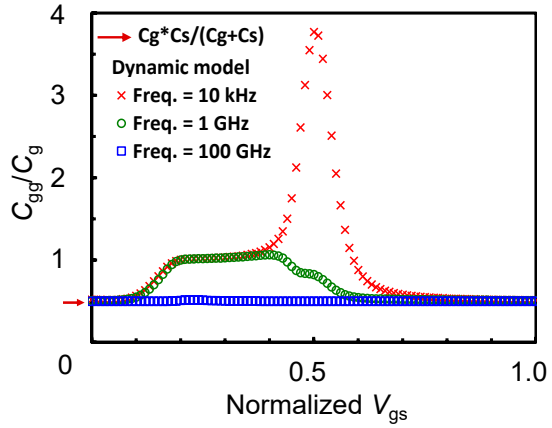


Figure 9. SET input capacitance C_{gg} as a function of the gate voltage V_{gs} for a drain current I_d = 26.7 pA at T = 15.5 K [0.05].

As can be seen in the figure at the low frequency (10 kHz), the C_{gg} shows a high peak at V_{gs} = 0.5 e/C_g due to the small V_{ds} and resultant abrupt change in the island charge. At the cutoff frequency (1 GHz), the peak height is reduced largely, and at the high frequency (100 GHz), the C_{gg} levels off to the baseline value that corresponds to the series connection of C_g and C_s as shown in the expression in the legend. Such behavior again verifies that the SET behaves like a passive circuit of capacitors at high frequencies.

Another interesting finding in Figure 9 is that the Miller effect [6] is not conspicuous in the SET-based amplifier as the C_{gg} at the operation point (V_{gs} = 0.33 e/C_g) is almost the same as that in Figure 4a because the feedback capacitance C_{gd} is negligibly small as shown

in Figure 4b, suggesting that it is only necessary to take care of the parasitic capacitance when we discuss the Miller effect in the SET-based amplifier.

We have focused on the intrinsic SET characteristics so far. In reality, lead lines connected to the terminals are always accompanied by parasitic components such as capacitance, inductance, resistance, etc. As an example of a real circuit, an inverting amplifier with a load capacitance C_L is analyzed (Figure 10). Actually, each terminal of SET should be connected to a constant-voltage source or a capacitor sufficiently larger than C_Σ so that the SET can be regarded as an independent circuit element [13], and this time the C_L is set to 30 aF (=10 C_Σ). As a consequence, the cutoff frequency $f_{C\text{-}CL}$ of 53.1 MHz ($=\frac{1}{4\pi R_\Sigma C_L}$) consisting of SET output resistance and C_L dominates the low-frequency part of the frequency response.

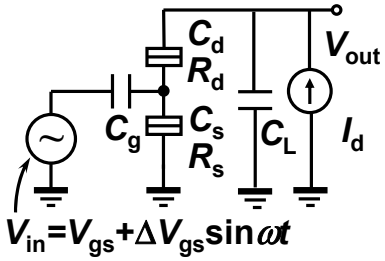


Figure 10. A circuit diagram of the SET-based inverting amplifier with constant-current load and load capacitance C_L.

Figure 11 compares the frequency responses of SET-based amplifier with a load capacitor, simulated by the proposed transient model and the steady-state model [13]. From both curves we can see that at low frequencies voltage gain is equal to the slope of the descending side of CD, and the phase is inverted. The gain starts to decrease at around $f_{C\text{-}CL}$, and continues to decrease in proportional to $1/f$, but further drop is observed by the transient model at around f_C where transistor action is lifted. Such a drop cannot be described by the steady-state model because the model itself is frequency-independent. The phase starts to decrease at around $f_{C\text{-}CL}$ and becomes saturated at 90 deg in case of the steady-state model, but it continues to decrease in the case of the transient model and finally gets saturated at −90 deg, reflecting the transition from inverting to non-inverting operations at high frequencies above the f_C as observed in Figure 8, which also cannot be expressed by the steady-state model. These results clearly demonstrate the importance of the proposed transient model in accurately describing the high-frequency behavior of the real circuits.

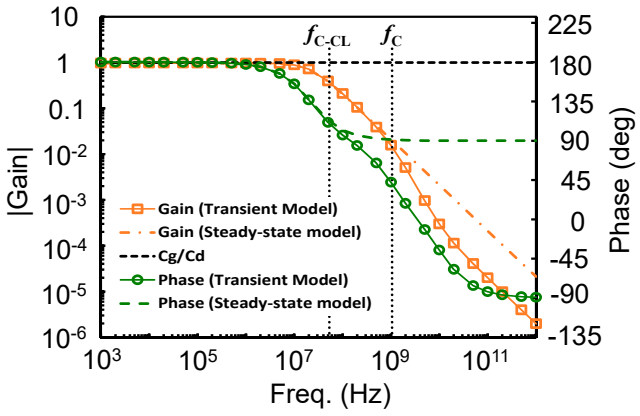


Figure 11. The frequency response of the SET inverting amplifier with a load capacitor C_L = 30 aF (10 C_Σ) operating at a drain current I_d = 26.4 pA, gate voltage V_{gs} = 53.4 mV [0.33] (center of the descending side of the CD) and T = 15.5 K [0.05].

Note that the relatively low $f_{C\text{-}CL}$ and f_C could be increased by three orders of magnitude at the highest by decreasing the tunneling resistance to the level of the resistance quantum [32]. There is also room for decreasing the capacitance parameters by size reduction to increase the cutoff frequencies.

4. Conclusions

A model for SETs was proposed based on the time-dependent master equation and taking dynamic gate current into account, and it was realized by using the SPICE circuit simulator as a solver for simultaneous differential equations. Based on this model, intrinsic terminal capacitances and transcapacitances in the SET were discussed as a function of gate voltage, frequency, and temperature. It was concluded that, at low frequencies, the capacitances depended on the biasing but, at high frequencies, the transistor action of the SET was lifted, and it acted as a passive capacitance circuit. Such a transition from the low-frequency to high-frequency characteristics of the SET could be described quantitatively by the proposed model. Also, the model could analyze the behavior of the SET covering a wide range of temperature, in which the C_{gg} for small V_{ds} was inversely proportional to the temperature on the low-temperature side, and the C_{gg} assumed the constant value insensitive to the temperature or V_{ds} on the high-temperature side.

In addition, the frequency response of the SET-based amplifier was investigated. The transformation from inverting amplifier at low frequencies to the capacitive divider at high frequencies was successfully described. It was also found that the Miller effect is not conspicuous in the SET-based amplifier due to the negligible feedback capacitance at the operation point.

From these results, we can expect that the proposed model can be widely used to analyze the circuits, including SETs for high-frequency amplification, oscillation, detection, qubits readout by gate-based sensing, and so on.

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