Study on High-Frequency Response of Single-Electron Transistors

DOCTORAL DISSERTATION

Study on High-Frequency Response of Single-Electron Transistors

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博士論文

単電子トランジスタの高周波応答に関する研究

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Abstract

Single-electron transistor (SET) is a three terminal device which has gained popularity in the field of nanoelectronics due to its advanced and attractive features i.e., small size, low power consumption, high functionality, etc.

Aggressive scaling of circuits with conventional scaled-down FETs have almost reached the limit, and SETs have the potential to replace FETs in the circuit for further scaling. However, it should be noted that replacing conventional transistors with SETs in the circuits can have desirable and undesirable consequences, and as a result careful evaluation of SETs behavior is crucial. Looking at the demand of future electronics, devices with high-speed/high-frequency capability are anticipated.

Traditionally, it was believed that SETs are slow due to high tunneling resistance ($R_T > 25.8\, k\Omega$). However, due to advanced nanofabrication technology it is now possible to fabricate SETs with capacitances in the range of attofarad. As a result, subpicosecond intrinsic time constant can be achieved bringing about an opportunity in high-speed or high-frequency operation.

Till now high-frequency operation of SETs has been discussed simply based on this small intrinsic time constant. Nevertheless, with advances in nanofabrication technology it is worthwhile to analyze the high-frequency

dynamic behavior of the SET in more detail. For this reason, rectifying effect of SET at high frequencies and capacitance components in a SET at high frequencies need to be discussed.

SET as a high frequency rectifier

It was reported that there seems no cutoff frequency in the rectifying operation of SETs. Theoretical explanation behind such behavior is attempted for the first time through the simulation using SET model based on the time-dependent master equation. From the obtained results it was concluded that the asymmetry in the tunneling rate (rate with which electron tunnels into or out of the Coulomb island) with respect to the drain voltage is responsible for the rectifying operation at high frequencies. In order to verify the rectifying characteristics predicted by the simulation, SETs fabricated by the pattern-dependent oxidation (PADOX) and those based on the heavily doped Si nonowire were evaluated in terms of the frequency response of the rectifying current. In the former SETs, the intrinsic SET characteristics could not be observed since the cutoff frequency f_c of the parasitic MOSFET is lower than the intrinsic f_c of the SET. In the latter SETs the f_c of the parasitic low-pass filter in the lead is sufficiently high due to its low sheet resistance, but unexpected reduction of the rectifying current at low frequencies is observed. Further research on the parasitic components that have not been considered, and on the stability of SET are necessary.

The experimental verification will lead to a clear prospect for the rectifier application of SETs in the high-frequency regime where conventional devices cannot operate.

Capacitance components inside SET

Understanding of the capacitance components inside the SET is crucial to discuss its high-frequency operation. For that purpose, SET model based on the time-dependent master equation by taking the dynamic gate current into account has been proposed which can represent terminal capacitances and transcapacitances.

By using this model, bias, frequency and temperature dependences of these intrinsic capacitances are evaluated. It was concluded that, at low frequencies, the capacitances depended on the biasing but, at high frequencies, the transistor action of the SET was lifted, and it acted as a passive capacitor circuit. Such a transition from the low-frequency to high-frequency characteristics of the SET could be described quantitatively by the proposed model. Also, the model could analyze the behavior of the SET covering a wide range of temperature.

In addition, the frequency response of the SET-based amplifier was investigated. The transformation from inverting amplifier at low frequencies to the capacitive divider at high frequencies was successfully described. It was

also found that the Miller effect is not conspicuous in the SET-based amplifier due to the negligible feedback capacitance at the operation point.

From these results, we can expect that the proposed model can be widely used to analyze the circuits including SETs for high-frequency amplification, oscillation, detection, qubits readout by gate-based sensing, and so on.

Acknowledgment

My first set of thanks and gratitude of course goes to Prof. Hiroshi Inokawa for being my doctoral supervisor. His attitude and vision towards science is something to look up to. His help in constantly improving my scientific outlook, to try and question every article I read and to give acute attention to figures, desi$_{gn}$s and other details that I thought to be trivial in the beginning is something that will remain with me for long, hopefully lifetime. He was a constant source of inspiration throughout this journey and without his guidance this couldn't have been possible.

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Chapter 1

INTRODUCTION

1.1 Research background

The idea of single-electron transistors (SETs) was proposed in the year of 1986 [1], and in the year 1987 first SET was fabricated and operation was confirmed for the first time [2]. Since then, continuous progresses have been made to understand its behavior and functionality. SET has many advanced features like small size, small number of electrons involved in its operation, periodic transfer characteristics, and hence it has a potential to replace conventional transistors in integrated circuits. However, understanding of high-speed/high-frequency capability of SET is one of the main issues to be discussed in comparison with the conventional transistors, and the purpose of my research.

High-frequency operation of SETs has been discussed before simply based on small intrinsic time constant. However, with advance nanofabrication technology that leads subpicosecond time constant, it is worthwhile to analyze the high-frequency dynamic behavior of the SET in more detail. For this purpose, I have analyzed:

- High-frequency rectifying behavior of SET

- Intrinsic capacitance components of the SET

1.1.1 Operation principle of SET

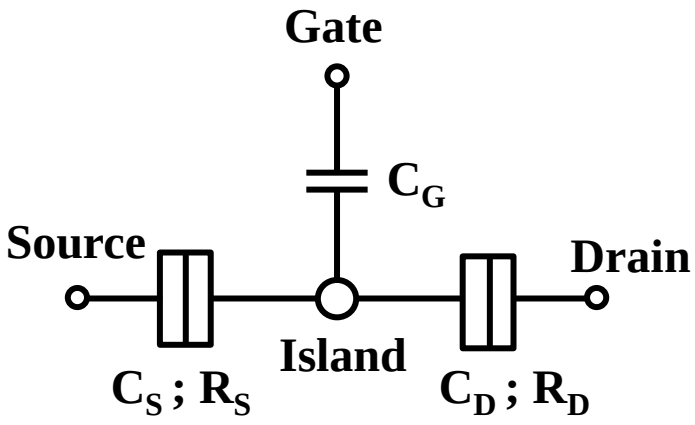

Fig. 1: Schematic diagram of basic SET

SETs (Fig. 1) are the one of the most primitive single-electron devices which works on the principle of Coulomb blockade (CB). It is a three-terminal device with a small island at the center which is connected to the drain and source terminal through a tunneling junction and is capacitively coupled to the gate terminal. Since the size of the SETs are in the range of nanometer the behavior of SET is predominantly governed by quantum mechanical effects. Two main operation conditions of SETs are CB and single-electron tunneling [1]–[5]. To observe these phenomena:

a. Charging energy W_c of single excess electron on a quantum dot should be greater than thermal energy $k_B T$.

$W_c = \frac{e^2}{2C} \gg k_B T$; Where C = Capacitance of quantum dot

T = Temperature of the system

b. Tunneling resistance R_t should be larger than quantum resistance h/e^2

$$R_t = \frac{h}{e^2} = 25.8\ k\Omega$$

Working principle of SETs is like a MOSFET where gate terminal controls the movement of electrons between drain and source. When gate and bias voltages are zero there is no current flow in the SET. As we increase the bias voltage electron can hop onto island when charging energy W_C is equal to the Coulomb energy $e^2/2C$ and current will flow when electron tunnels in from source to island and tunnel out from island to drain, keeping excess electron on the island constant. This process is called the Coulomb blockade and the voltage required to tunnel one electron on the island is called the Coulomb gap voltage given by e/C [2][6][7].

SETs have many desirable features i.e., small size, small number of electrons, periodic transfer function etc. and therefore it has potential to replace FETs in many applications. Nevertheless there believed to be many associated drawbacks as well which is limiting the full-fledged utilization of SETs [5] i.e., slow speed, fabrication difficulty, low operation temperature, experimental difficulties, etc. Anyhow, aggressive miniaturization of transistors is reaching the physical limit and further consideration of all the

believed drawbacks are important as it can play crucial role in continued miniaturization of transistors.

1.1.2 High-speed/High-frequency operation of SET

In the beginning it was believed that one of the major drawbacks of SET was low operation speed [8]–[10]. Three main reasons for which was:

1. Firstly, since the operation frequency of SET is determined by the RC time constant and the value of tunneling resistance should be higher than quantum resistance = 25.8 kΩ, the resultant RC cutoff frequency of conventional SET was assumed to be low.
2. Secondly, high-frequency characteristics of SET was not evaluated as the voltage at the drain terminal was supposed to be kept low to maintain the CB condition.
3. Thirdly, difficulties related to the fabrication of such small device.

Over the years high-speed operation of SET and fabrication methods to achieve the reduced dimension of SETs have been studied intensively. Many journal articles were published throughout the world with regards to the operational speed of the SET and gradually it was concluded that RC time constant can be made small to achieve the high-speed operation [7][11][12].

A wide number of high-speed SET based application has already been proposed. Kouwenhoven et al. proposed RF turnstile devices; the intrinsic frequency response of SET was very high due to small capacitor[13]. J. Pettersson et al. proposed SET with an InP high-electron-mobility transistor [9]. The external load capacitance was reduced from 1 nF to less than 1 pF by adding high-electron-mobility transistor and on-chip biasing resistor. The cutoff frequency of 700 kHz was obtained. R. J. Schoelkopf et al. proposed RF SET which can be operate at frequency 100 MHz or more [8]. Y. Takahashi et al. merged a SET and 1D MOSFET into a memory device which featured a high-speed operation [14]. H. Inokawa and Y. Takahashi proposed SET-based 7-3 counter which can operate at moderated speed of 100 MHz [15]. G. Yamahata et al. discussed high-speed single-electron transfer via a small island electrically formed using silicon transistors and via a trap level in silicon for which a high speed of 3.5 GHz was achieved [16]. Y. Takahashi et al. fabricated SET by PADOX method and evaluated high frequency limit of SET operation [10]. It was observed that there seems no cutoff frequency in the rectifying effect set by RC delay.

To address the second issue in achieving high-speed operation of SET Y. Takahashi et al. proposed a new technique to evaluate the high-frequency limit of operation of SET [10]. They utilized rectifying effect of SETs for this purpose.

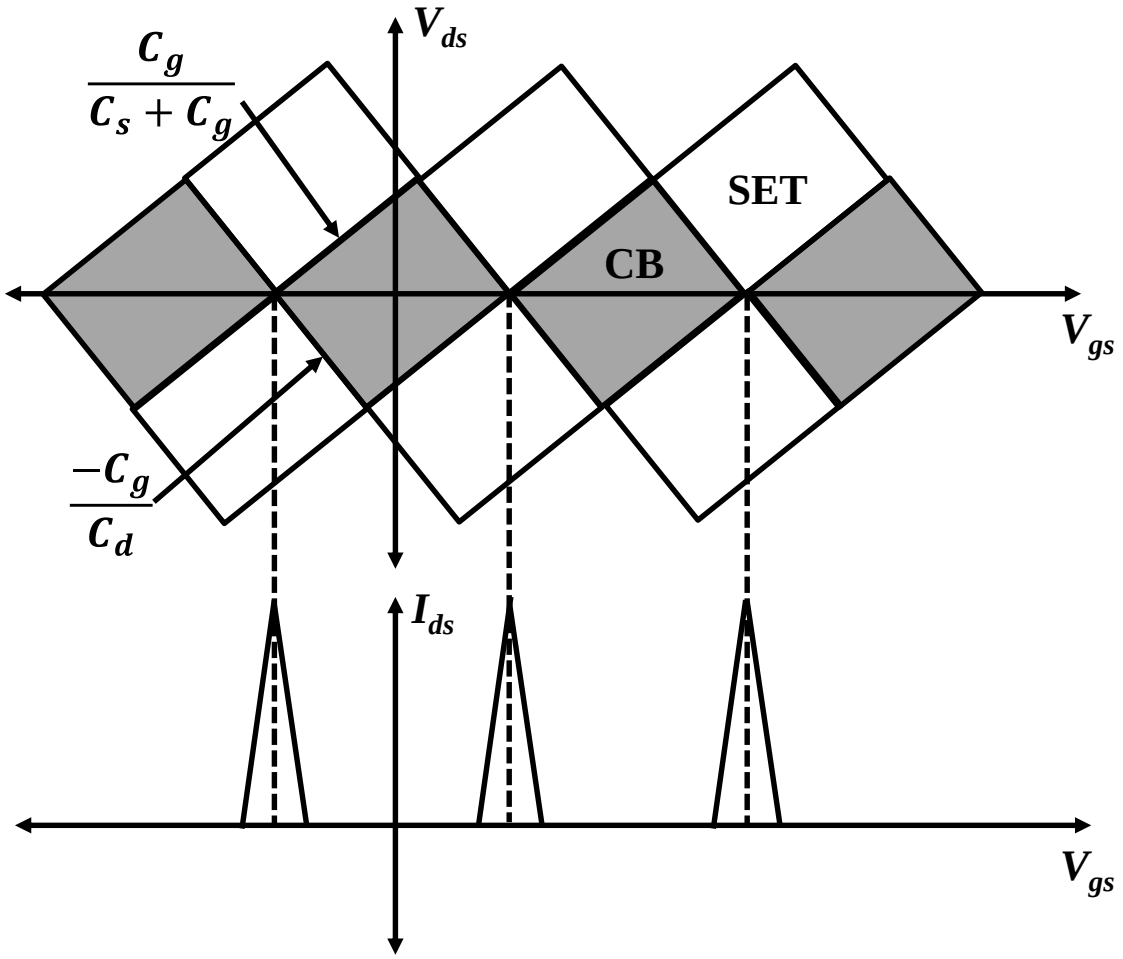

Fig. 2: Coulomb blockade boundary and corresponding drain current

As shown in Fig. 2 the slope of the Coulomb blockade (CB) region in SET is determined by the capacitance ratios $C_g/(C_s+C_g)$ and $-C_g/C_d$ which is asymmetric in shape and causes rectification as shown in Fig. 3. When AC voltage is applied to the drain, the average drain current I_d becomes nonzero (positive or negative) depending on the gate voltage V_g that affects the inclusion relation between the amplitude and the CB region where current

flow is prohibited [17]. This is a well-known characteristics of SET which has already been discussed previously [18][19][20].

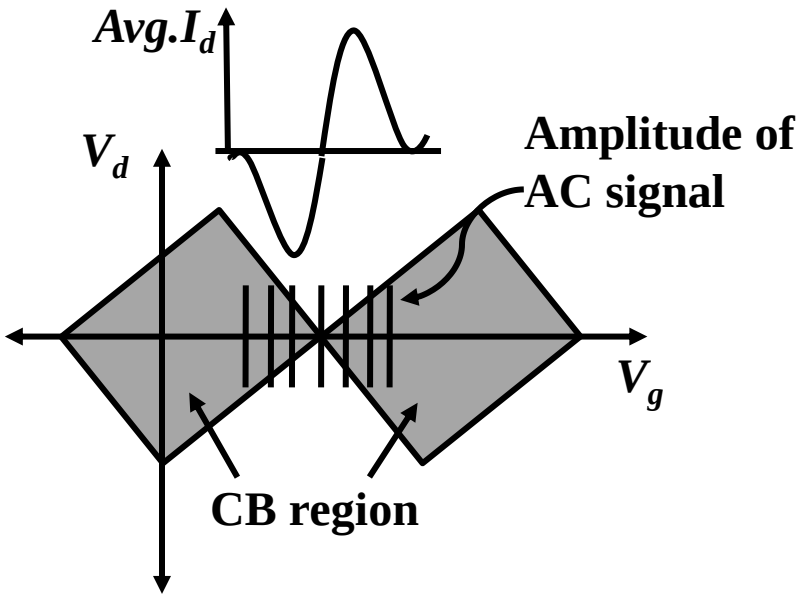

Fig. 3: Rectification in SETs

Using this phenomenon the frequency response of SET was simulated and it was reported that there is no cutoff frequency in the rectifying effect set by RC delay [10]. Using this feature of SET high-frequency characteristics of SET can be evaluated without disturbing the CB condition.

The third issue in realizing the high-speed operation of SET is related to the fabrication difficulties. However, due to ever-evolving advanced nanofabrication technology it now possible to fabricate small SETs with capacitances in the order of attofarad. Resulting room temperature operation

and Subpicosecond intrinsic time constant set by RC time constant. Some of the examples are SET fabricated by PADOX method, Heavily doped Si nanowire-based SET, SET with multiple-island channel, etc. One of the simple technique to fabricate the SET is through PADOX method [20][21]. In this method silicon nanowire gets converted into a silicon island in a self-aligned manner. This type of SET has advantages like high-temperature operation, high stability, and tunable tunnel barrier. Apart from SET fabricated by PADOX method there are other types of SETs as well which are suitable for high-frequency operation i.e., heavily doped Si nanowire-based SET and SET with multiple islands. In heavily doped Si nanowire based SETs island are formed generally by the random fluctuation of dopants [23][24][25]. This type of devices has reduced series resistance. On the other hand SET with multiple island can be fabricated as a 1D array of nanoscale island on SOI layer by EBL[26]. This type of devices can be operated at room temperature has suppressed cotunneling and large peak to valley current ratio.

Apart from above discussed points understanding of capacitance components inside the SET is crucial to discuss the high-frequency operation. Recently, charge detection for qubit readout is attempted by observing the gate input capacitance [27], which also requires SET models with capacitance analysis capability. Previously, analytical SET capacitance model based on steady-state master equation was proposed but the derived capacitances were frequency independent [28]. Hence, further advancement in the model is

necessary for evaluating the behavior of capacitances inside the SET near or above the cutoff frequency.

From the above discussion it is concluded that SET can have high-speed/high-frequency operation. High-frequency operation of SETs has been discussed previously simply based on the small intrinsic time constant but with advance nanofabrication technology it is worthwhile to analyze the high-frequency dynamic behavior of the SET in more detail.

1.2 Purpose of the research

The main purpose of this research is to contribute to the understanding of high-frequency behavior of the SET. For this purpose, following topics has been analyzed

- Rectifying operation of SET at high frequencies
- Capacitance components in a SET at high frequencies

High-frequency rectifying operation of SET has already been investigated [10] and it was reported that rectification can be observed 10 order magnitude higher than the cutoff frequency set by RC time constant. We took this work further by simulating the reason behind such behavior for the first time and concluded that asymmetry in the tunneling rate with respect to the drain voltage V_d is responsible for the rectifying operation at high frequencies [17]. Furthermore experimental verification of the simulated result is attempted [29]. For experimental verification SET fabricated by PADOX method is analyzed initially and it is concluded that this type of

device is not suitable for high frequency measurement due to low cutoff frequency of parasitic MOSFETs. As a result, heavily doped nanowire-based SETs are analyzed for high frequency measurement. To understand the frequency response of the SETs, measurement setup and contact resistance of the pad area and measurement probe has been discussed further. Experimental verification is necessary as such verification will help realizing the SET as a high frequency rectifier where conventional devices cannot operate.

Capacitance components inside the SET has previously been discussed based on the steady state model [28]. However, the derived capacitances were frequency independent. To study the dynamic behavior of capacitances inside the SET we newly proposed SET model based on time-dependent master equation by keeping dynamic gate current into account. Proposed model has the capability to analyze dynamic behavior of capacitances for the first time. Also, using this model frequency, bias, and temperature dependent behavior of the SET can be analyzed quantitatively. Since proposed model has used SPICE circuit simulator as a solver it can be used to analyze the circuits including SETs for high-frequency amplification, oscillation, qubits readout by gate-based sensing and so on.

1.3 Synopsis of the book chapters

This thesis consists of four chapters and each chapter content is summarized as follows.

Chapter 2 consists of simulation work. In the beginning time dependent master equation is discussed. By solving the master equation drain and gate

current equation has been obtained and using the equations SET model for simulation has been proposed.

In the first part, simulation results of the SET as a high-frequency rectifier have been discussed. Which includes frequency response of the rectified current and reasons behind the rectification above cutoff frequency. In the second part capacitance components inside the SET has been discussed. It includes simulation results of bias, frequency, and temperature dependence of the capacitance components of SET. Also, simulation result of SET as a voltage rectifier is discussed. Under which frequency response of the amplifier and Miller effect has been discussed.

Chapter 3 focuses on the experimental aspect of high frequency response of various SETs. In this chapter we have discussed about different types of SETs namely

- Heavily doped Silicon nanowire-based SET
- SET with multiple island channel structure
- SET fabricated by PADOX method.

and its high frequency response. We also have discussed about the factors which needs to be considered carefully to evaluate the real frequency response of SET devices.

Chapter 4 provides the summary, conclusion, limitations of the present work and suggestion for future work in this area.

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Chapter 2

SINGLE ELECTRON TRANSISTOR (SET) MODELING AND HIGH FREQUENCY SET SIMULATION

To understand the high-frequency dynamic behavior of single electron transistor we simulated its rectifying operation and internal capacitance components at high frequencies.

For this purpose, SET modeling is important. To analyze the high-frequency dynamic behavior of the SET, time dependent master equation is solved and based on the solution SET model is proposed.

2.1 Introduction to time dependent master equation

Design of single electron circuit has long been recognized and till now various models has been proposed. Generally, there are three types of SET models based on [1], [2], [3]:

- Steady state master equation [4], [5], [6]
- Monte Carlo method [2]
- Time-dependent master equation [7]

Among all the three types of modelling Monte Carlo method is superior to all the other approaches as it gives better transient and dynamic characteristics of the SET, information of relevant state is not required for starting the simulation etc. [2]. However, one major disadvantage is its limitations when

it comes to cotunneling. Steady state master equation on the other hand is fast and simple. Nonetheless we can't evaluate the intrinsic parameter of SET through this approach. The third approach is based on time dependent master equation, which is simple and self-sufficient. Our simulation model as well is based on this approach.

Master equation is a process of electrons tunneling from island to island and thus circuit occupies different states [2]. We can only consider finite number of states to solve the master equation. This finite set of states along with the transition probability from one state to another is required to solve the master equation [2]. To understand the time-dependent master equation, state transition diagram of two states is shown in fig. 2.1.

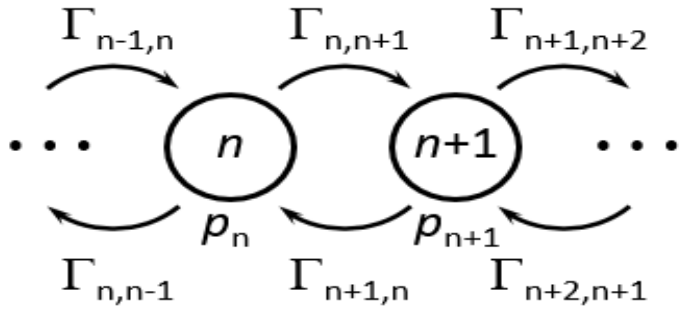


Fig. 2.1: State transition diagram

As we can see from the diagram probability of finding electron *n* on the island is given by p_n. The rate with which electron *n* will tunnel through the tunneling junction is given by $\Gamma_{n, n+1}$. This tunneling of electron accompanies a transition of electron number in the dot from *n* to *n*+1. Hence, probability of finding electron on the island will change to $p_{n+1.}$ This process of electron

tunneling from n to n+1 is described by the master equation. It can be represented as [4]:

$$\Gamma_{n,n+1} = \frac{1}{e^2 R_t} \frac{\Delta F(n, n+1)}{1 - \exp[-\Delta F(n, n+1)/k_B T}$$

Where, $\Delta F(n, n+1)$ is free energy change that accompanies the tunneling and R_t is tunneling resistance.

Free energy change associated with the transition of electrons number from n to n+1 is expressed with critical charges $Q_c = \frac{e}{2}(1 + \frac{C_g}{C_t})^{-1}$ and polarization charge on tunneling junction $Q_t = (V_g \times C_g - n \times e)/(C_g + C_t) \times C_t$, where, V_g is gate voltage, C_t and C_g is tunnel and gate capacitor, as:

$$\Delta F(n, n+1) = F(n) - F(n+1) = \frac{e}{C_t}(Q_t - Q_C)$$

There can be two types of tunneling with which electron can tunnel forward or backward and is represented by:

- $\Gamma_{n+1, n} = \Gamma_{s, n+1, n} + \Gamma_{d, n+1, n}$; backward tunneling, from *n+1* state to *n* state
- $\Gamma_{n, n+1} = \Gamma_{s, n, n+1} + \Gamma_{d, n, n+1}$; forward tunneling, from *n* state to *n+1* state

Where, transition rate is given by the summation of tunneling rate through source and drain junction.

2.2 SET Simulation Modelling

Our proposed SET model is based on time dependent master equation and number of electrons in the Coulomb island is limited to four (-1, 0, 1, 2).

Gate current I_g as well as the drain current I_d has been calculated using this model [8].

Drain current of the SET

Using the tunneling rate of electrons (discussed in the above section) we can calculate drain current through quantum dot.

The probability of finding electron in the island is given by the equation

Equation 1: $dp_n/dt = p_{n+1}\,\Gamma_{n+1,\,n} + p_{n-1}\,\Gamma_{n-1,\,n} - p_n\,[\,\Gamma_{n,\,n+1} + \Gamma_{n,\,n-1}]$

There also exists normalization condition given by equation

Equation 2: $\sum_{n=-1}^{2} p_n = 1$

Drain current which generates from the tunneling of electrons from one state to another state is given by solving both abovementioned equation:

$I_d = e\sum p_n\,[\Gamma_{d,\,n,\,n-1} - \Gamma_{d,\,n,\,n+1}]$

Gate current of the SET

Using potential and average charge of the Coulomb island we can calculate the gate current through SET .

Potential of the Coulomb island V_{isl} is given by

Equation 1: $V_{isl} = \frac{C_g V_g + C_s V_s + C_d V_d + Q_{isl}}{C_\Sigma}$

Average charge Q_{isl} in the Coulomb island is given by

Equation 2: $Q_{isl} = -e \times \sum n P_n$

On substituting equation 2 in equation 1, V_{isl} can be rewritten as

Equation 3: $V_{isl} = \frac{C_g V_g + C_s V_s + C_d V_d - e\sum nP_n}{C_\Sigma}$

Considering the gate current I_g flowing from gate terminal to the Coulomb island via gate capacitor the gate current can be expressed as change in charge at gate terminal Q_g with respect to time.

Equation 4: $I_g = \frac{dQ_g}{dt} = \frac{d}{dt}\left(V_g - V_{isl}\right) \times C_g$

$$= \frac{d}{dt}\left\{\frac{C_g}{C_\Sigma}\left(V_g C_\Sigma - C_g V_g - C_d V_d - C_s V_s + e\sum nP_n\right)\right\}$$

Here, C_g, C_s, and C_d are the gate source and drain capacitor and $C_\Sigma = C_g + C_s + C_d$ and V_g, V_s and V_d are gate source and drain voltages.

The SPICE circuit simulator is used as a solver for the simultaneous differential equation, which also enables the model to analyze the behavior of various circuits including SETs.

2.3 SET as high frequency rectifier simulation

To determine the high frequency operation limit of SET, Y. Takahashi et.al. employed rectifying behavior of SET which happens due to asymmetry of the Coulomb diamond. It was observed that rectifying operation continues above the conventional cutoff frequency set by RC time constant [9]. Which results in the rectifying effect to be usable beyond the THz regime.

In our first part of simulation, we firstly reconfirmed the finding of operation far beyond the conventional cutoff frequency. And further we successfully attempted the theoretical explanation behind such behavior for the first time [7].

Shown in Figure 2.2 is the schematic circuit diagram to operated SET as a rectifier and simulation parameters are summarized in the Table 1.

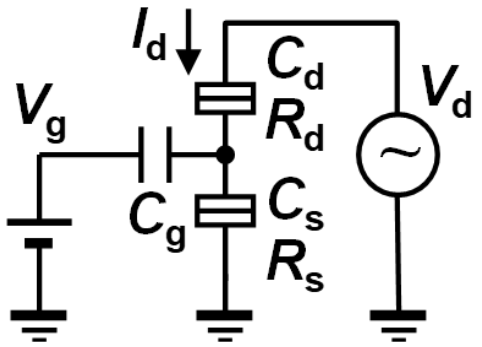


Fig. 2.2: Schematic circuit diagram to operated SET as a rectifier

Table 1: Simulation Parameters

Drain Voltage, V_d	**$\pm$5.34 mV [0.2]**
Gate Voltage, V_g	**44.5 mV**
Temperature, T	**1.55 K [0.01]**
Gate, Drain and Source Capacitor, $C_g = C_d = C_s$	**2 aF**
Tunnel Resistors, $R_d = R_s$	**2.5 GΩ**
Cutoff frequency, $f_c = 1/(2\pi R_\Sigma C_\Sigma)$	**5.31 MHz**

[ ] indicates normalized temperature $2C_\Sigma k_B T/e^2$ and normalized drain voltage e/C_Σ

Normalized values [] are used generally to see the various effects, clearly and easily. In this case of SET simulation, at the normalized values Coulomb

blockade effects are in effect and number of electrons on the quantum dot will take a fixed value [4], [10].

Initially, experimental findings that rectifying operation continues above the conventional cutoff frequency set by RC time constant is verified using the schematic circuit diagram to operated SET as a rectifier as shown in Fig 2.2 and parameters in Table 1. Rectified current (Average I_d) as a function of gate voltage V_g is simulated using LTspice circuit simulator at a constant drain voltage of ±5.34 mV and temperature 1.55 K (Fig. 2.3).

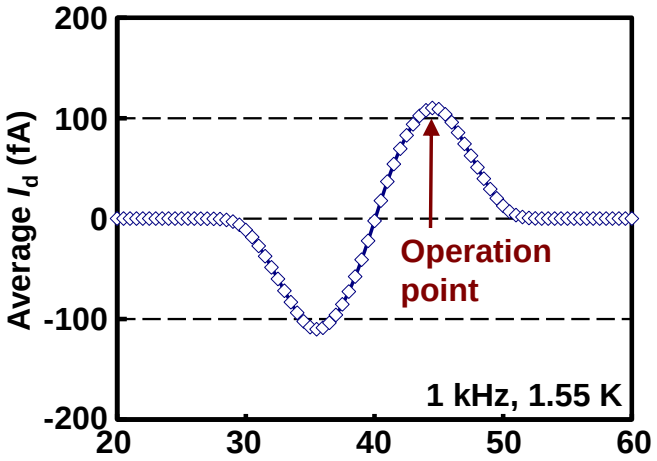


Fig. 2.3: Rectifying current vs. gate voltage V_g. C_g=C_d=C_s=2.0 aF, R_d=R_s=2.5 GΩ, V_d=±5.34 mV_{p-p} [0.2], T=1.55 K [0.01].

It can be seen from the graph that rectified current is becoming positive and negative depending on the gate voltage and hence rectification is reconfirmed. Next, to understand the frequency response of rectified current it is plotted as a function of frequency. Considering gate voltage to be 44.5 mV corresponding to the maximum drain current as an operation point rectified current is then plotted against the frequency (Figure 2.4).

Through Fig. 2.4 it is observed that the average drain current I_d drop at around the cutoff frequency $f_c = 1/(2\pi R_\Sigma C_\Sigma)$ set by RC time constant comprising of $C_\Sigma = C_g + C_d + C_s$ and $R_\Sigma = R_d + R_s$ but continues to assume a finite value up to 1 THz. This observation indicates that rectification can be observed far beyond the cutoff frequency of 5.31 MHz.

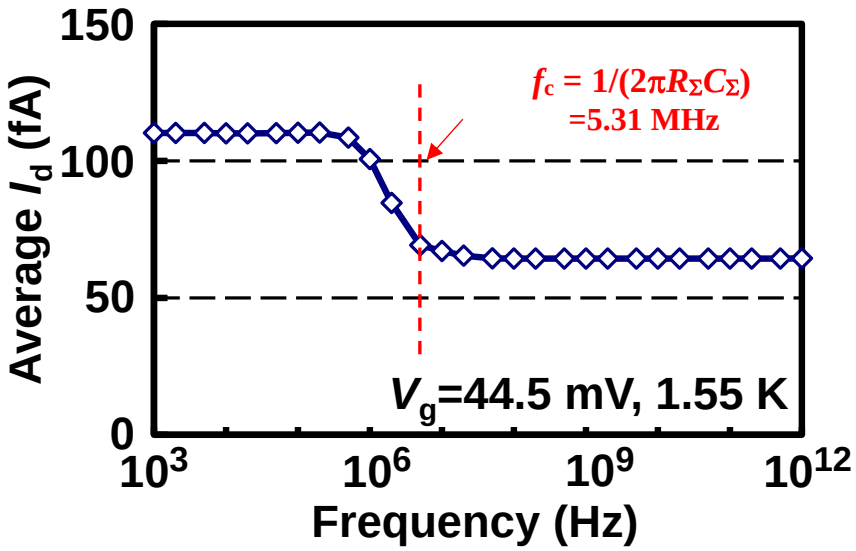


Fig. 2.4: Frequency response of the rectified current

To understand such frequency response of rectified current probability of state $p(n)$ and tunneling rate is discussed.

Firstly, probability of states $p(n)$ as a function of drain voltage V_d is simulated at representative low frequency of 1 kHz and high frequency of 100 MHz (Figure 2.5 and 2.6). As can be seen from the graphs at low frequency, $p(0)$ and $p(1)$ are nearly 0 and 1, respectively, around V_d=0, and increases and decreases asymmetrically as $|V_d|$ increases reflecting the asymmetry in the

Coulomb diamond region. However, at high frequency, $p(n)$ cannot follow the rapid change in V_d and becomes almost constant. This can also be seen in the contour plots of n (Figure 2.6). At high frequency, n depends only on V_g and the Coulomb diamond disappears. Hence, asymmetry is observed only at the low frequency not at the high frequency.

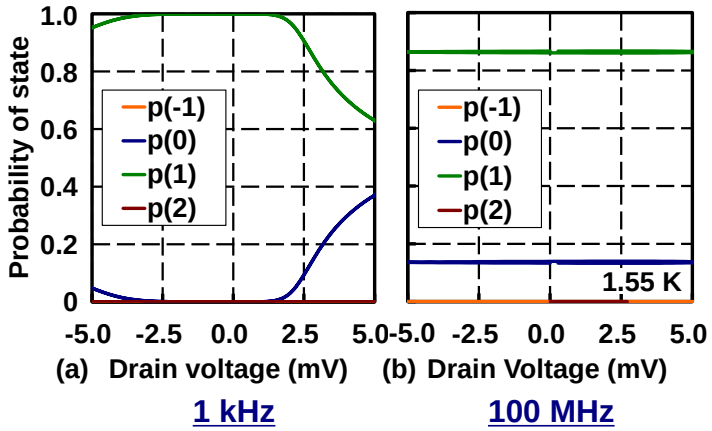


Fig. 2.5: Probability of state vs drain voltage at (a) low frequency (1 kHz) and (b) high frequency (100 MHz)

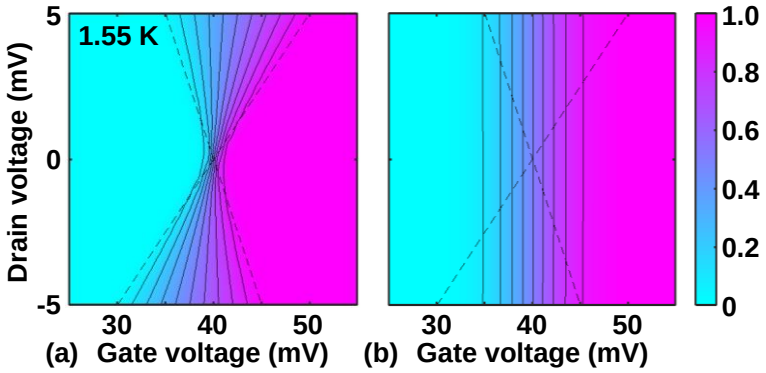


Fig. 2.6: Contour plots of the number of electrons in the Coulomb island at (a) low frequency (1 kHz), and (b) high frequency (100 MHz). Dashed lines represent the boundary of the Coulomb diamond set by the capacitance parameters C_g, C_d and C_s.

Next, the tunneling rate $\Gamma_{d,n,m}$ for transition from electron number n to m as a function of drain voltage V_d is simulated at representative low frequency

of 1 kHz and high frequency of 100 MHz (Figure 2.7). As can be seen from the graphs asymmetry in tunneling rates $\Gamma_{d,n,m}$ with respect to $V_d = 0$ is clearly visible at both the representative low and high frequencies. Hence, it is concluded that unlike probability of state $p(n)$ asymmetry can be visible in tunneling rates $\Gamma_{d,n,m}$ irrespective of the frequencies.

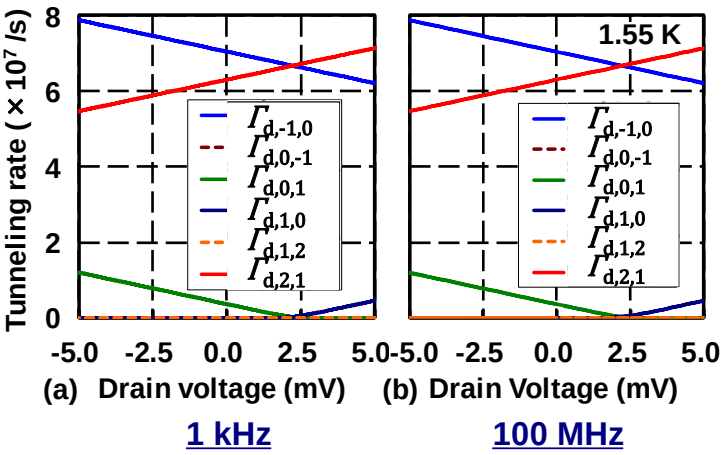


Fig. 2.7: Tunneling rate vs. drain voltage at (a) low frequency (1 kHz), and (b) high frequency (100 MHz).

Furthermore, the drain current I_d as a function of drain voltage V_d is plotted to understand the characteristics of drain current (Fig. 2.8). At low frequency, there is an asymmetric drain voltage V_d range with respect to drain current $I_d = 0$, which corresponds to the Coulomb blockade region. However, at high frequency, it is observed that current flows even at drain voltage $V_d = 0$ and a different curve of asymmetry has been appeared which is responsible for rectifying operation of SET at higher frequencies.

This characteristic of drain current can be explained from Figure 2.9. Figure 2.9 shows the I_d waveform in which at the lower frequency Coulomb

diamond (CD) is responsible for the cutoff region due to which there is no current flow. Whereas at the higher frequency CD has disappeared, causing continuous flow of current.

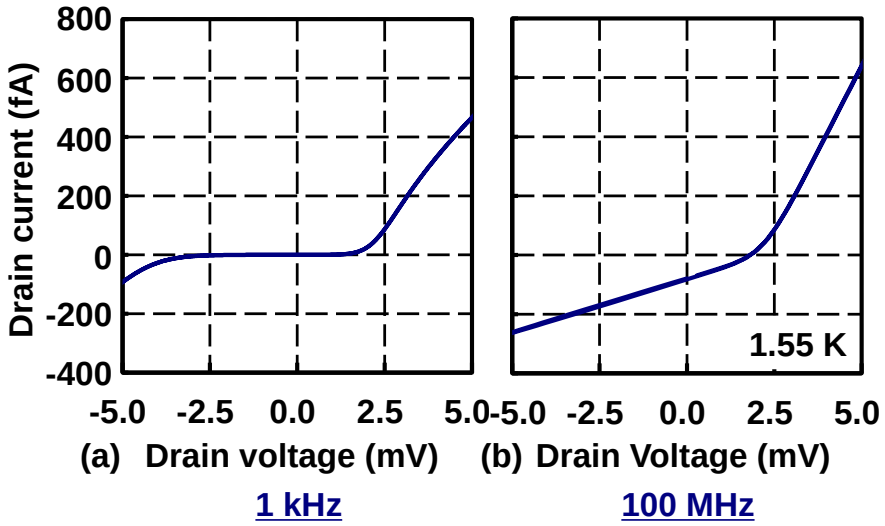


Fig. 2.8: Drain current vs. drain voltage at (a) low frequency (1 kHz), and (b) high frequency (100 MHz).

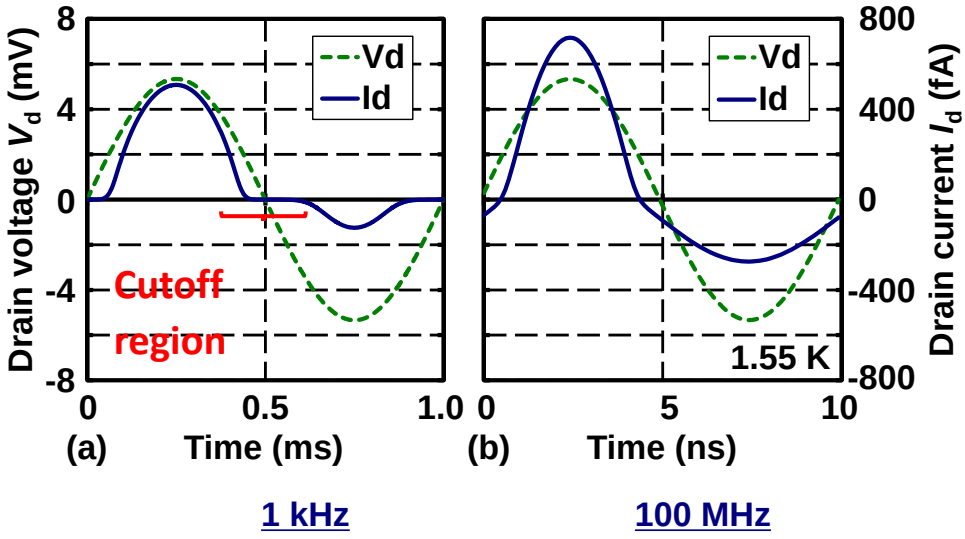


Fig. 2.9: Drain current wave form

Based on abovementioned discussion it is concluded that at high frequency unlike probability of states $p(n)$, the asymmetry in the tunneling rate Γ_d can be visible. This asymmetry in tunneling at high frequency is responsible for the asymmetry in drain current I_d (rectified current) resulting continued rectifying operation beyond cutoff frequency.

If main terms are considered, the drain current can be approximated in the form of equation as:

$$I_d \sim e \times [p(1) \times \Gamma_{d,1,0} - p(0) \times \Gamma_{d,0,1}]$$

Based on the proposed equation the reason behind drop in the rectified current at cutoff frequency shown in Fig. 2.4 as well can be explained. As the equation of suggests drain current depends on probability of state and tunneling rate. However, based on the abovementioned results it is concluded that at low frequency drain current depends on probability of state and tunneling rate whereas, at high frequency drain current depends only on the tunneling rate. Since at high frequency drain current depends only on one parameter a small drop can be observed at the cutoff frequency.

Summarizing abovementioned, results and theoretical explanations:

- It is stated that the simulation based on the time-dependent master equation has revealed that there is no cutoff frequency in the rectifying operation of SETs and rectification has been observed up to the 1 THz far beyond the cutoff frequency of 5.31 MHz

- Theoretical explanation behind such behavior is attempted and it is concluded that the asymmetry in the tunneling rate with respect to the drain voltage is responsible for the rectifying operation at high frequencies.
- This finding suggests that SET can becomes an important rectifier at ultrahigh frequencies where conventional devices cannot operate.

2.4 Dynamic input capacitance of SET simulation

To understand dynamic behavior of the SET in more detail understanding of the capacitance components inside the SET is crucial. For example, the Miller effect caused by the feedback capacitance largely affects the frequency response of amplifiers [11]. Recently, charge detection for qubit readout is attempted by observing the gate input capacitance [12]-[15] which also requires SET models with capacitance analysis capability.

Historically, high-speed or high-frequency performance of SET-based circuits have been studied with models based on steady-state master equation [16]-[23], under the assumption that the external load capacitance is much larger than the internal one, but the intrinsic high-frequency response of SETs cannot be assessed by the steady-state models. Even with such a model, it is still possible to derive the capacitance components such as terminal capacitances and transcapacitances inside the SET [18],[19], but the frequency dependence of capacitances cannot be evaluated.

Black-box models [24] and macro models [25] have similar features as long as they just provide an output current instantaneously as a function of terminal voltages.

Monte Carlo (MC) method [26]-[28] can simulate the dynamic or transient behavior of the intrinsic SET. Since the charges in the gate and source/drain tunnel capacitors are explicitly calculated, terminal capacitances and transcapacitances can also be derived from the simulation result. Actually, reference [29] discussed the input capacitance of SETs in conjunction with the electrometer sensitivity. However, MC method is usually not compatible with the standard circuit simulator such as SPICE and have difficulties in analyzing frequency-dependent behavior of SET itself or circuits including SETs and other circuit elements.

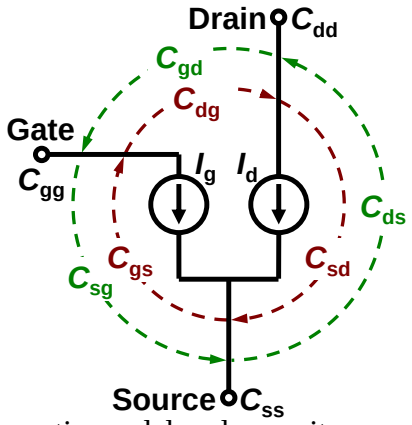


Fig. 2.10: Schematic model and capacitance components in SET

Table 2: Simulation parameter

Temperature, T	**15.49 K [0.05]**
Gate, Drain and Source Capacitor, $C_g = C_d = C_s$	**1 aF**
Tunnel Resistors, $R_d = R_s$	**25 MΩ**
Cutoff frequency, $f_c = 1/(2\pi R_\Sigma C_\Sigma)$	**1 GHz**

[ ] indicates normalized temperature $2C_\Sigma k_B T/e^2$

SET models based on time-dependent master equation that are capable of analyzing the dynamic behavior have been developed by many researchers [16],[30],[31]. Since the source/drain current can be directly expressed, implementation of the models to SPICE circuit simulator [32],[33] is also straightforward. However, to the best of our knowledge, there has been no model that can properly describe the terminal capacitances and transcapacitances.

Considering the above-mentioned background, we have proposed a SET model (Figure 2.10) based on the time-dependent master equation, taking the gate current into account [34]. Our model can not only analyze the high-frequency dynamic behavior of SETs, but also can represent terminal capacitances and transcapacitances. Since this model is implemented in the SPICE circuit simulator, it can be used to evaluate the high-frequency characteristics of various SET-based circuits such as amplifier, oscillator, detector, etc.

2.4.1 Input capacitance dependence on bias, frequency, and temperature

Using the proposed model and simulation parameters (Table 2) we extracted the capacitance components. Parameters in Table 2 are set rather arbitrarily to realize the cutoff frequency of 1 GHz where experimental verification is relatively easy and are also viable considering that the subattofarad capacitances have already been realized [35-37], and the tunneling resistance could be varied in a wide range by changing the insulator thickness. We also try to generalize the results by normalization, i.e., when the operation condition is described, temperature T, gate-source voltage V_{gs},

and drain-source voltage V_{ds} are normalized as $K_BT/(e^2/2C_\Sigma)$, C_gV_{gs}/e and $C_\Sigma V_{ds}/e$, respectively, and enclosed in square brackets [ ] if these are put down with raw values. The normalized V_{gs} ranges from 0 to 1 electron in the simulation since only n's from -1 to 2 are considered in solving the master equation. Two cases of small and moderate normalized V_{ds} of 0.01 and 0.5 are considered. The normalized temperature is set to 0.05 in most of the simulation in or-der not to thermally disturb the Coulomb blockade condition.

As shown in Fig. 2.10, a three-terminal SET has in total 9 terminal capacitances and transcapacitances. Since the I_g current source is newly added to the proposed model, the gate input capacitance C_{gg}, the drain-to-gate feedback capacitance C_{gd}, and source-to-gate capacitance C_{gs} can be extracted from the simulation.

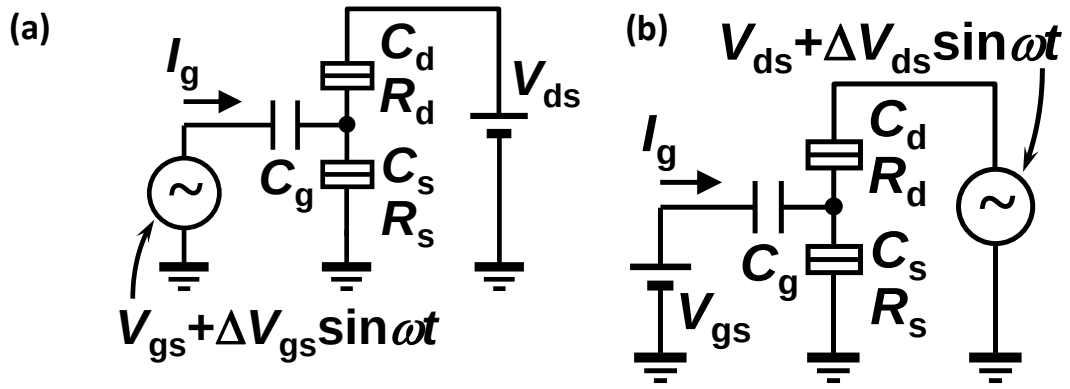


Fig. 2.11 Circuit diagrams for the measurement of (a) C_{gg} and (b) C_{gd}.

The C_{gg} is charge induced on the gate terminal capacitor by varying gate voltage and it can be evaluated using circuit shown in Figure 2.11(a) where small sinusoidal fluctuation with amplitude ΔV_{gs} (= $e/C_g/1000$) is added to the gate bias voltage V_{gs}, and then the amplitude ΔI_g of the gate current fluctuation is measured by the simulation. The C_{gg} is calculated by: $C_{gg} = (\Delta I_g)/(\omega \Delta V_{gs})$.

As shown in Fig. 2.11(b), the C_{gd} is charge induced on gate terminal by varying the drain voltage and is measured by adding small sinusoidal fluctuation with amplitude ΔV_{ds} (= $e/C_{\Sigma}/1000$) to the drain bias voltage V_{ds}, and the amplitude ΔI_g of the gate current fluctuation is observed. Similarly, the C_{gd} is obtained by: $C_{gd} = (\Delta I_g)/(\omega \Delta V_{ds})$.

Considering that the sum of C_{gd} and C_{gs} is equal to C_{gg}, the C_{gs} is given by

$C_{gs} = C_{gg} - C_{gd}$.

Simulation results

a) Gate bais dependence of capacitances

Figs. 12.12(a), (b) and (c) represent the C_{gg}, C_{gd}, and C_{gs}, respectively, as a function of gate voltage Vgs for a low drain voltage of $e/C_{\Sigma}/100$ at three different frequencies. The solid line shows the result of the steady-state model [18],[19], which coincides well with the data points (□) of the proposed model at a low frequency (10 kHz).

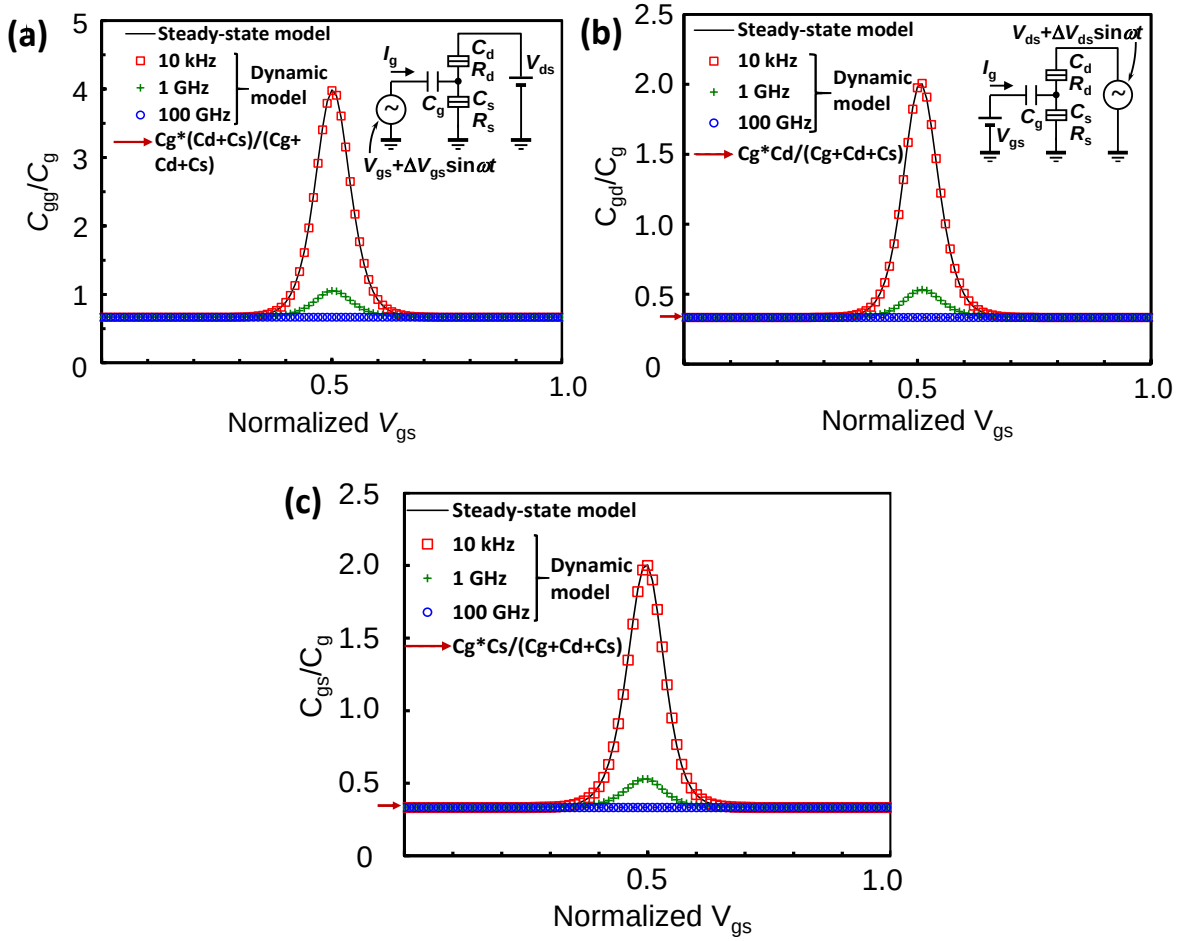
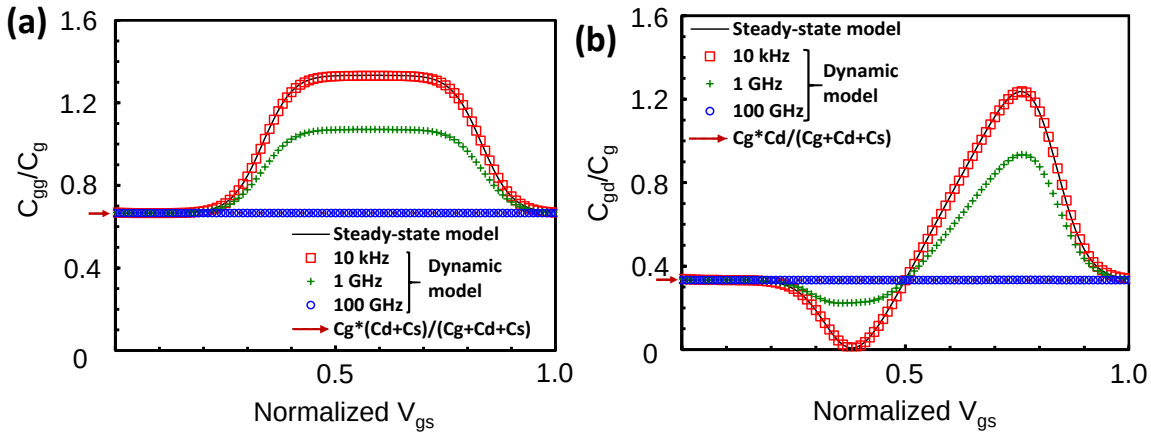


Fig. 2.12: (a) SET input capacitance C_{gg} (b) drain-to-gate capacitance C_{gd} and (c) source-to-gate capacitance C_{gs} as a function of gate voltage V_{gs} at drain voltage V_{ds} = 0.534 mV [0.01] and temperature T= 15.5 K [0.05]



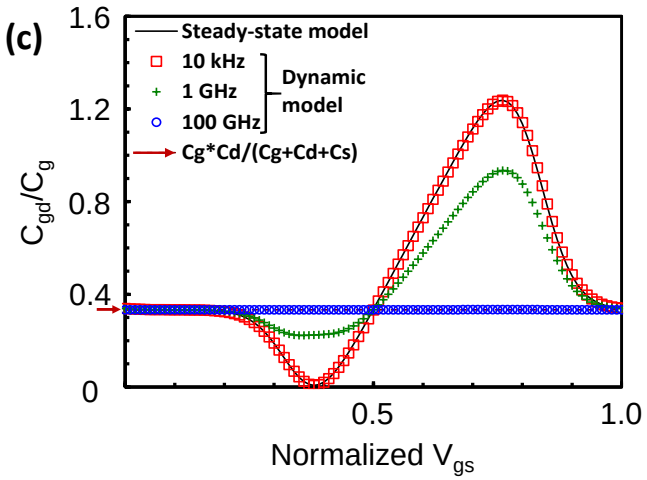


Fig. 2.13: (a) SET input capacitance C_{gg} (b) drain-to-gate capacitance C_{gd} and (c) source-to-gate capacitance C_{gs} as a function of gate voltage V_{gs} at drain voltage V_{ds} = 26.7 mV [0.5] and temperature T= 15.5 K [0.05]

The C_{gg} shows sharp peak at V_{gs}=0.5e/C_g, where Coulomb blockade is lifted. The peak C_{gd} and C_{gs} are almost equal to each other, and are a half of the peak C_{gg}, indicating that the gate is equally coupled to the drain and source at this low drain voltage.

At the cutoff frequency (1 GHz), the peak height is largely reduced, and levels off at 100 GHz due to the disappearance of the transistor action of the SET, i.e., the charge state of the Coulomb island cannot follow the rapid change of the signal. The baseline values of the C_{gg}, C_{gd}, and C_{gs} are C_g*(C_d+C_s)/C_Σ, C_g*C_d/C_Σ and C_g*C_s/C_Σ, respectively, which can be understood by considering the SET as a passive capacitance circuit consisting of C_g, C_d and C_s.

Figs. 12.13(a), (b) and (c) represent the C_{gg}, C_{gd}, and C_{gs}, respectively, as a function of gate voltage V_{gs} for a high drain voltage of $e/C_\Sigma/2$ at three

different frequencies. The proposed model at a low frequency (□) and the steady-state model (solid line) [18],[19] give the same result even at this large drain voltage.

The C_{gg} shows lower and wider plateau compared to the case with the low drain voltage [Fig. 12.12(a)] reflecting the gentler change in the island charge with respect to V_{gs}, and wider V_{gs} area where the Coulomb blockade is lifted. In view of the behavior of the C_{gd} and C_{gs}, it is found that the gate is strongly coupled to the source at low V_{gs}'s, and to the drain at high V_{gs}'s due to the large asymmetry in applied voltages to the source and the drain.

When the frequency is increased to the cutoff frequency (1 GHz), the capacitances come close to the baselines, and level off at 100 GHz due to the loss of the transistor action. The baseline values of the capacitances are the same as those for the low drain voltage (Fig. 12.12), and can be also explained based on the passive capacitance circuit

b) Phase change

Fig. 2.14 (a) and (b) shows the phase of the gate current with respect to the applied sinusoidal voltage in the circuit for C_{gg} evaluation [Fig. 2.11(a)] as a function of gate bias voltage for low and high drain voltages of $e/C_{\Sigma}/100$ and $e/C_{\Sigma}/2$, respectively at three different frequencies. It can be seen that at the low frequency of 10 kHz and high frequency of 100 GHz phase change is ~ -90 degree, indicating that the gate input impedance is purely capacitive and

there is no power dissipation. However, at the cutoff frequency of 1 GHz large phase change has been observed for both drain voltages. Such large phase change is indicating that there is power dissipation/energy loss at around the cutoff frequency.

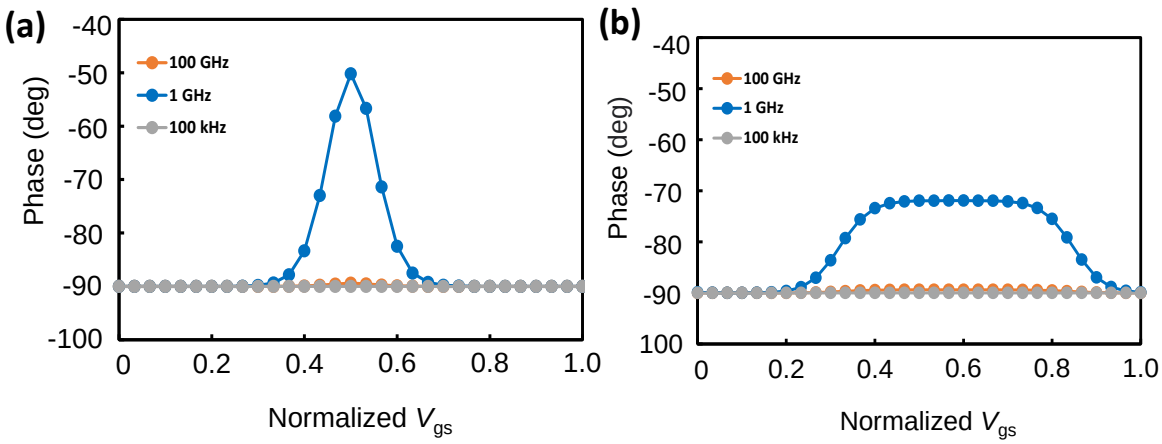


Fig. 2.14: Phase of the gate current with respect to the applied sinusoidal voltage in the circuit for C_{gg} evaluation [Fig. 2.11(a)] as a function of normalized gate voltage at drain voltages (a) V_{ds} = 0.534 mV [0.01] and (b) 26.7 mV [0.5] and temperature T= 15.5 K [0.05].

c) Frequency dependence of capacitances

Fig. 2.15 shows the gate input capacitance C_{gg} as a function of frequency at low and high drain voltages of $e/C_{\Sigma}/100$ and $e/C_{\Sigma}/2$, respectively. It can be seen that the C_{gg} starts to decrease at a frequency about an order of magnitude lower than the cutoff frequency (1 GHz), and approaches the dashed line at higher frequencies, which can be explained again as the approach to the condition of passive capacitance circuit consisting of C_g, C_d

and C_s. From such an analysis, we can quantitatively understand the frequency-dependent behaviors of the capacitances inside the SET.

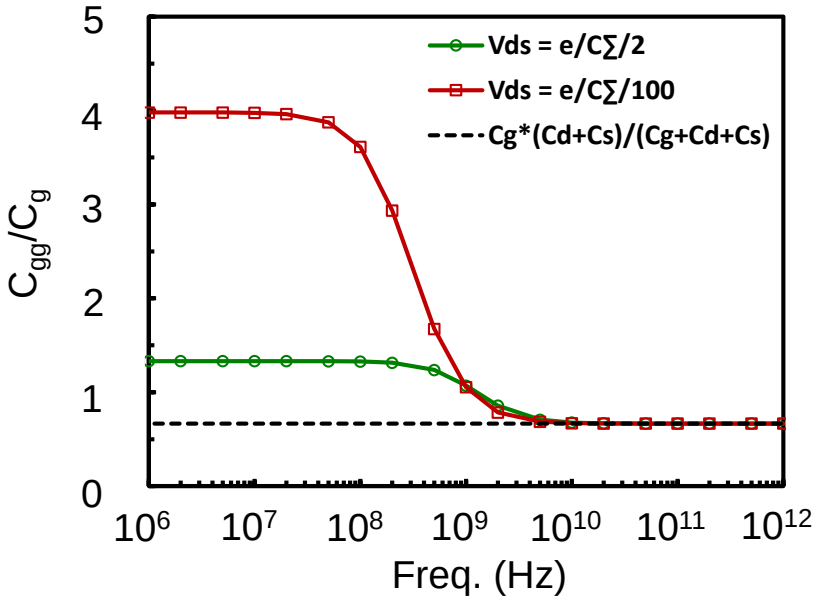


Fig. 2.15: Gate input capacitance C_{gg} as a function of frequency at drain voltage V_{ds} = 0.534 mV [0.01] and 26.7 mV [0.5], gate voltage V_{gs} = 80.1 mV [0.5] and 93.5 mV [0.6] and temperature T= 15.5 K [0.05].

d) Temperature dependence of capacitances

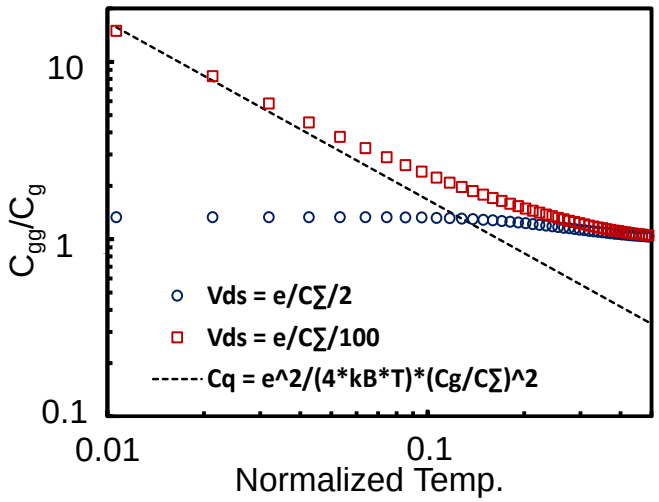


Fig. 2.16: Gate input capacitance C_{gg} as a function of temperature at drain voltage V_{ds} = 0.534 mV [0.01] and 26.7 mV [0.5], gate voltage V_{gs} = 80.1 mV [0.5] and 93.5 mV [0.6] and temperature T = 15.5 K [0.05]

Figure 2.16 shows the gate input capacitance C_{gg} as a function of temperature at low and high drain voltages of $e/C_{\Sigma}/100$ and $e/C_{\Sigma}/2$, respectively. The simulation is performed up to the temperature of 155 K [0.5] because the proposed model is accurate up to this temperature as was previously discussed.

For a small V_{ds}, C_{gg} increases as the temperature decreases almost inversely proportional to the temperature as predicted by the quantum capacitance C_q (dashed line) [12]. This is due to the steeper change of the island charge with respect to the V_{gs} at lower temperatures.

For a large V_{ds}, the change of the island charge is gentle due to the wider transition region between n=0 and 1, and thus the C_{gg} is small and insensitive to the temperature.

At higher temperatures, the C_{gg} assumes the common and nearly constant value as the Coulomb blockade is lifted, and the proposed model can describe the behavior up to the normalized temperature of 0.5 in contrast to the simplified equation of C_q

2.4.2 SET as a voltage amplifier simulation

Fig. 2.17(a) shows the circuit diagram of the SET-based inverting amplifier with a constant-current load, and Fig. 2.17(b) describes the operation point in the Coulomb diamond plot. The operation point is set at the

center of the descending side in the input-output (V_{ds}-V_{gs}) characteristics for the I_d = ±26.7 pA [=(V_{ds}/4R_t)/10 with V_{ds} = e/C_Σ/2].

To evaluate the frequency response of the amplifier, small sinusoidal fluctuation with amplitude ΔV_{gs} (=e/C_g/1000) is added to the gate bias V_{gs}, and the fluctuation in V_{out} is observed by the simulation.

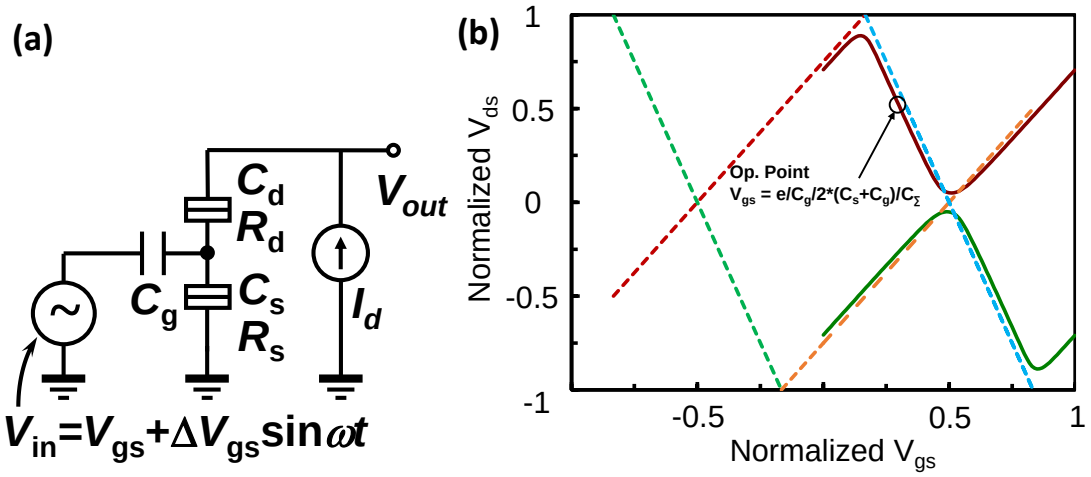


Fig. 2.17: (a) Circuit representation of SET as a voltage amplifier and (b) Corresponding operation point in V_{ds}-V_{gs} graph at drain voltage I_d = ±26.7 pA.

Fig. 2.18 depicts the frequency response of the SET-based amplifier. At low frequencies, the voltage gain close to the slope of the descending side of the Coulomb diamond (=C_g/C_d) is obtained, and the phase is inverted. At high frequencies, the transistor action is lifted, the gain becomes that of passive capacitive divider consisting of the C_g and C_s, and the output is in phase with the input. Interestingly, the gain and phase start to change at higher frequency compared to the case in Fig. 2.15 probably due to the high-impedance condition at the output terminal.

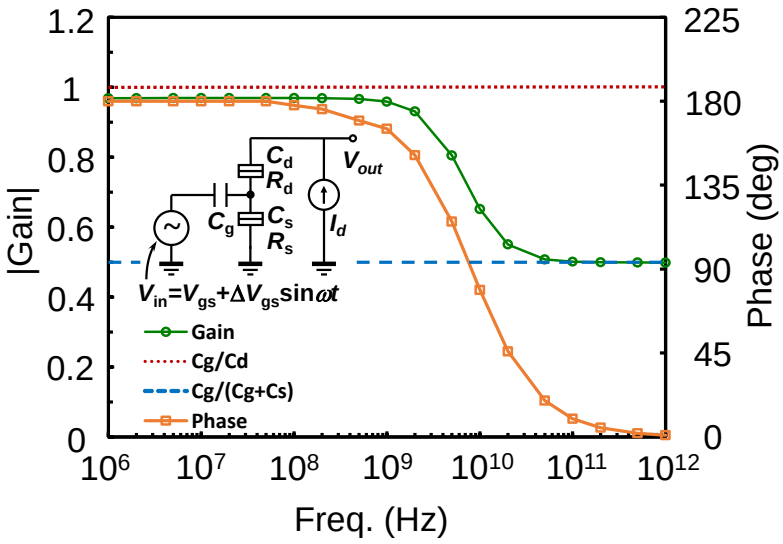


Fig. 2.18: Frequency response of SET inverting amplifier operating at drain current I_d = 26.4 pA, gate voltage V_{gs} = 53.4 mV (center of the descending side of the Coulomb diamond) and temperature T = 15.5 K [0.05].in SET.

The input capacitance C_{gg} is also simulated as a function of the gate voltage V_{gs} at three different frequencies and shown in Fig. 2.19. As can be seen in the figure at the low frequency (10 kHz), the C_{gg} shows a high peak at V_{gs}=0.5e/C_g due to the small V_{ds} and resultant abrupt change in the island charge. At the cutoff frequency (1 GHz), the peak height is reduced largely, and at the high frequency (100 GHz), the C_{gg} levels off to the baseline value that corresponds to the series connection of C_g and C_s as shown in the expression in the legend. Such behavior again verifies that the SET behaves like a passive circuit of capacitors at high frequencies.

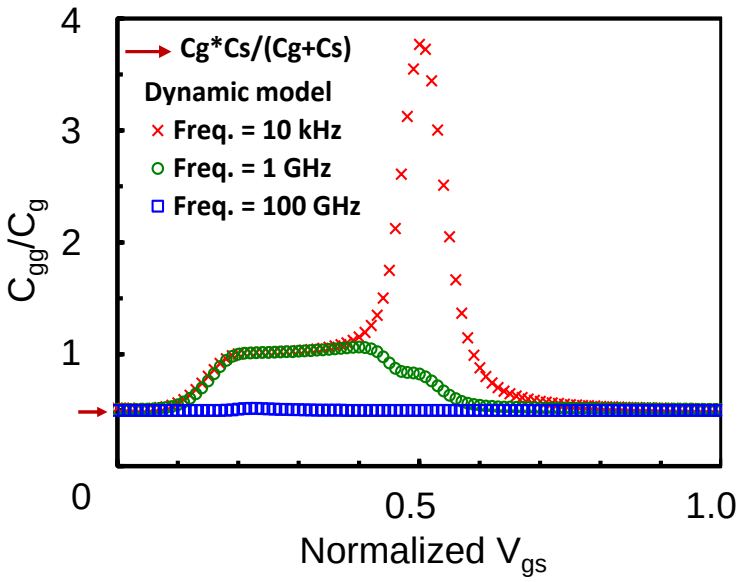


Fig. 2.19: SET input capacitance C_{gg} as a function of gate voltage V_{gs} at drain current I_d = 26.7 pA and temperature T= 15.5 K [0.05]

Another interesting finding in Fig. 2.19 is that the Miller effect [11] is not conspicuous in the SET-based amplifier as the C_{gg} at the operation point (V_{gs}=0.33e/C_g) is almost the same as that in Fig. 4(a) because the feedback capacitance C_{gd} is negligibly small as shown in Fig. 4(b), suggesting that it is only necessary to take care of the parasitic capacitance when we discuss the Miller effect in the SET-based amplifier.

This behavior can also be explained based on Fig. 2.20. As we can see from the graph at the operation point (V_{gs}=0.33e/C_g) C_{gg} value of SET based amplifier is almost the same as C_{gg} value of SET circuit with constant drain voltage at the lower frequency side. We as well have quantitatively analyzed the C_{gg} value at low frequency of 1kHz in Table 3.

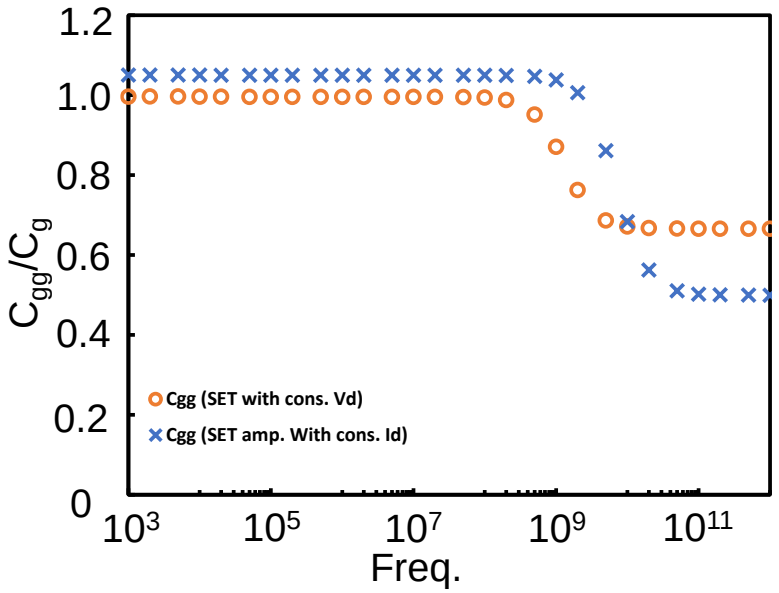


Fig. 2.20: SET input capacitance C_{gg} as a function of frequency at gate voltage V_{gs} = 53.4 mV and temperature T= 15.5 K [0.05]

Table 3: Gate capacitance at freq. 1 kHz and gate voltage V_{gs}=0.33e/C_g

SET with constant drain voltage	SET based amplifier
$C_{gd}/C_g = 0.086$	C_{gg}/C_g (Simulated) = 1.050
$C_{gs}/C_g = 0.910$	|Gain| (A) = 0.970
$C_{gg}/C_g = (C_{gd} + C_{gs})/C_g$ = 0.996	$*C_{gg}/C_g = \{(1+A)C_{gd} + C_{gs}\}/C_g$ = 1.079

As we can see from Table 3, C_{gg} value of SET based amplifier is larger than that of C_{gg} value of SET with constant drain voltage. This small increment in the C_{gg} value can be roughly explained with the help of Miller Effect where feedback capacitance C_{gd} gets multiplied with the Miller multiplication factor (1+A) resulting in the overall increment of $*C_{gg}$. However, since this

increment is not so high, we can say that Miller effect is not conspicuous in the SET-based amplifier as long as the intrinsic capacitance is concerned.

We have focused on the intrinsic SET characteristics so far. In reality, lead lines connected to the terminals are always accompanied with parasitic components such as capacitance, inductance, resistance, etc. As an example of real circuit, an inverting amplifier with a load capacitance C_L is analyzed (Fig. 2.21). Actually, each terminal of SET should be connected to a constant-voltage source or a capacitor sufficiently larger than C_Σ so that the SET can be regarded as an independent circuit element [18, 19], and this time the C_L is set to 30 aF (=10C_Σ). As a consequence, the cutoff frequency $f_{C\text{-}CL}$ of 53.1 MHz (= $1/(4\pi R_\Sigma C_L)$) consisting of SET output resistance and C_L dominates the low-frequency part of the frequency response.

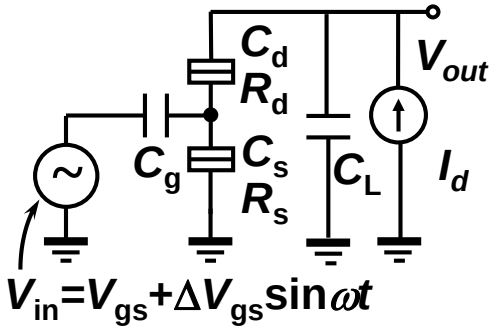


Fig. 2.21: Circuit diagram of the SET-based inverting amplifier with constant-current load and load capacitance C_L

Figure 2.22 compares the frequency responses of SET-based amplifier with a load capacitor, simulated by the proposed transient model and the steady-state model [18,19]. From both curves we can see that at low

frequencies voltage gain is equal to the slope of the descending side of CD, and the phase is inverted. The gain starts to decrease at around $f_{C\text{-}CL}$ and continues to decrease in proportional to $1/f$, but further drop is observed by the transient model at around f_C where transistor action is lifted. Such a drop cannot be described by the steady-state model because the model itself is frequency-independent. The phase starts to decrease at around $f_{C\text{-}CL}$ and becomes saturated at 90 deg in case of the steady-state model, but it continues to decrease in the case of the transient model, and finally gets saturated at -90 deg reflecting the transition from inverting to non-inverting operations at high frequencies above the f_C as observed in Fig. 2.18, which also cannot be expressed by the steady-state model. These results clearly demonstrate the importance of the proposed transient model in accurately describing the high-frequency behavior of the real circuits.

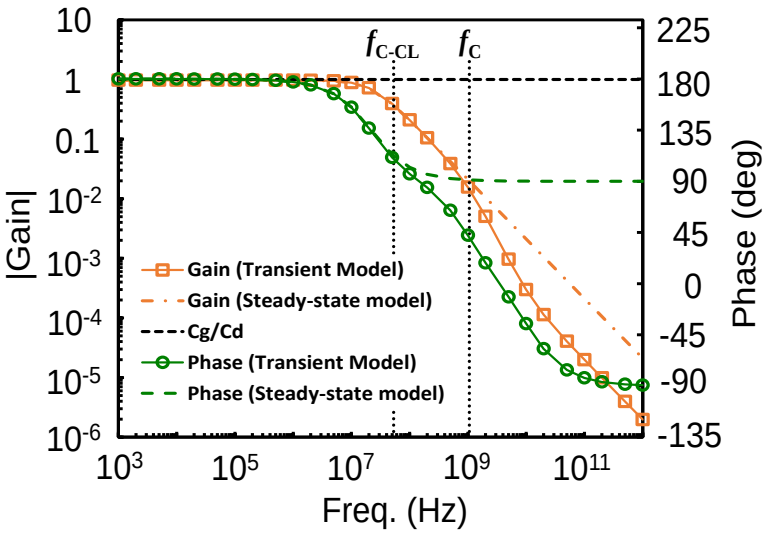


Fig. 2.22: Frequency response of the SET inverting amplifier with a load capacitor C_L=30 aF ($10C_\Sigma$) operating at a drain current I_d = 26.4 pA, gate voltage V_{gs} = 53.4 mV [0.33] (center of the descending side of the CD) and T = 15.5 K [0.05].

Note that the relatively low $f_{C\text{-}CL}$ and f_C could be increased by three orders of magnitude at the highest by decreasing the tunneling resistance to the level of the resistance quantum [38]. There is also a room for decreasing the capacitance parameters by size reduction to increase the cutoff frequencies.

We as well discussed the Miller effect [11] in the SET based amplifier with load capacitance at low frequency of 1 kHz. As we can see from Table 4, same as the C_{gg} value of SET based amplifier in Table 3, C_{gg} value of SET based amplifier with load capacitance is larger than that of C_{gg} value of SET with constant drain voltage.

Table 4: Gate capacitance at freq. 1 kHz and gate voltage $V_{gs}=0.33e/C_g$

SET with constant drain voltage	SET based amplifier with load capacitance
$C_{gd}/C_g = 0.086$	C_{gg}/C_g (Simulated) = 1.050
$C_{gs}/C_g = 0.910$	|Gain| (A) = 0.970
$C_{gg}/C_g = (C_{gd} + C_{gs})/C_g$ = 0.996	$^{**}C_{gg}/C_g = \{(1+A)\ C_{gd} + C_{gs}\}/C_g$ = 1.079

This small increment in the C_{gg} value as well can be roughly explained with the help of Miller effect where feedback capacitance C_{gd} gets multiplied with the Miller multiplication factor (1+A) resulting in the overall increment of $^{**}C_{gg}$. However, since this increment is not so high, we can say that Miller

effect is not conspicuous in the SET-based amplifier with load capacitance as well.

Summary

In this chapter mainly simulation results of dynamic high-frequency behavior of SET are discussed.

Initially the time dependent master equation (TDME) has been discussed and by solving the TDME equation dynamic SET model has been proposed.

Using this model high-frequency rectifying behavior of SET has been simulated and it has been observed that rectifying current has a finite value up to 1 THz and beyond. Theoretical explanation has been attempted for such behavior and it has been concluded via simulation results that the asymmetry in the tunneling rate with respect to the drain voltage is responsible for the rectifying operation of SETs at high frequencies.

Such finding suggests that SET can become an important rectifier at ultrahigh frequencies where conventional devices cannot operate.

In the second part of simulation intrinsic terminal capacitances and transcapacitances in the SET has been discussed as a function of gate voltage, frequency, and temperature. Based on the simulation results it is concluded that, at low frequencies, the capacitances depended on the biasing but, at high

frequencies, the transistor action of the SET is lifted, and it acted as a passive capacitance circuit. Such a transition from the low-frequency to high-frequency characteristics of the SET could be described quantitatively by the proposed model. Also, the model could analyze the behavior of the SET covering a wide range of temperature, in which the C_{gg} for small V_{ds} was inversely proportional to the temperature on the low-temperature side, and the C_{gg} assumed the constant value insensitive to the temperature or V_{ds} on the high-temperature side.

In addition, the frequency response of the SET-based amplifier was investigated. The transformation from inverting amplifier at low frequencies to the capacitive divider/non inverting operation at high frequencies was successfully described. It was also found that the Miller effect is not conspicuous in the SET-based amplifier due to the negligible feedback capacitance at the operation point.

From these results, we can expect that the proposed model can be widely used to analyze the circuits including SETs for high-frequency amplification, oscillation, detection, qubits readout by gate-based sensing, and so on.

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Chapter 3

EXPERIMENTAL ASPECT OF HIGH FREQUENCY RESPONSE OF VARIOUS SETs.

It is previously proposed (in chapter 2, section 2.3) through simulation that SET can become an important high frequency (HF) rectifier where conventional rectifiers can't operate. However, experimental verification for such claim is required. For the verification we have performed high frequency characterization on two different types of SETs: SET fabricated by PADOX method and heavily doped silicon nanowire-based SET. Details of which are shared in this chapter.

3.1 SET fabricated by PADOX method

Initially I characterized SET fabricated by pattern-dependent oxidation (PADOX) method (Fig. 3.1). In this method a short Si nanowire converts into small Si island with tunnel barriers on both sides of the island[1], [2], [3], [4]. SET fabricated with this method has many advantages like large temperature operation [2], tunable tunnel barrier [5] and high stability [3] which are desirable for high frequency operation.

This SET is fabricated at NTT and can be classified into 4 categories depending on different dimensions and layouts:

1) SET with SOI thickness 248 to 258 Å
2) SET with SOI thickness 283 to 293 Å

3) SET with lower and upper gate (UG)

4) SET without lower gate (LG)

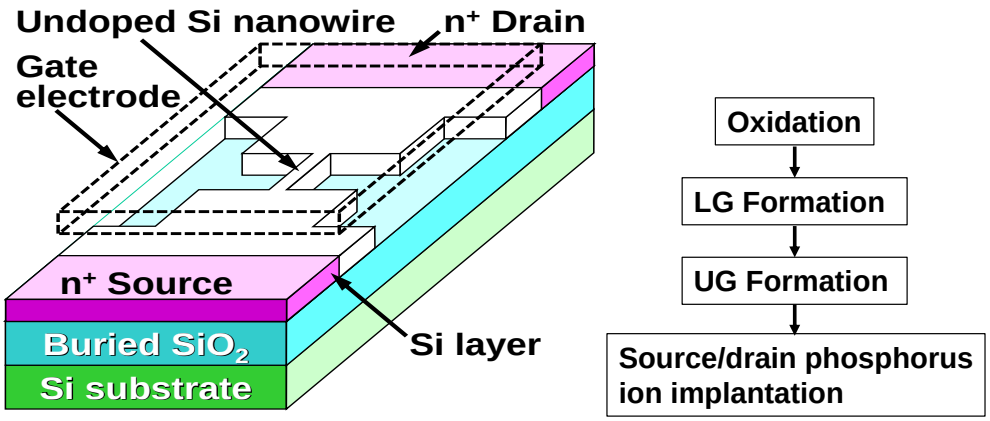


Fig. 3.1: Silicon SET fabricated by PADOX method along with fabrication steps

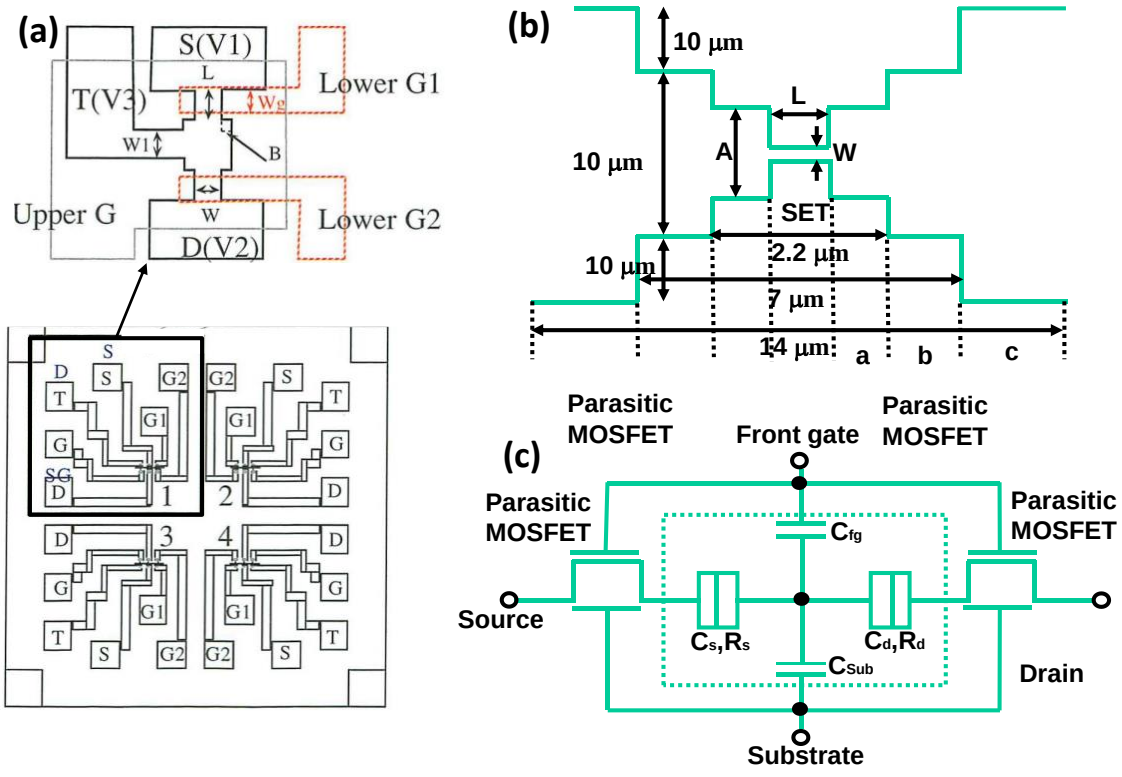
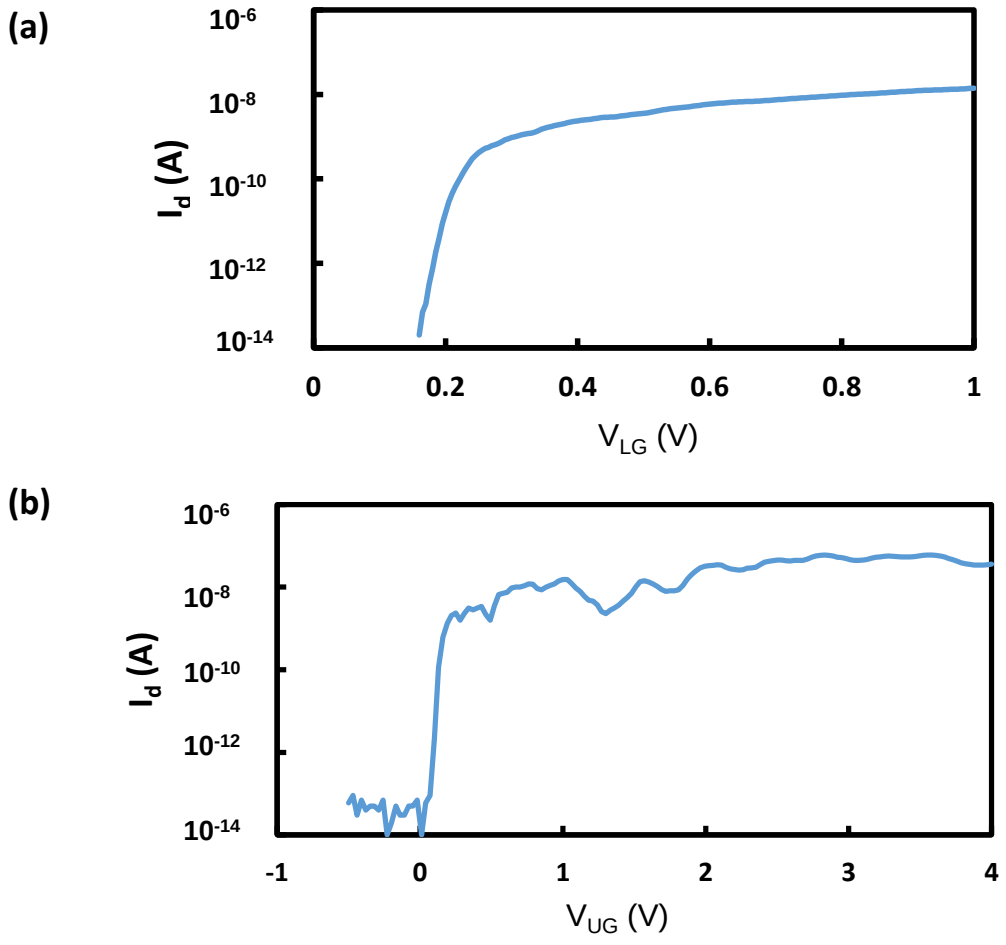


Fig. 3.2: (a) Layout of silicon SET fabricated by PADOX method

(b) schematic of Si SET (c) equivalent circuit

The impurity used in SOI layer is phosphorous and doping concentration in n^+ source/drain and gate polysilicon (not the wire) is phosphorous > $1x10^{20}$ cm^{-3}. Layout, schematic, and equivalent circuit diagram of the SET device is shown in Figure 3.2 (a), (b) and (c) respectively. Length of the devices are either 50, 70 or 100 nm and width 30, 36, 40, 44 & 50 nm.

We initially performed DC characterization on all the devices to see the Coulomb oscillation characteristics of the devices at temperature 20 K, drain voltage 5 mV and substrate voltage 0. Shown in figure 3.3 is the I_d-V_{sub} characteristics of some devices.



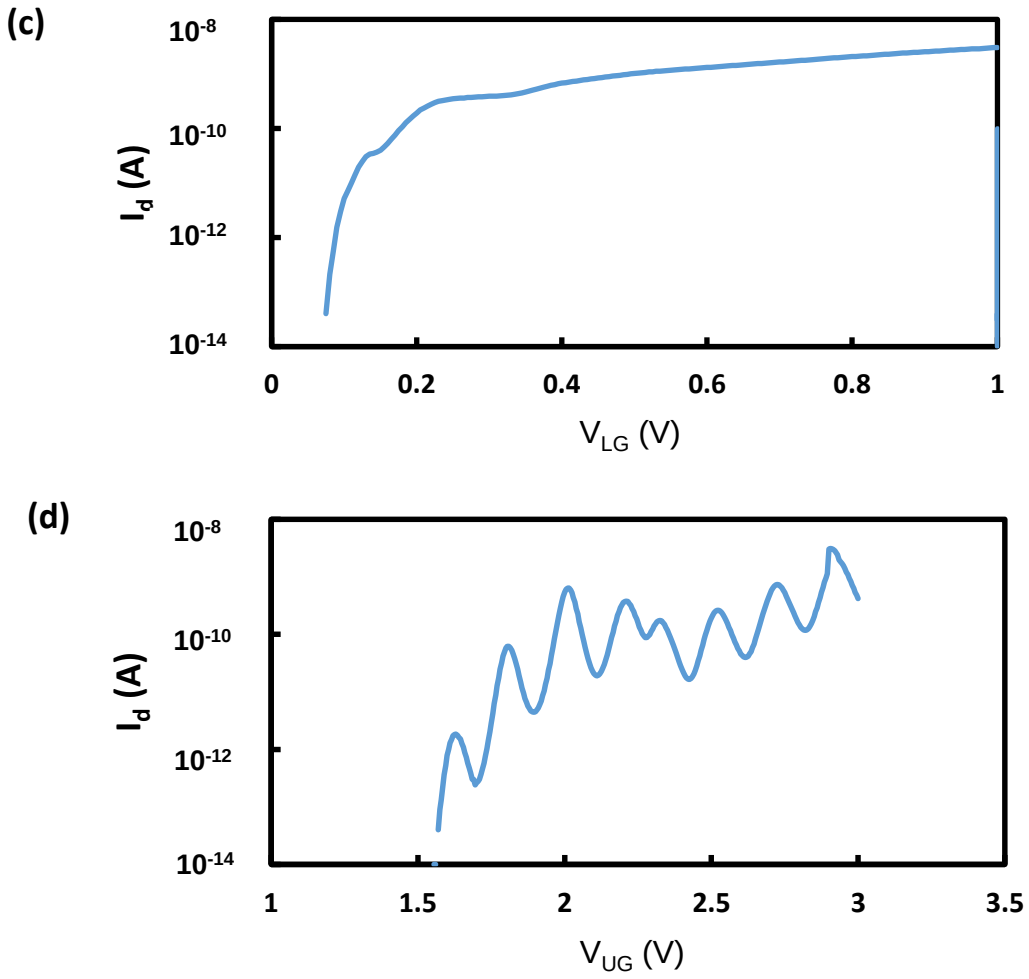


Fig. 3.3: I_d-V_g Characteristics of device type 1 (a) with lower and upper gate, L50 nm W50 nm (b) with only upper gate, L50 nm W 44 nm; device type 2 (c) with lower and upper gate L50 nm W 50 nm (d) with only upper gate: L50 nm W 44 nm

From the obtained characteristics we can see that the Coulomb oscillation is not prominent in most of the cases. Through further optimization in the measurement condition, we may be able to see the Coulomb oscillation in remaining devices. For example, during this measurement effect of substrate voltage and temperature was not considered. Since the thickness of buried oxide is 400 nm the maximum applicable substrate voltage is limited

to 400 Volt (10 mV/cm). Also, temperature can be further decreased to 10 K (limit of the measurement system).

However, high-frequency characterization of this device has an issue of parasitic MOSFET. In case of PADOX devices the sheet resistance is modulated by the upper gate (Fig. 3.2 (a)) responsible for transistor action of parasitic MOSFET. Parasitic MOSFET formed on both side of the SET [3] may fatally affect the device characteristics. To judge the effect of parasitic component we may have to extract its cutoff frequency and devices cutoff frequency to see the influence of parasitic components.

To address this issue cutoff frequency of parasitic MOSFET was simulated using the distributed CR circuit (Fig. 3.4).

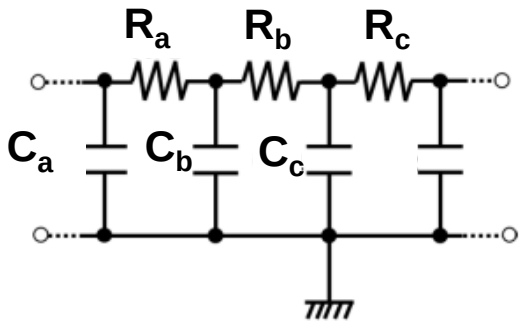


Fig. 3.4: Distributed CR filter model to calculate the frequency response of the parasitic component (lead). Note that each section *a*, *b* or *c* is further divided into 10 subsections to properly simulate the distributed circuit characteristics [8].

Based on the geometry of the device (Fig. 3.2 (b)) capacitance and resistance value of the plate areas are calculated using the following formula:

$$C_{MOSFET} = \frac{\varepsilon k A}{d} \quad \ldots. (1)$$

Where, ε is the permittivity of space, 8.854×10-12, k is permittivity of SiO_2, 3.9, d is thickness of buried oxide and A is area of SOI (a, b, c)

$$R_{MOSFET} = \frac{X}{Y} \times R_{Sheet} \quad \ldots(2)$$

Where, X is length and Y is width of the SOI layer and R_{sheet} is sheet resistance of the device.

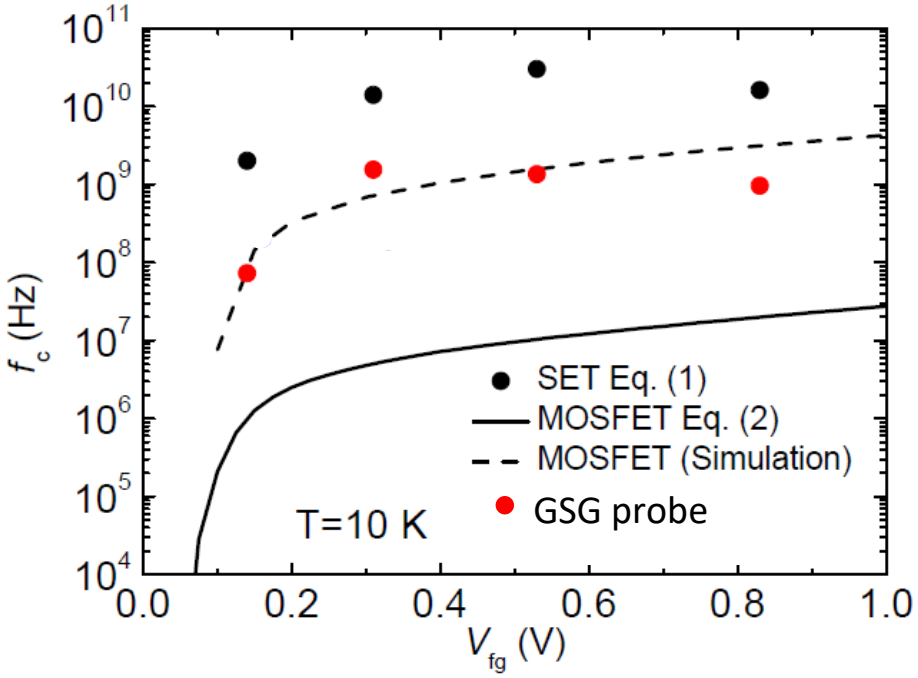


Fig. 3.5: Cutoff frequency of SET and parasitic MOSFETs [6], [7], [8]

Through simulation cutoff frequency of ~100 MHz was obtained for MOSFET devices which seems to be on the lower frequency side (Fig. 3.5). Also, if the cutoff frequency of parasitic component is lower than the cutoff frequency of SET it is difficult to evaluate the intrinsic transistor properties. As a result it is concluded that SET fabricated by PADOX method is not

suitable for high frequency measurement due to low cutoff frequency of parasitic MOSFET of the SET [6], [7], [8].

Consequently, heavily doped Si nanowire SETs fabricated by Shizuoka University (SU) and Hiroshima University (HU) are selected for high-frequency measurement. Unlike the case with PADOX device, external lead of these types of devices is heavily doped and has lower and fixed sheet resistance. Specification of both the devices are listed in Table 1 and 2 respectively:

Table 1: Heavily doped SET Fabricated at Shizuoka University

Parameters	Values
Dopant Concentration	3.5×10^{19} cm^{-3} (Phosphorus)
Sheet Resistance	883.5 Ω
SOI Thickness	23.7 nm
Pad Area	30 X 22 μm
BOX Thickness	400 nm

Table 2: Heavily doped SET Fabricated at Hiroshima University

Parameters	Values
Dopant Concentration	1.88 x 10^{19} to 2.08 x 10^{19} cm^{-3} (Arsenic)
Sheet Resistance	873.1 Ω to 932.6 Ω
SOI Thickness	37.8 nm
Pad Area	50 X 40 μm
Contact Resistance	6.84 X 10^{-04} to 3.99 X 10^{-04} Ωcm^2
BOX thickness	400 nm
Remarks	Multiple island structure

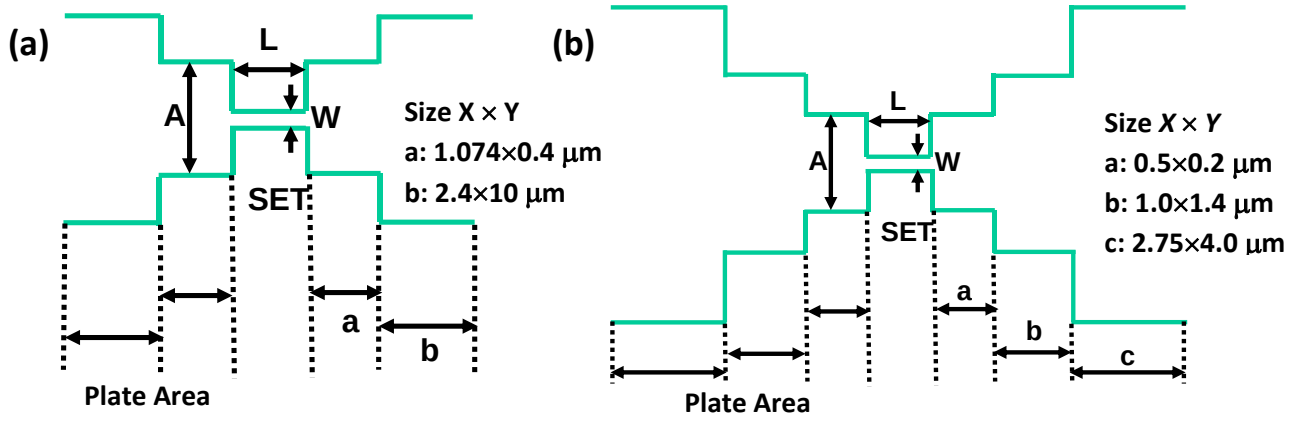
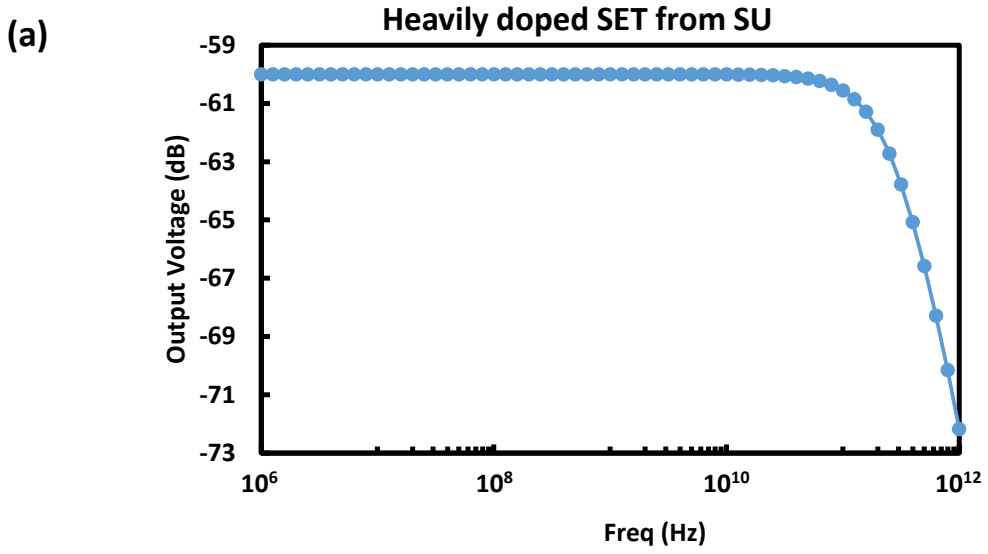


Fig. 3.6: Schematic diagram of heavily doped Si SETs channel (a) fabricated at SU (b) fabricated at HU. Note that each section *a*, *b* or *c* is further divided into 10 subsections to properly simulate the distributed circuit characteristics [8].

Initially, the cutoff frequency of the lead in both devices is simulated as a distributed CR circuit. Shown in Fig 3.6 is schematic diagram of Si SET for both devices and to evaluate the accurate cutoff frequency of the lead area that is divided into small sections *a*, *b* and *c* and further divided into 10 subsections each. These small sections are then converted into the distributed CR circuits for LTspice simulation (Fig. 3.4).



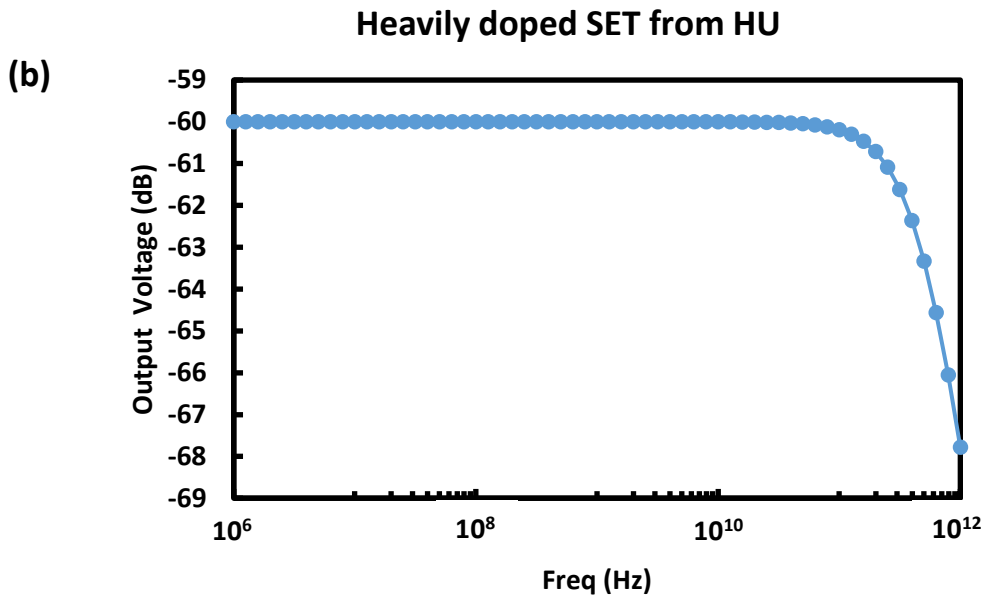


Fig. 3.7: Cutoff frequency of distributed CR filter of (a) Heavily doped SET from SU (b) Heavily doped SET from HU

Through simulation cutoff frequency of distributed CR circuit (Fig. 3.7) is evaluated and it is observed that cutoff frequency of CR distributed circuit is sufficiently high (~100 GHz). Hence, intrinsic transistor properties could be evaluated by using these devices without being affected by the parasitics.

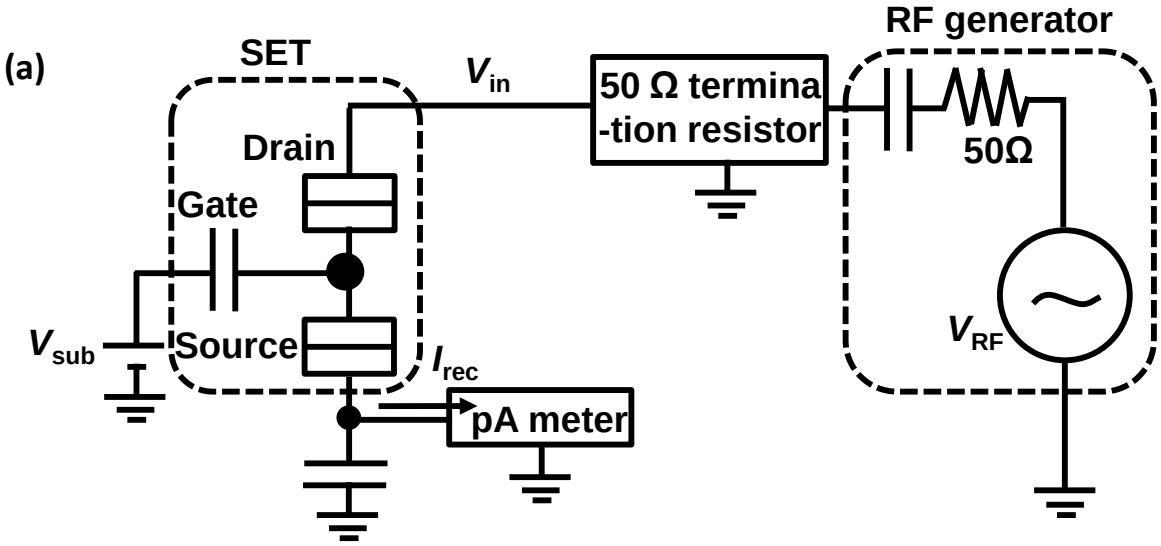
In the next section firstly optimization of the high-frequency measurement setup is discussed and then using the optimized measurement setup DC characterization and high frequency response of nanowire-based SET devices are presented.

3.2 Optimization of high frequency measurement setup

Optimization of the measurement system is performed with the help of heavily doped silicon nanowire-based SET having length 52 nm, width 92 nm and cutoff frequency 32.2 GHz.

Shown in Figure 3.8 (a) is the high frequency measurement setup that is used initially for high-frequency characterization of SET. The circuit consists of radio frequency (RF) generator (Agilent N5181A), 50 Ω termination resistor, a picoampere meter (Agilent 4156C) and a substrate voltage supply. RF generator is used to supply AC signal to the drain terminal of SET, picoampere meter is used to measure the rectified current (I_{rec}) through source terminal and 50 Ω termination resistor inserted in front of RF generator is used for ensuring DC return path of the rectified current.

Temperature is another important factor which may affect the overall performance of the SET device. Hence, we are using low-temperature prober (Nagase Techno-Engineering Grail 21-205-6-LV-R) for the measurement which is equipped with the temperature controller (cryogenic control system Inc Crycon 32) with an accuracy of ±0.2 K. The device temperature inside the ultralow temperature prober is controlled by the temperature controller.



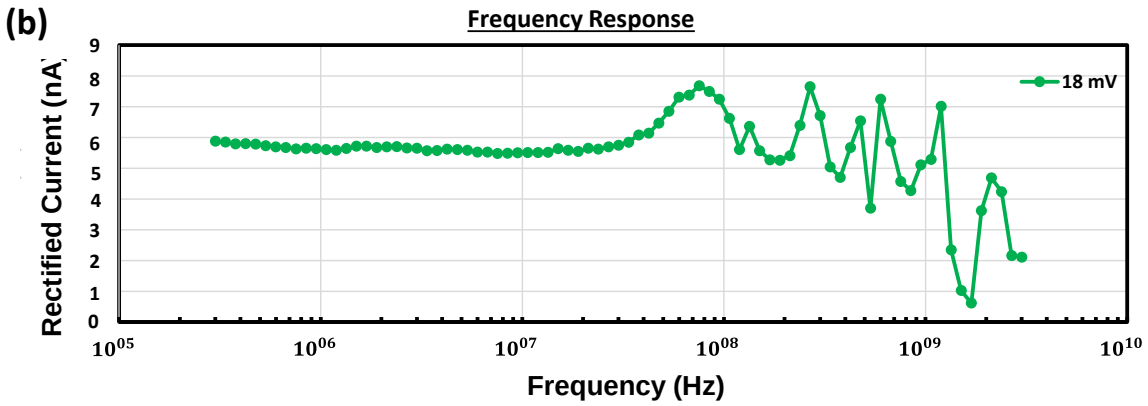


Fig. 3.8: (a) High-frequency measurement setup for rectifying current (b) frequency response of SU SET having L = 52 nm and W = 92 nm and RF signal amplitude 18 mV

Apart from it, multiple connectors (9 BNC), ordinary cables (RGS8-A/U) and standard probes is used in the setup.

Using this measurement setup high-frequency measurement was performed (discussed in section 3.3 and 3.4) and shown in Figure 3.8 (b) is the corresponding frequency response. As we can see from the figure flat frequency characteristics is achieved till 33 MHz and after that high fluctuation is observed.

Since the calculated cutoff frequency is around 32.2 GHz and flat frequency response is achieved only till 33 MHz, it is concluded that further optimization in the measurement system is required. Hence, measurement system is modified as shown in Fig. 3.9 (a) [9], [10].

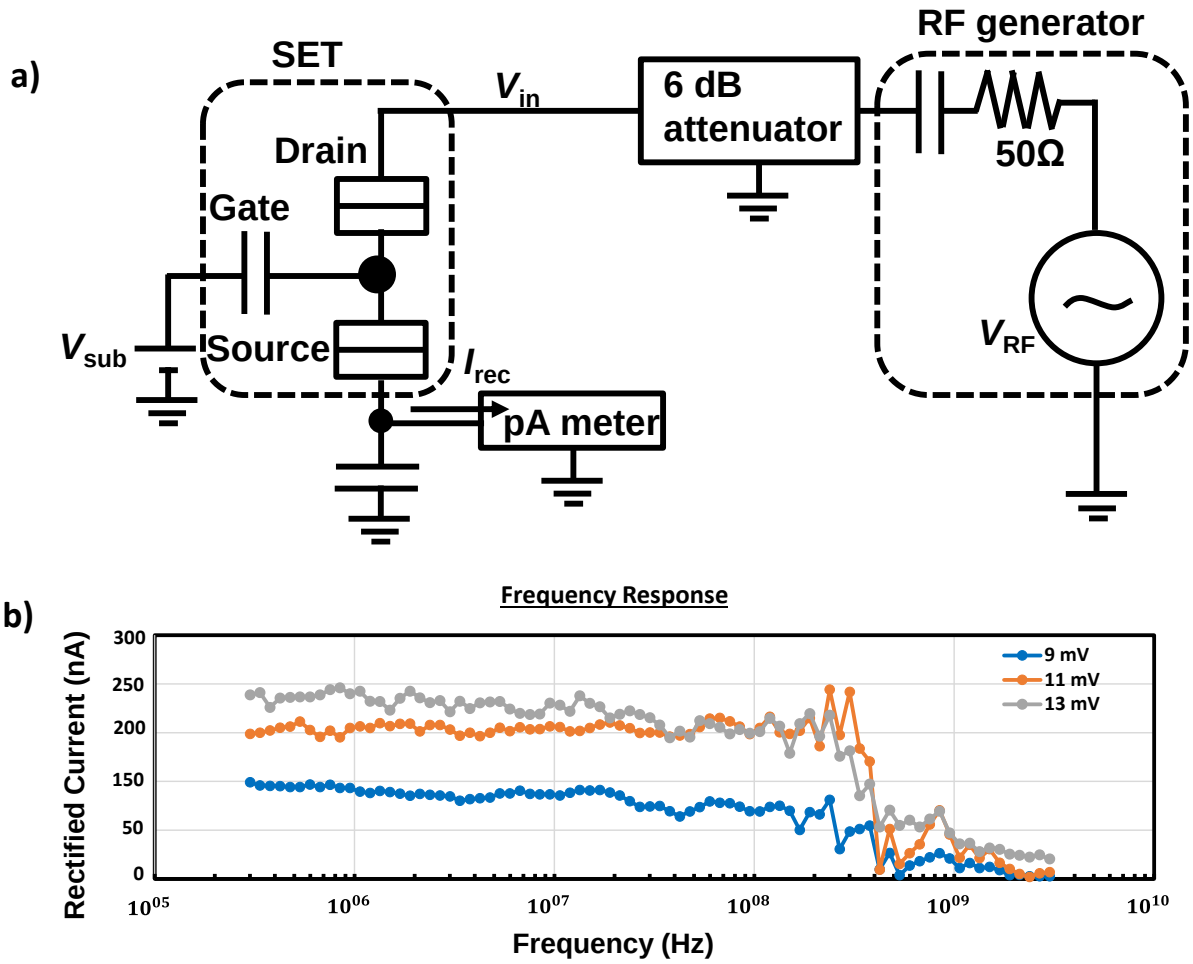


Fig. 3.9: (a) Modified high-frequency measurement setup for rectifying current (b) frequency response of SET having L = 52 nm and W = 92 nm and RF signal amplitude 9, 11 and 13 mV

The modified measurement system as well consists of radio frequency (RF) generator (Agilent N5181A), a picoampere meter (Agilent 4156C) and a substrate voltage supply. However, 50 Ω termination resistor inserted in front of RF generator is replaced with 6 dB attenuator. The number of connectors is reduced from 9 BNC to 3 SMA and 1 BNC and ordinary cable is replaced with high frequency cables (PE-SR405FLJ Coax) to avoid the

degradation of the signal integrity. Also, instead of using standard probes GSG probes is used for contacting SET terminals (Fig. 3.10), ensuring proper transmission of signals.

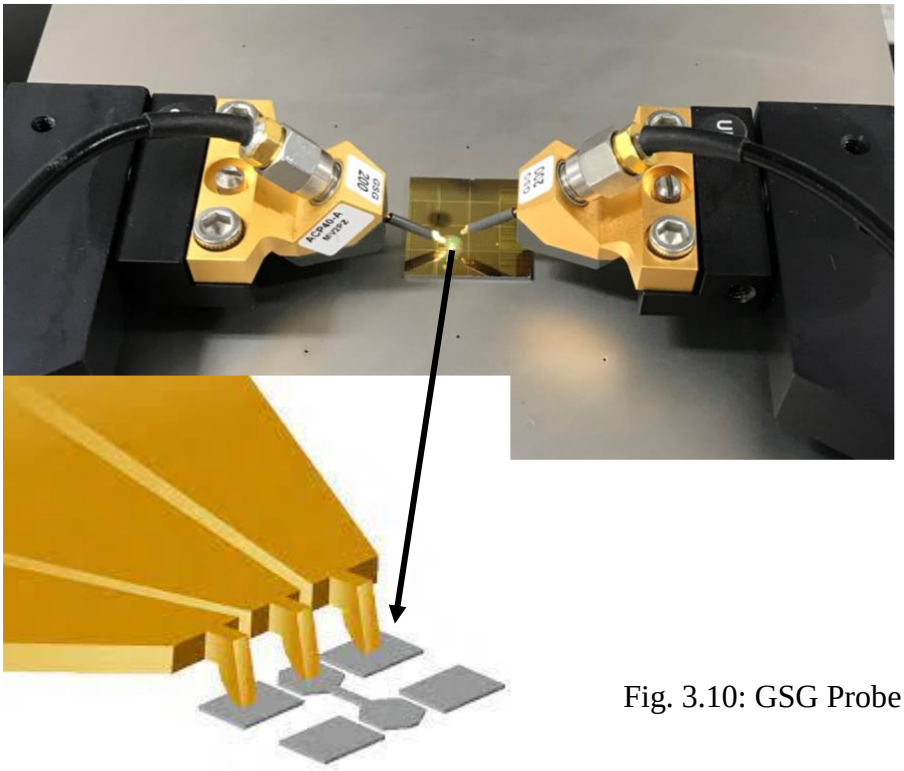


Fig. 3.10: GSG Probe

All the equipment involved in the measurement setup is calibrated and validated before high-frequency measurement is performed.

Using the modified measurement setup high frequency measurement is again performed on the same device and improved frequency response is achieved with flat frequency response till 200 MHz (Fig. 3.9 (b)).

In such a way optimization of the measurement setup is completed. Using this optimized measurement setup further high frequency characterization of SET is performed. Details are discussed in next section.

3.3 Heavily doped silicon nanowire-based SET

3.3.1 SET Fabricated at SU

To evaluate the HF characteristics of SET, we firstly evaluated heavily doped silicon nanowire-based SET fabricated at SU.

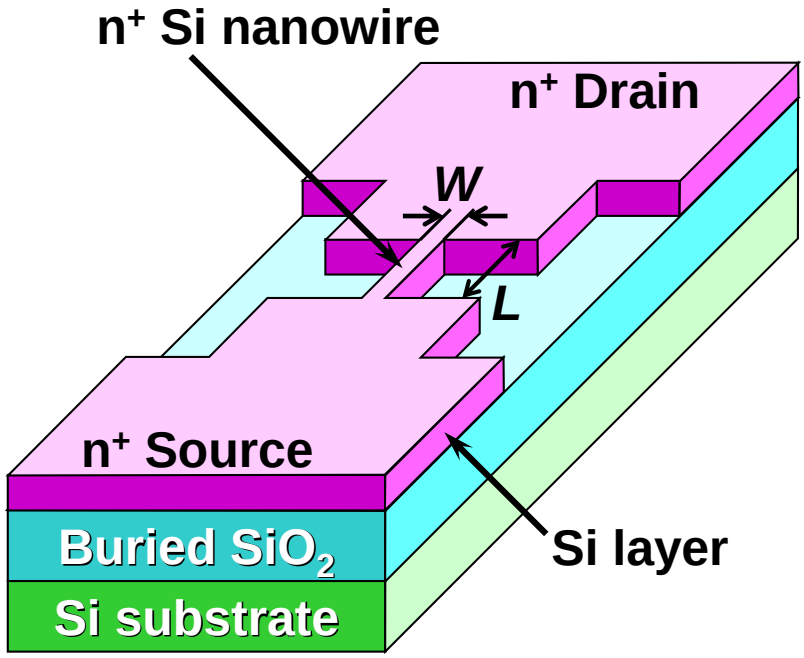


Fig. 3.11: Heavily doped silicon nanowire-based SET

In this type of SET highly doped SOI film is used and by lateral structuring SOI wire is formed (Fig. 3.11). In this kind of device quantum dot structure is formed naturally by the fluctuation of dopant. This fabrication approach has already been discussed in many scientific journals [11], [12], [13], [14].

We are particularly interested in this type of device as heavily doped devices have reduced series resistance which is important for accurately evaluating HF behavior of SET. The device that we are evaluating is in house fabricated, has bottom (substrate) gate and GSG pads specifically for HF measurement. Shown in Figure 3.12 is the device structure along with fabrication steps.

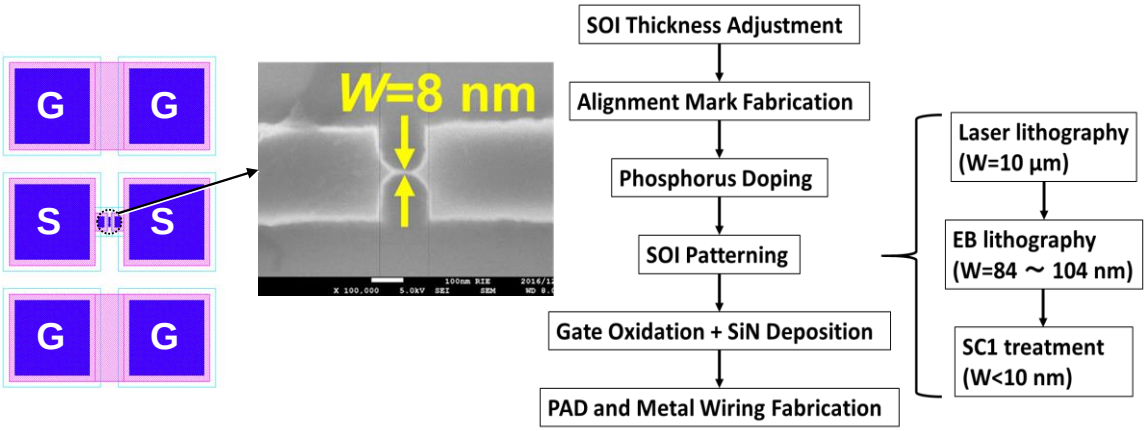


Fig. 3.12: Schematic of heavily doped silicon nanowire-based SET along with fabrication step

This device is heavily doped with phosphorus and the dopant concentration is 3.5×10^{19} cm^{-3}. Also, the SOI thickness in the large area is about 23.7 nm. Total there are 18 (x 4) types of SET devices with different dimension (Fig. 3.13):

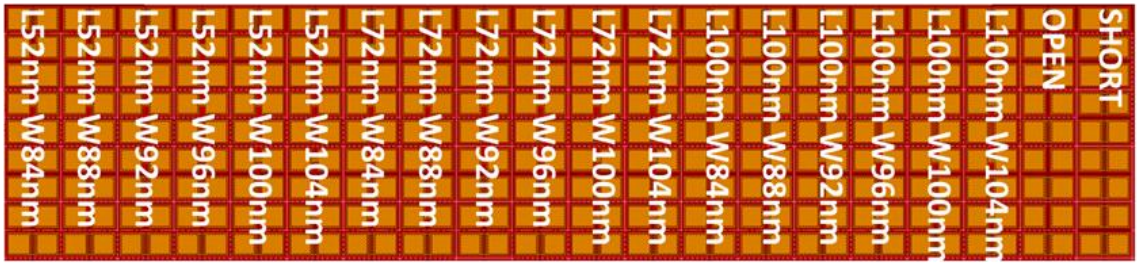


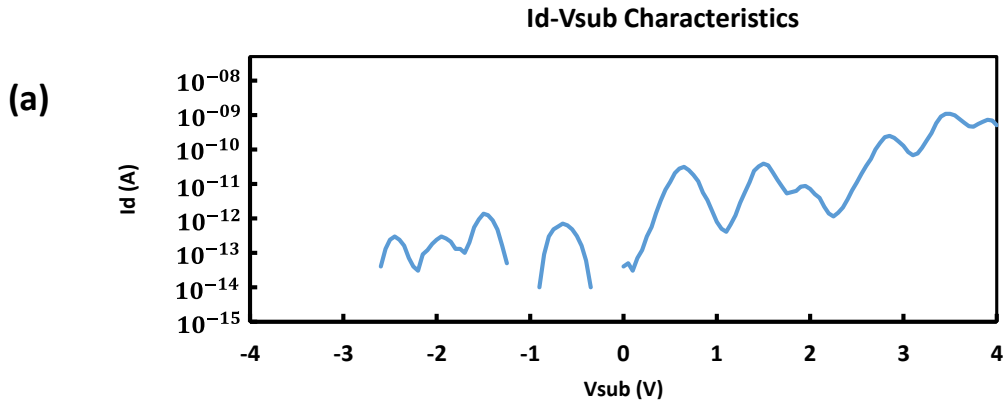
Fig. 3.13: Heavily doped silicon nanowire-based SET layout with different dimensions

We divided our experiment in two parts: in the first part we did the DC characterization of SET to confirm the presence of Coulomb blockade effect and in the second part of our experiment, we performed high frequency experiment.

DC characterization at temperature 20 K

DC characterization is performed on all the devices at 20 K temperature. To see the Coulomb oscillation characteristics (I_d-V_{sub}) substrate voltage V_{sub} is swept from -12 to 4 V at a fixed drain voltage V_d of 10 mV. 80% of the devices showed the oscillation. SET with dimension 52 nm length (L) and 92 nm width (W) is selected as a representative device because Coulomb oscillation is prominent in this device.

Shown in Figure 3.14 (a), (b) is the I_d-V_{sub} characteristics of the device along with V_d-V_{sub} characteristics at drain current I_d ±10 pA. Quasi-periodic oscillation can be observed from the Figure 3.14 (a). We also plotted stability diagram (Fig. 3.14 (c)) as a function of drain and substrate voltage at temperature 20 K, which supports the presence of Coulomb blockade effect.



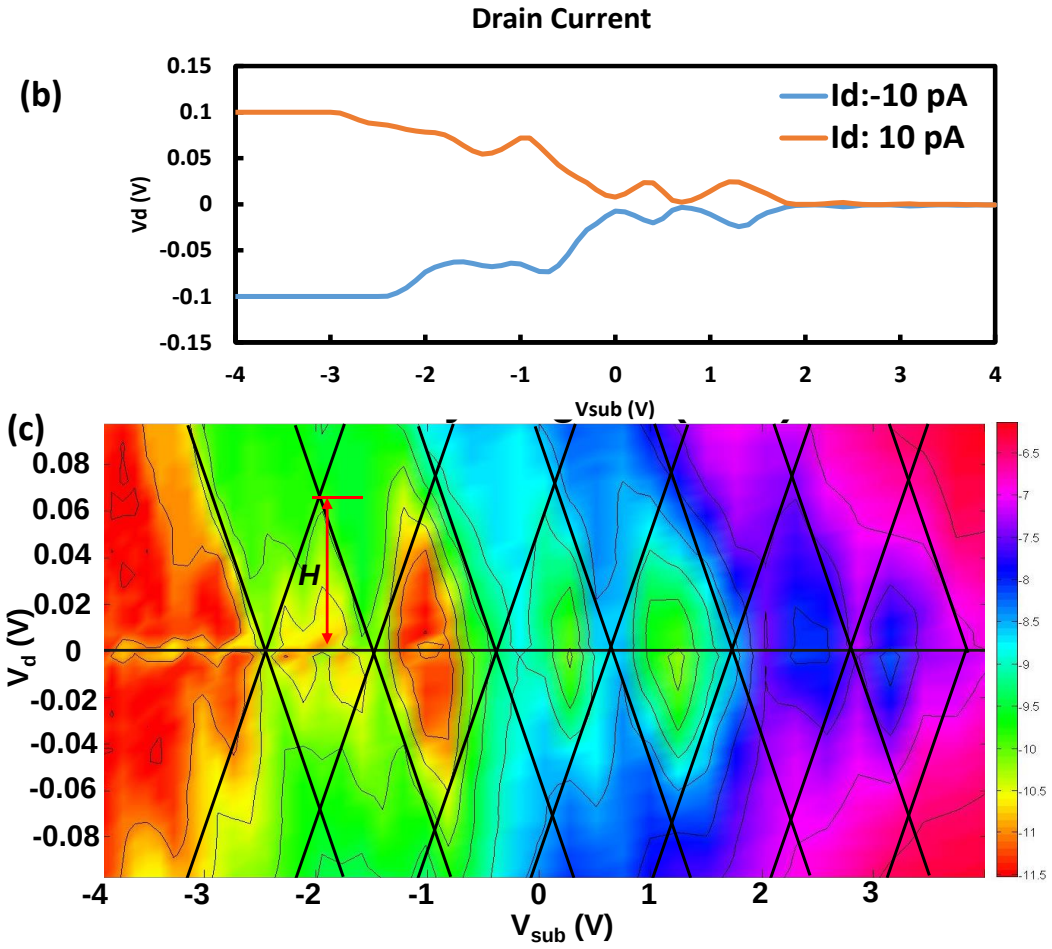


Fig. 3.14: (a) I_d-V_{sub} (b) V_d-V_{sub} and (c) Stability diagram of SET (L:52 ; W: 92 nm) at T = 20 K

We extracted several parameters from the stability diagram of the SET i.e., gate (C_g), drain (C_d) and source (C_s) capacitance, source (R_s)and drain (R_d) resistance, cut off frequency (f_c) and AC signal amplitude (A). Where capacitance values were extracted considering positive and negative slope of the diamond as $C_g/(C_g + C_s)$ and $-C_g/C_d$, Tunnel resistance ($R_t = R_s = R_d$) were extracted using the formula; peak $I_d = V_d/4R_t$, Cut off frequency was extracted

using formula; $f_c = 1/2\pi R_\Sigma C_\Sigma$ and finally, RF signal amplitude (RMS) for rectifying operation was extracted using formula A= $\frac{H}{4\sqrt{2}}$ where height of the diamond is $H = e/C_\Sigma$. All the extracted values corresponding to all the 6 diamonds are summarized in Table 3.

Table 3. List of extracted SET parameters

Diamond	V_{sub} [V]	C_g [aF]	C_S [aF]	C_d [aF]	$R_S=R_d$ [Ω]	f_c [Hz]	Height [V]	RF Amplitude (RMS) [mV]
1	-1.40	0.18	0.87	1.05	2.14×10^9	1.78×10^7	0.068	12.0
2	-0.05	0.15	1.00	1.15	1.51×10^8	2.30×10^8	0.076	13.4
3	0.70	0.15	1.07	1.21	5.39×10^7	6.08×10^8	0.072	12.7
4	2.05	0.15	0.81	0.96	6.77×10^6	6.14×10^9	0.076	13.4
5	2.85	0.16	1.36	1.52	4.34×10^6	6.05×10^9	0.074	13.0
6	4.00	0.15	0.87	1.01	1.17×10^6	3.37×10^{10}	0.072	12.7

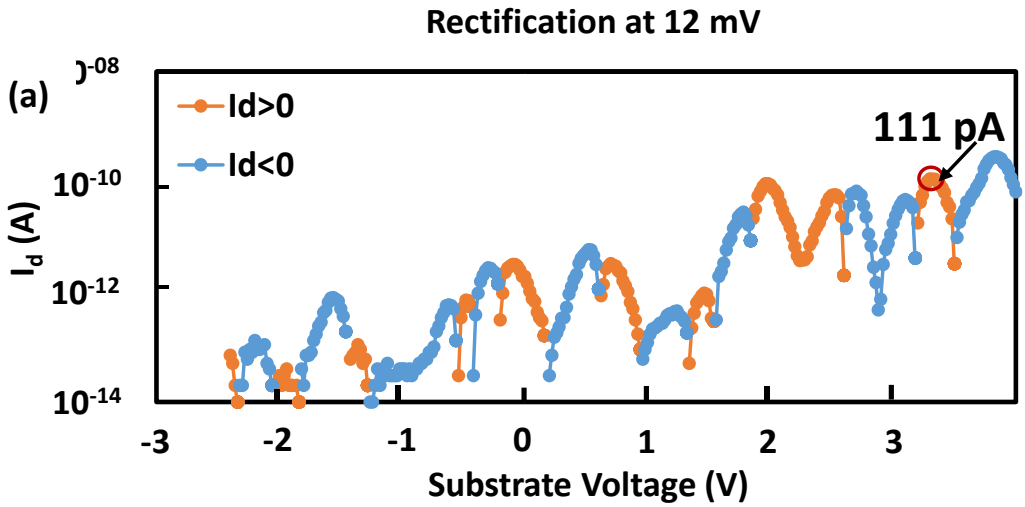
As we can see from the table the cut off frequency of the device is around ~6 GHz and lies between diamond 4 and 5. Also, we have got two AC amplitudes: 12 mV and 13 mV. Setting up an amplitude is crucial for rectification because if the amplitude is too small it may fall inside the Coulomb diamond in most of the gate voltage range and we may not achieve the appreciable current [9]. Hence, amplitude is set to be at least one tenth of the height of the Coulomb diamond, i.e., e/C_Σ. It is important to note that the upper frequency limit of our measurement system is around 3 GHz which is less than the cutoff frequency of the device.

After getting all the required parameters we moved on to perform the high-frequency measurement using the setup discussed in section 3.2.

High- frequency measurement at temperature 20 K

Using the high frequency measurement setup rectified current was measured at temperature 20 K. Shown in Figure 3.15 (a) and (b) is substrate dependence of rectified current I_d when AC signal of 1 MHz with amplitude 12 and 13 mV is applied to the drain terminal sequentially.

As we can see from the graph polarity of the rectified current is changing depending on the substrate voltage, which is a typical behavior of SET rectifier [15]. Maximum rectified current of 111 pA and 140 pA was obtained at 3.30 mV and 3.34 mV of substrate voltage corresponding to 12 mV and 13 mV of AC signal amplitude, respectively. The operation point for frequency response measurement was validated from Table 3, according to which cutoff frequency should lies between diamond 4 and 5 (Fig 3.14 (c)).



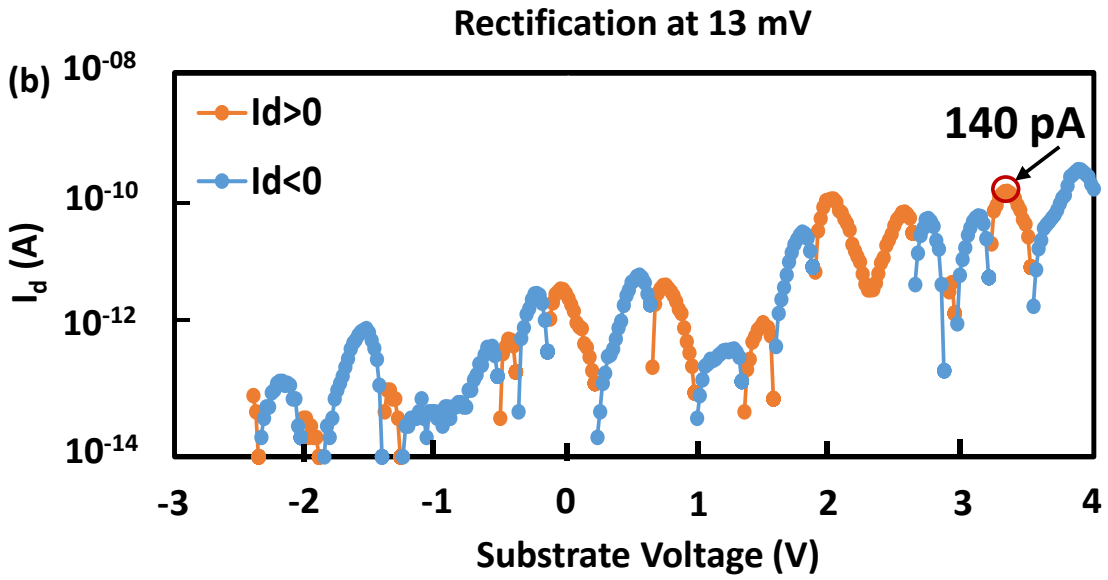


Fig. 3.15: Rectified current I_d as a function of substrate voltage V_{sub} at AC signal 1 MHz and amplitude (a) 12 mV and (b) 13 mV

Fig. 3.16 shows the frequency response of rectified current at a frequency range 300 kHz to 3 GHz. As we can see from the graph flat frequency response was achieved till 100 MHz . However, as we are moving towards the high-frequency regime high fluctuation in the response was observed and frequency response shows roll-off at frequency lower than the cutoff frequency.

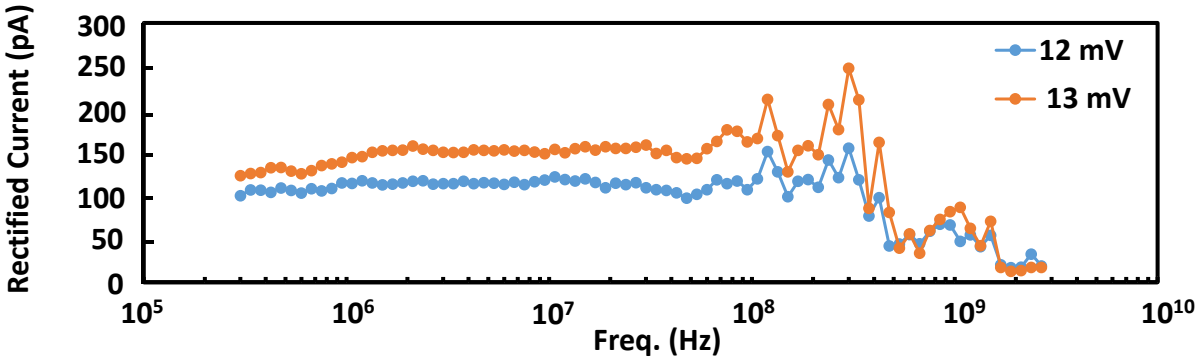


Fig. 3.16: Frequency response of the rectified current

3.3.2 SET fabricated at HU

Another type of device we evaluated is multiple island channel structure SETs. This device as well is highly doped Si nanowire based SET with an array of nanoscale island in a SOI layer (Fig. 3.17) [16], [17], [18].

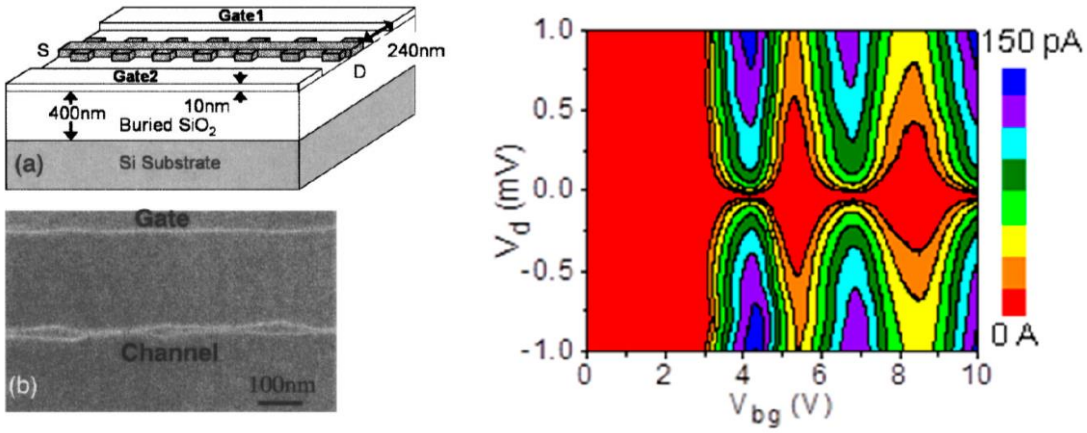


Fig. 3.17: SET with multiple channel island structure [16], [17].

There are several advantages associated with this device, i.e., high-temperature operation, suppressed cotunneling, large peak to valley ration (PVCR), easy fabrication etc. [16], [17], [19]. This device as well is heavily n^+ doped to reduce the series resistance and supports GSG pad for high frequency measurement.

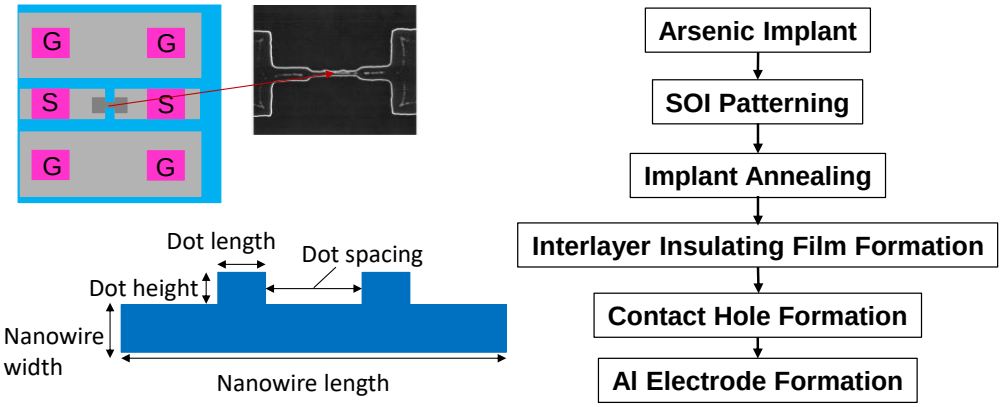


Fig. 3.18: Schematic of Si SET with multiple islands along with fabrication step

Shown in Figure 3.18 is the schematic of SET and fabrication steps involved in the fabrication of device.

This device is fabricated at Hiroshima University for HF measurement. The dot spacing and dot length of the device is fixed to 500 nm and 50 nm respectively. Whereas nanowire width is varying from 20-70 nm and nanowire length is varying from 500-3000 nm. Dot width is either 10 or 20 nm and the number of dots is either 0, 1, 2 or 11.

Shown in Fig. 3.19 is layout device. There are 9 identical chips, and each chip has 240 devices (60 types) of various dimensions.

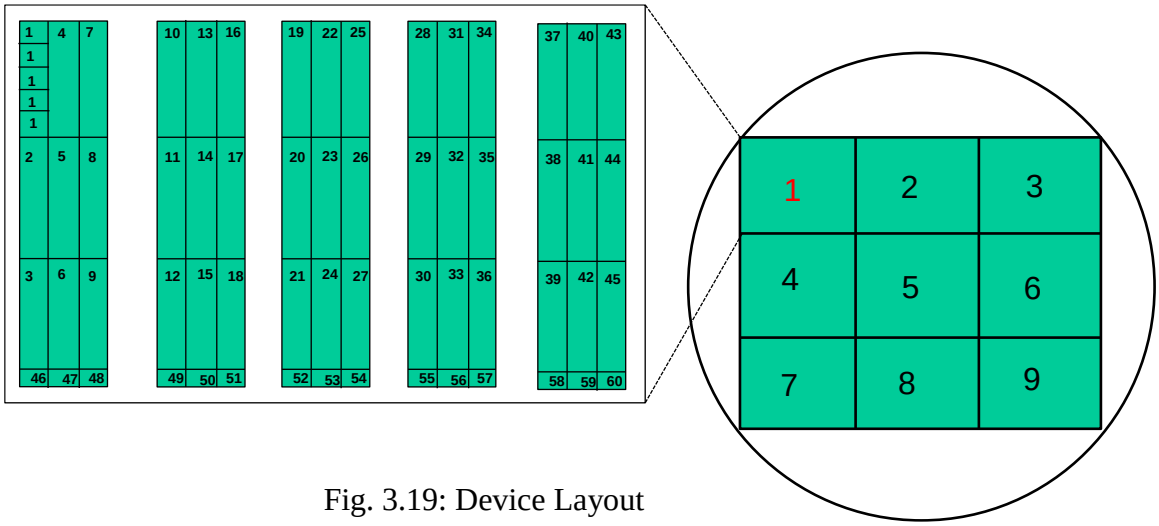


Fig. 3.19: Device Layout

Before DC characterization and HF measurement of SET devices, we checked dopant concentration of the device. This device is heavily doped with n-type arsenic dopant and SOI thickness in large area is 37.8 nm. The dopant concentration was evaluated through four probe measurement method and summarized in Table 4.

Table 4: Dopant concentration

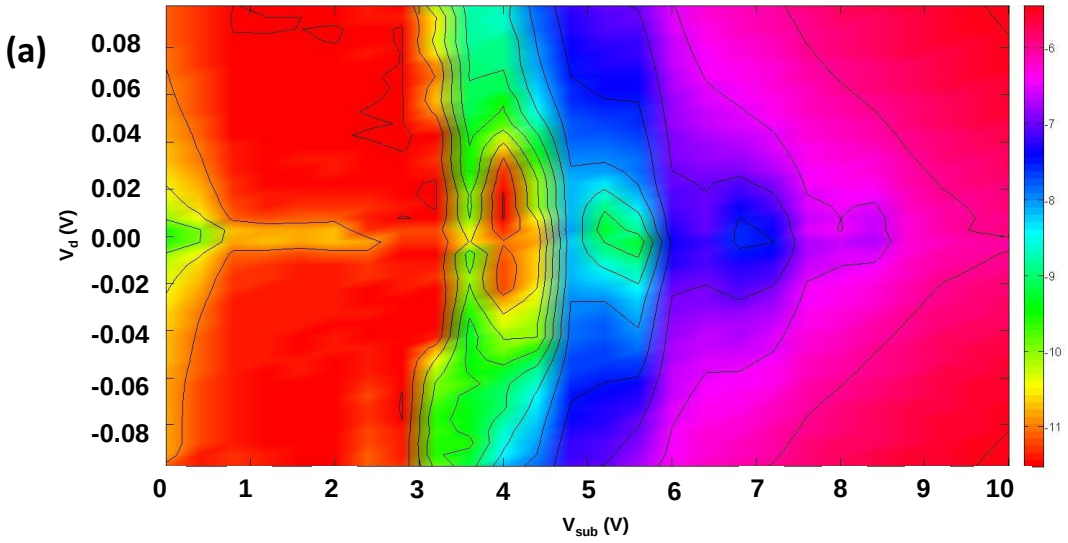
Device No.	Sheet Resistance (Ω)	Resistivity (Ωcm)	Dopant Conc. (cm^{-3})
Chip 3			
Device 1	861.89	3.26×10^{-3}	2.08×10^{19}
Device 2	884.34	3.34×10^{-3}	2.01×10^{19}
Chip 6			
Device 1	935.85	3.54×10^{-3}	1.88×10^{19}
Device 2	929.48	3.51×10^{-3}	1.88×10^{19}
Chip 9	924.12	3.49×10^{-3}	1.94×10^{19}

It was observed that the dopant concentration of Si sheet is varying chip to chip for same device specification (L: 100 μm; W: 3 μm). However, the variation is not very high and hence and be accepted.

After basic characterization we performed DC characterization of the device.

DC Characterization at temperature 20 K

Initially we selected chip 1 for the characterization. Chip 1 has total of 240 devices and stability diagram of some devices are shown in Fig. 3.20



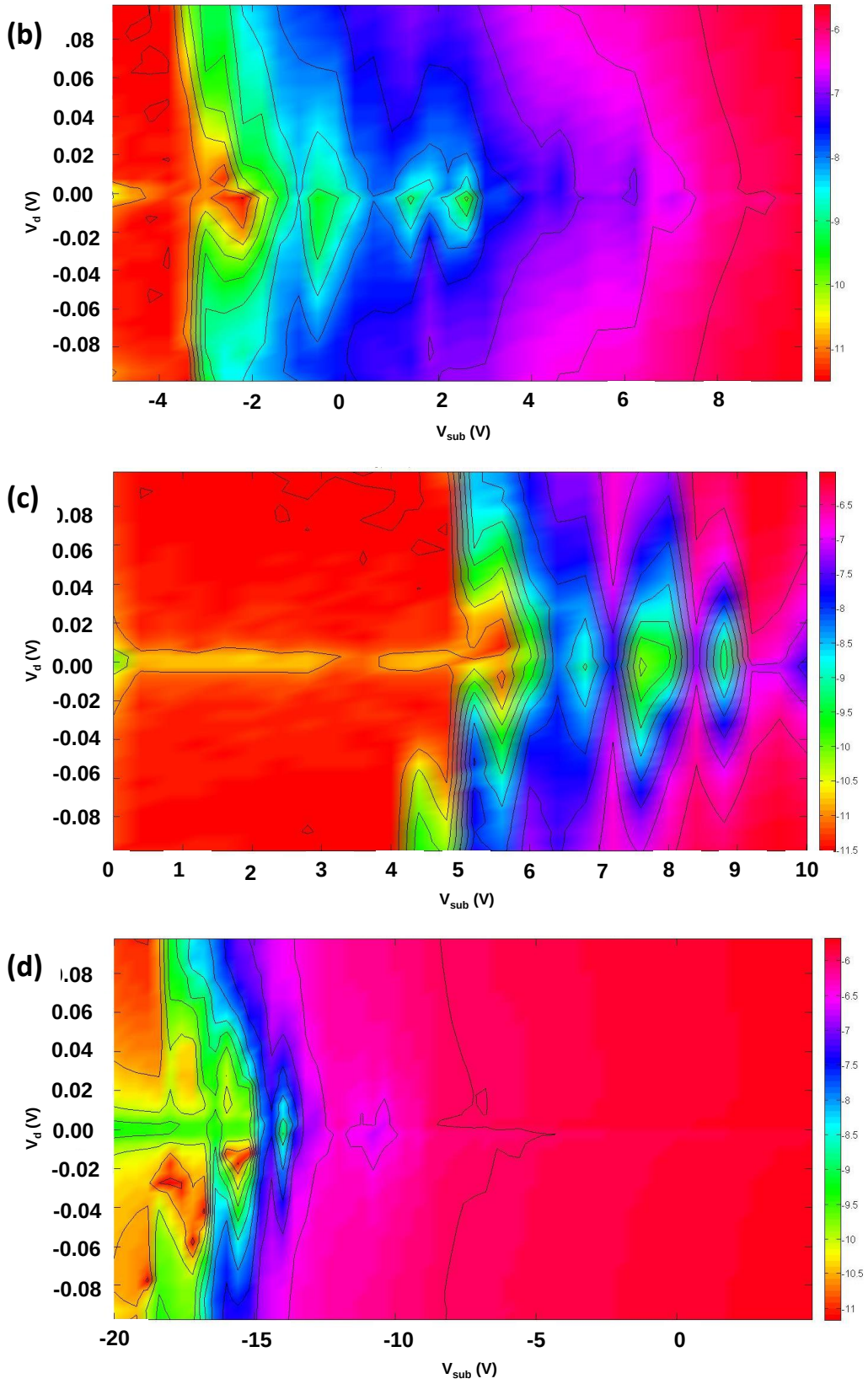
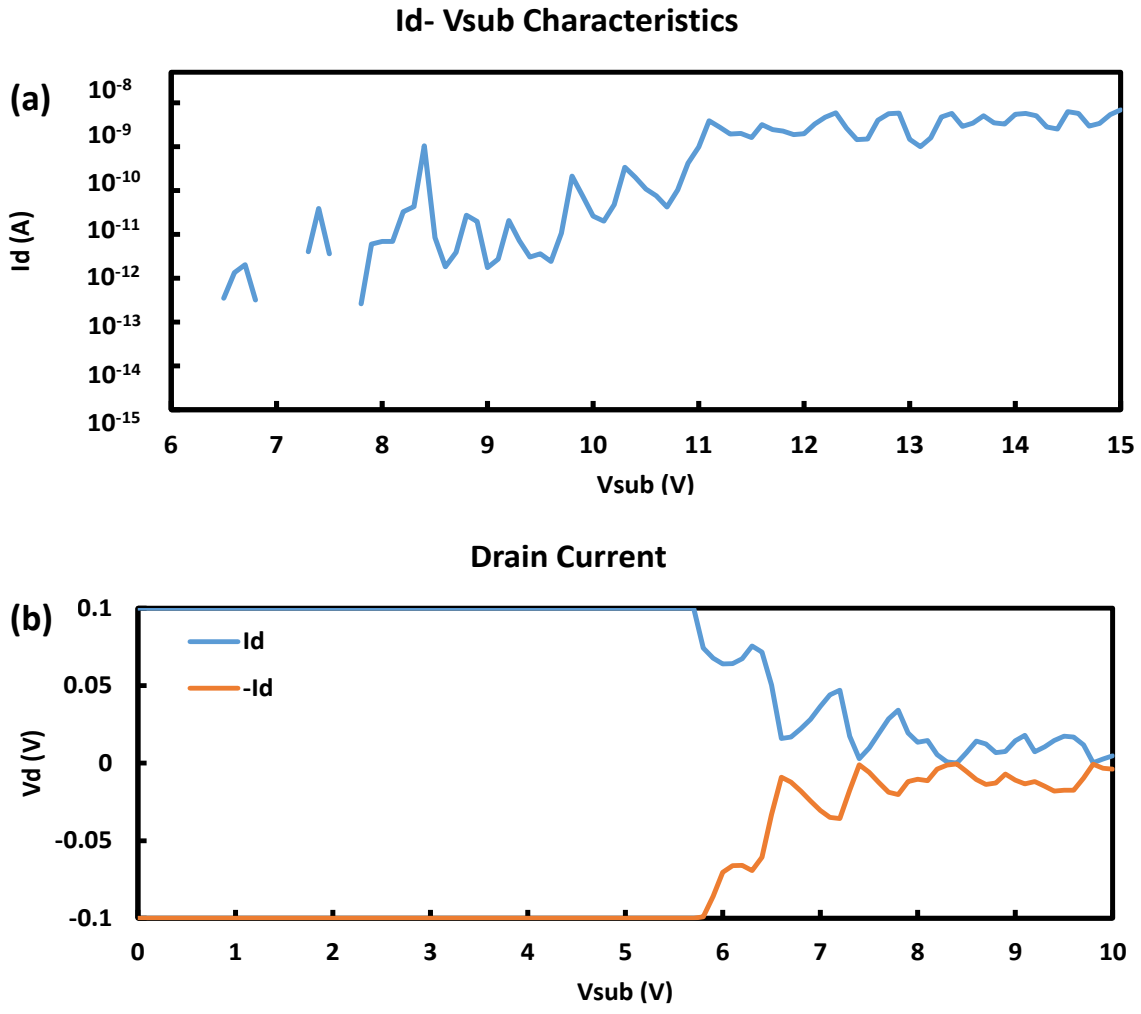


Fig. 3.20: Stability diagram of (a) #37a, L:500 nm, W:30 nm, D:0 (b) #30a, L:1000 nm, W:40 nm, D:1 (c) #44b, L:1500 nm, W:30 nm, D:2 and (d) #23c, L:3000 nm, W:50 nm, D:11

After the DC characterization of all the devices we selected device 44b as a representative device because it has good stability and better Coulomb oscillation. Device 44b has a length of 1500 nm, width 30 nm and number of dots is 2.

Shown in Figure 3.21 (a) is the drain current, I_d as a function of substrate voltage V_{sub} at drain voltage V_d 10 mV and Figure 3.21 (b) shows the V_d-V_{sub} graph at drain current ±10 pA. Coulomb oscillation was clearly visible, also, the flow of drain current was confirmed through the graph.



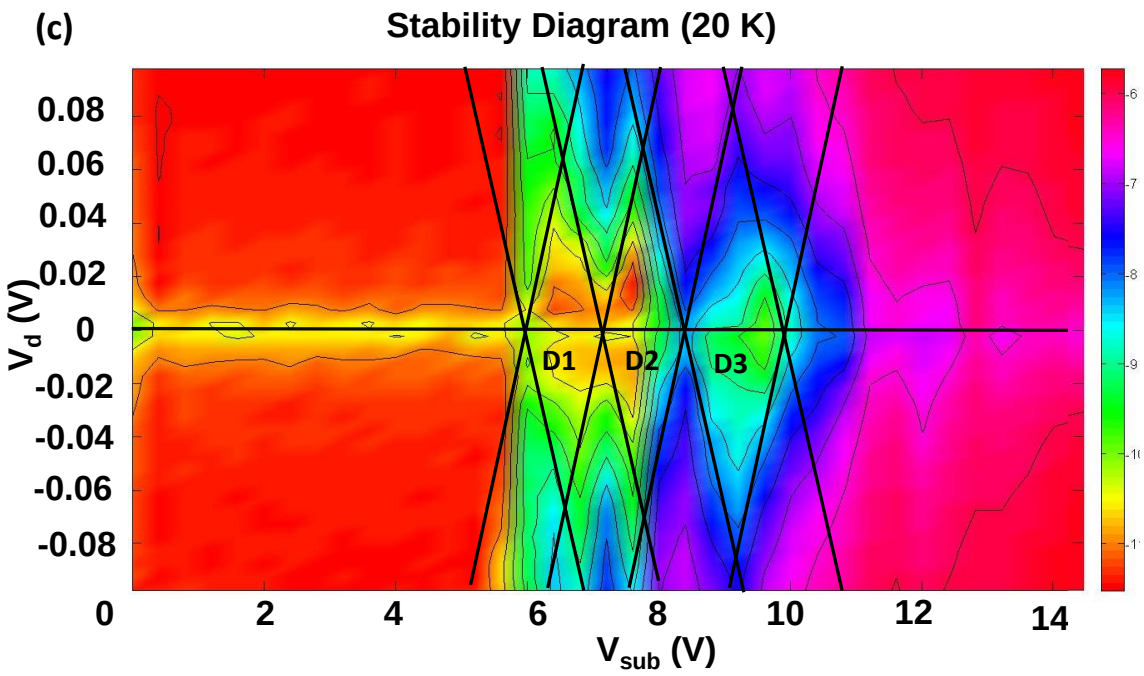


Fig. 3.21: (a) I_d-V_{sub} (b) V_d-V_{sub} and (c) Stability diagram of SET (L:1500 ; W: 30 nm)

Figure 3.21 (c) shows the drain conductance plot as a stability diagram with respect to substrate and drain voltage at 20 K temperature. Coulomb blockade effect was clearly visible with three diamonds of different sizes. Such variation in the shapes of diamonds are due to serially connected SETs with different capacitance values around the Coulomb island [20].

Considering the positive and negative slope of the diamond yet again we extract the intrinsic parameters of the SET device, i.e., source, drain and gate capacitance, source and drain resistance and cut off frequency of the device. Extracted parameters are summarized in Table 5.

Method of parameter extraction is same as discussed in section 3.3.1. Based on the extracted parameter cutoff frequency of the device lies at

diamond 2 (Fig. 3.21 (c)) with value around 15 GHz and we also got two AC signal amplitude (RMS) 11 and 13 mV.

Table 5. List of extracted SET parameters

Diamond	C_g (aF)	C_s (aF)	C_d (aF)	R_d=R_s(MΩ)	f_c(GHz)	*Amplitude (mV)*
Diamond 1	0.16	1.09	1.25	64.4	0.49	11.31
Diamond 2	0.11	1.01	1.11	2.38	15.0	12.72
Diamond 3	0.11	0.95	1.05	7.33	5.15	13.43

Based on the extracted parameter we performed the high frequency measurement using the measurement circuit described in section 3.2.

High-frequency measurement at temperature 20 K

Initially we applied AC signal to drain terminal of SET and rectified current at the source terminal was measured using pA meter. Figure 3.22 shows the rectified current as a function of substrate voltage when an AC signal at 1 MHz is applied to the drain terminal with an amplitude of (a) 11 mV and (b)13 mV. It can be seen that rectified current is becoming positive and negative depending on the substrate voltage, which is the typical behavior of SET rectifier [15].

Operation point for high-frequency measurement is where rectified current is maximum. In Figure 3.22 (a) and (b) maximum rectified current, 117 pA and 216 pA respectively, was obtained corresponding to substrate voltage 9.5 V, which corresponds to the position of second diamond. Hence,

the extracted parameters in Table 5 validate the operation point of high frequency measurement as cutoff frequency of the device lies in second diamond.

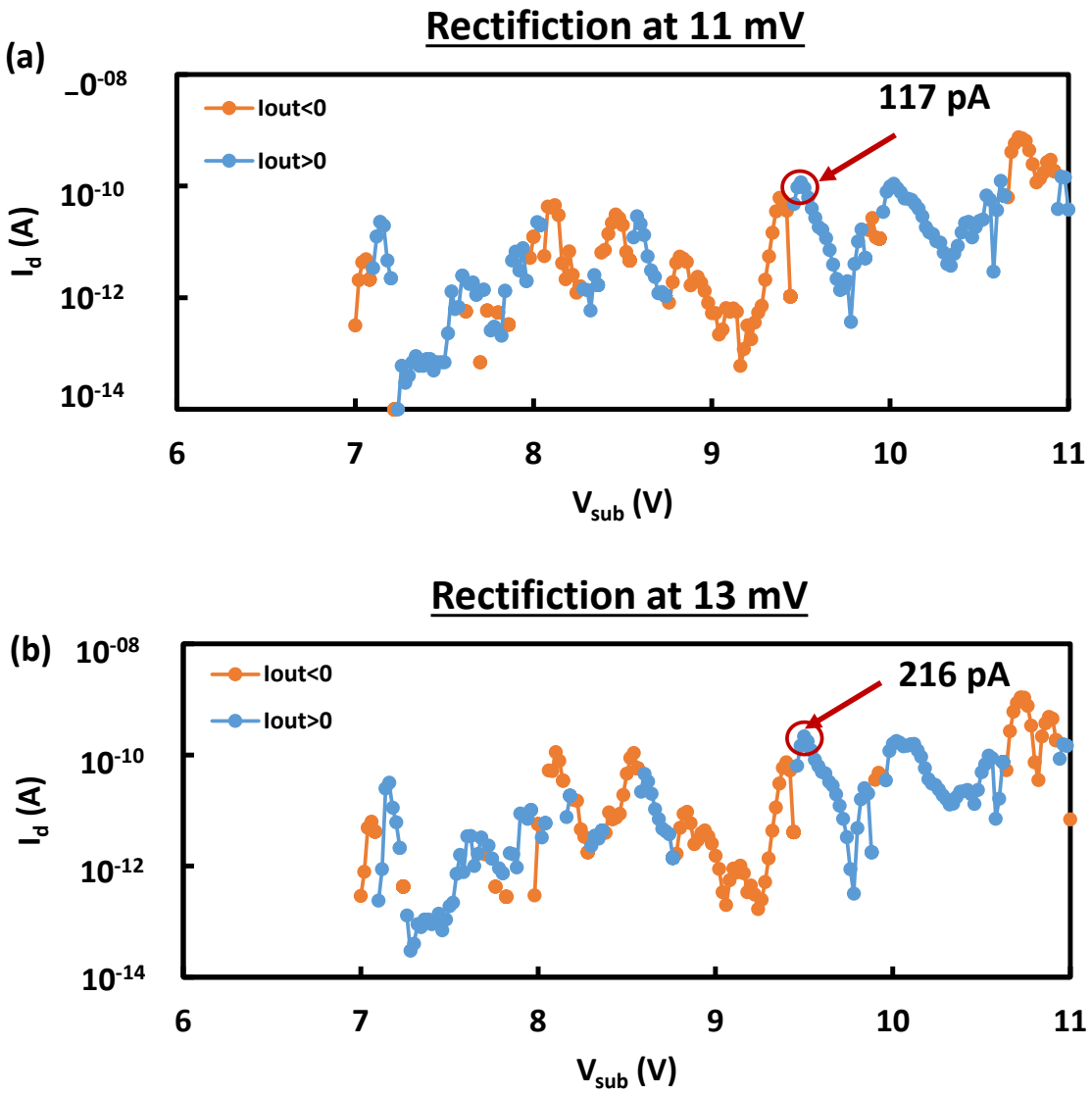


Fig. 3.22: Rectified current I_d as a function of substrate voltage V_{sub} at AC signal 1 MHz and amplitude (a) 11 mV and (b) 13 mV

At an operation point of substrate voltage 9.5 V we checked the frequency response of rectified current. Shown in Figure 3.23 is the frequency response of SET at a frequency range 300 kHz to 3 GHz (upper limit of the measurement system).

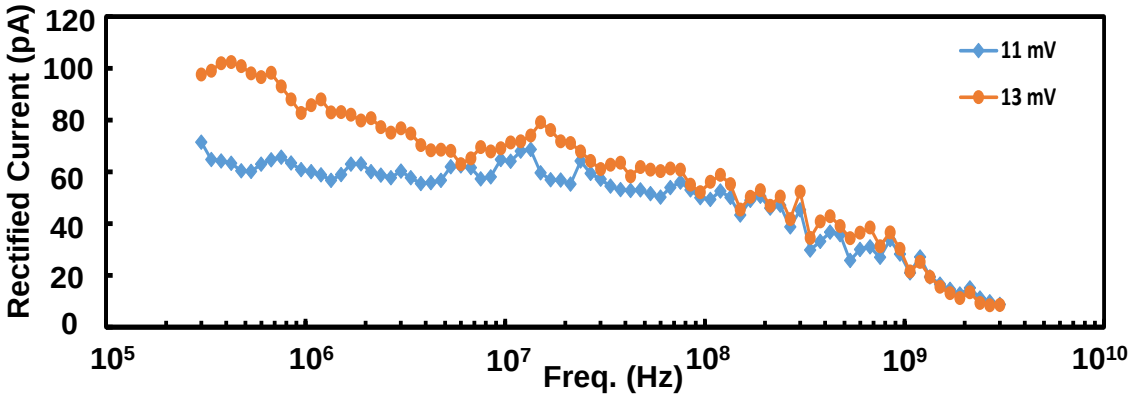


Fig. 3.23: Frequency response of the rectified current

As we can see from the graph towards the lower frequency side almost flat curve is visible. However, as we are moving towards the higher frequency side curve has descended. It is also to be noted that fluctuation at the higher frequency side is not much and compared to the frequency response of heavily doped Si nanowire-based SET fabricated at SU, smooth curve is obtained.

3.4 Discussion on high frequency response of SET

In the abovementioned sections 3.3 high frequency response of the heavily doped Silicon nanowire-based SET devices has been discussed. However, frequency response of both devices in the high frequency regime is not as expected. As per the simulation result (in chapter 2, section 2.3) frequency response of the SET devices should be flat with a small drop around

the cutoff frequency. However, the experimental verification of frequency response is not achieved due to fluctuation in the characteristics at the high frequency regime (Fig. 3.16 and 3.23).

As per our understanding there could be two reasons for such behavior:

- Limitation of the high-frequency measurement setup
- Issue of the contact resistance between pad and probe

However, as we already have discussed about the optimization of high frequency measurement setup in section 3.2, we will now discuss about the contact resistance in the following sections.

3.4.1 Contact resistance between pad and probe

Contact resistance between pad area and measurement probe is an important parameter which needs to be discussed to understand the frequency response of SET devices. Shown in Figure 3.24 is the layout of device used for contact resistance measurement.

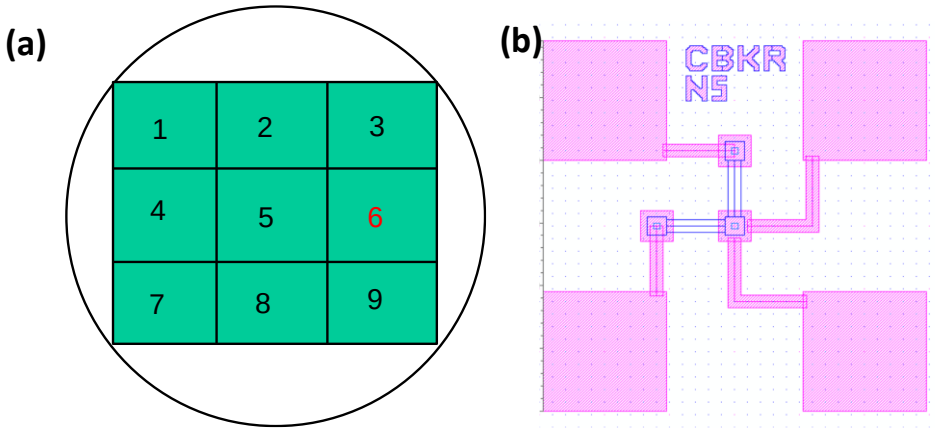


Fig. 3.24: (a) Si wafer layout of SET devices with multiple island channel (b) CBKR layout of chip 6 for evaluating contact resistance

Devices having dimension 5 μm, 10 μm and 15 μm are evaluated using four probe measurement method at temperature 300 K. Evaluated contact resistances are listed on Table 6.

Table 6: Contact Resistance

Dimension	**Contact resistance (Ωcm^2)**
5 x 5 μm	6.84×10^{-04}
10 x 10 μm	4.59×10^{-04}
15 x15 μm	3.99×10^{-04}

As we can see from Table 6 contact resistance for the devices are large. Such large values are not desirable as it may perturb the devices performance.

Also, the cutoff frequency between pad area capacitance and contact resistance is calculated at 300 K of temperature to check its effect on frequency response of the SET device. Using the dimension of pad area (50 x 40 μm) having six contacts of 10 μm^2, capacitance C is calculated using the formula: $C = \frac{\varepsilon k A}{d}$, where ε is permittivity of space, k is permittivity of SiO_2 , A is area of the pad and d is BOX thickness (400 nm). Resistance R is calculated using the contact resistance corresponding to device having 10 μm of dimension. Finally cutoff frequency f_c is calculated using the formula $f_c = \frac{1}{2\pi RC}$ = 12 GHz. It is to be noted that this calculated cutoff frequency may become lower at low temperatures due to the increased contact resistance.

Based on the obtained results it is concluded that the contact resistance of all the devices is high. However, since the cutoff frequency set by the contact resistance and pad area capacitance is high (12 GHz) it should not affect the frequency response of SET devices if the contact resistance is fixed.

Summary

To verify the simulated result that, 'SET can become an important high frequency (HF) rectifier where conventional rectifiers cannot operate' (section 2.3), experimentally, we characterized three types of SETs: SET fabricated by PADOX method and two heavily doped silicon nanowire-based SET.

After initial characterization of SET fabricated by PADOX method it was concluded that this type of device is not suitable for high-frequency characterization due to low cutoff frequency of parasitic MOSFETs. Consequentially, heavily doped nanowire-based SETs were further characterized and considered as potential reference devices for high-frequency measurement.

High frequency measurement was then performed on heavily doped SET using the optimized high-frequency measurement setup and it was observed that at the lower frequency side frequency response of rectified current is almost flat. However, towards the high frequency side reduced

current continues to flow up to 3 GHz (limit of the measurement system). Observed high fluctuation towards the higher frequency side is not desirable.

We further discussed the frequency response of nanowire-based SETs and tried to understand the reason behind fluctuation in the frequency response at high-frequency regime. In this regard we discussed contact resistance between pad area of the device and measurement probe. However, the reason behind high fluctuation at the high frequency regime is still not clear and further understanding is needed.

The goal is to evaluate the accurate high-frequency rectifying response of SET which is not affected by any external components.

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Chapter 4

SUMMARY AND FINAL CONCLUSION

4.1 Summary and Conclusion

The main objective of this thesis is to investigate the high-frequency behavior of single electron transistors. In order to do it we studied the high frequency rectifying characteristics of SET and capacitance components inside the SET at high frequency.

High-frequency rectifying characteristics of SET

Under this section we investigated the reason behind, 'no cutoff frequency in the rectifying action of SET'. Using the SET model, based on time dependent master equation with an assumption that number of electrons on the island is limited to four (-1,0,1,2), we reproduced the experimental finding of the rectifying operation far beyond the conventional cutoff frequency set by the CR time constant. We further clarified the mechanism behind such phenomena. Finally, it was concluded that the asymmetry in the tunneling rate with respect to the drain voltage is responsible for the rectifying operation at high frequencies even if the asymmetry in the probability of state (probability of finding electrons in the island) observed at low frequencies doesn't exist at high frequency .

We also attempted experimental verification of the simulated results using 2 different types of SETs.: i) SET fabricated by PADOX method and ii) Heavily doped Si nanowire-based SET. Initially, DC characterization of all the devices were performed and then high frequency measurement was performed. Among all the three devices it is reported that SET fabricated by PADOX method is not suitable for high-frequency measurement because of low cutoff frequency of parasitic MOSFETs. Consequentially, heavily doped nanowire-based SET is selected as a reference device for high-frequency measurement.

For high-frequency measurement we prepared measurement setup and then optimized it as well. All the equipment's involved in the measurement setup has been calibrated and validated before HF measurement was performed. Special attention has been paid to avoid the degradation of the signal integrity i.e., using high frequency cables and connectors and GSG probe. Also, to provide the DC return path 6 dB attenuator has been used.

Frequency response of the SETs is then studied, and it is reported that at the lower frequency regime flat frequency response is achieved however, towards the high frequency regime there is high fluctuation in the characteristics.

Furthermore, reason behind such behavior of frequency response at higher frequency is discussed based on the contact resistance. Contact resistance between pad area and measurement probe is discussed and it is

reported that value of contact resistance is large (~10^{-4} Ωcm^2). Such high values are not desirable, and it raises some concern of the increased contact resistance at low temperature. However, the calculated cutoff frequency caused by pad area capacitance and contact resistance as well is high (12 GHz). Hence, it should not be the reason behind high fluctuation of the frequency response at high frequencies at least at room temperature.

As a conclusion reason behind high fluctuation in the frequency response is still not clear and further understanding is required.

Capacitance components inside the SET

Understanding of capacitance components inside the SET is crucial for understanding the high frequency operation of SET. In order to understand the capacitance components of SET, based on the time-dependent master equation and taking the dynamic gate current into account, a new single-electron transistor (SET) model is proposed, which can represent terminal capacitances and transcapacitances.

By using this model, bias, frequency, and temperature dependences of these intrinsic capacitances has been evaluated. Based on the obtained result it was concluded that at the at the higher frequency transistor action of the SET is lifted and it behaves like passive capacitance network.

High-frequency characteristics of the SET-based amplifier as well is evaluated, and results indicate the same. At low frequencies, the voltage gain

close to the slope of the descending side of the Coulomb diamond is obtained, and the phase is inverted. At high frequencies, inverting amplifier transforms to the capacitive divider and the output is in phase with the input.

Apart from abovementioned point the SPICE circuit simulator is used as a solver for the simultaneous differential equation, which also enables the model to analyze the behavior of various circuits including SETs.

4.2 Future Work

This time in our proposed SET model tunneling time is not considered. Hence, in the future new approach for SET model can be considered by taking tunneling time into account.

Based on the achieved simulation results we can say that SET can becomes an important rectifier at ultrahigh frequencies where conventional devices cannot operate. However, for experimental verification further understanding of the frequency response of SET is necessary. After experimental verification in the future SET rectifier can be used as terahertz detector, mixer for heterodyne detection, frequency multiplier, optical rectenna etc., where the use of conventional rectifiers has been limited due to varieties of fundamental limitations.

Also, using our newly proposed dynamic SET model we can gain an insight and understanding of the intrinsic capacitance component of SET behavior at high frequency. Since the proposed dynamic SET model is

implemented in the SPICE circuit simulator, it can be used to analyze the circuits for high-frequency amplification, oscillation, detection, the gate-based sensing of quantum states, and so on.

List of Publications and Proceedings

List of Journal Publications

[1] **A. Singh**, T. Nishimura, H. Satoh and H. Inokawa, "Dynamic Single-Electron Transistor Modeling for High-Frequency Capacitance Characterization.," *Applied Sciences 2022, 12, 8139.* https://doi.org/10.3390/app12168139

[2] Y. Iwata, T. Nishimura, **A. Singh,** H. Satoh, and H. Inokawa, "High-frequency rectifying characteristics of metallic single-electron transistor with niobium nanodots," *2022 Jpn. J. Appl. Phys. 61 SC1063*.

List of Conference Proceedings

[1] **A. Singh**, S. Matsumoto, H. Satoh, and H. Inokawa, "Silicon single-electron transistor as a high-frequency rectifier," *Proc. 2021 Silicon Nanoelectronics Workshop (SNW), 2021, pp. 1-2.*

[2] **A. Singh**, T. Nishimura, H. Satoh, and H. Inokawa, Dynamic single-electron transistor model with capacitance analysis capability,"*2022 Silicon Nanoelectronics Workshop (SNW), 2022.*

List of Conferences and Symposium

[1] **A. Singh** , T. Nishimura, H. Satoh, and H. Inokawa, "High frequency characterization of silicon single-electron transistor as a rectifier", *4th International Symposium on Biomedical Engineering*,2019, Japan

[2] **A. Singh** , T. Nishimura, H. Satoh, and H. Inokawa, "High-frequency response of Si-SET: Experimental verification", *67th Japan Society of Applied Physics Spring Meeting*, 2020, 14p-B508-3, Japan

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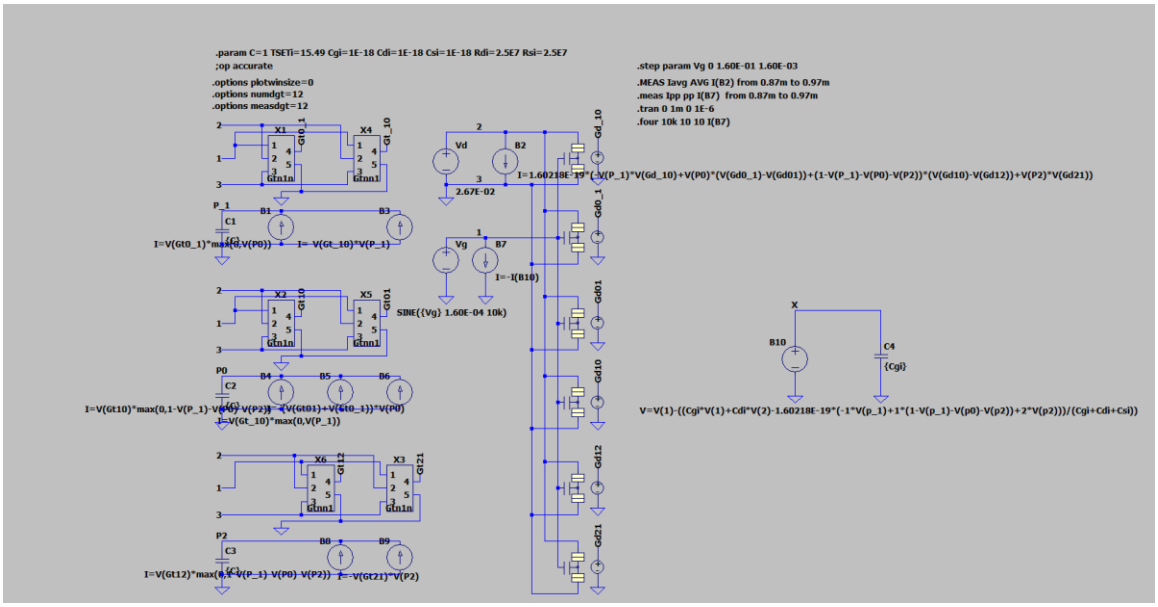
Appendix

A1. Schematic and netlist of the simulation used in chapter 2



Net list of the circuit used in the time-dependent master equation method

```
C1 P_1 0 {C}
B1 0 P_1 I=V(Gt0_1)*max(0,V(P0))
B3 0 P_1 I=-V(Gt_10)*V(P_1)
C2 P0 0 {C}
B4 0 P0 I=V(Gt10)*max(0,1-V(P_1)-V(P0)-V(P2))
B5 0 P0 I=V(Gt_10)*max(0,V(P_1))
B6 0 P0 I=-(V(Gt01)+V(Gt0_1))*V(P0)
C3 P2 0 {C}
B8 0 P2 I=V(Gt12)*max(0,1-V(P_1)-V(P0)-V(P2))
B9 0 P2 I=-V(Gt21)*V(P2)
```

```
XU2 1 2 0 Gd_10 0 Gdnn1 nelec=-1 TSET=TSETi Cg=Cgi
Cd=Cdi Cs=Csi Rd=Rdi Rs=Rsi

XU4 1 2 0 Gd01 0 Gdnn1 nelec=0 TSET=TSETi Cg=Cgi Cd=Cdi
Cs=Csi Rd=Rdi Rs=Rsi

XU6 1 2 0 Gd12 0 Gdnn1 nelec=1 TSET=TSETi Cg=Cgi Cd=Cdi
Cs=Csi Rd=Rdi Rs=Rsi

XU8 1 2 0 Gd0_1 0 Gdn1n nelec=-1 TSET=TSETi Cg=Cgi
Cd=Cdi Cs=Csi Rd=Rdi Rs=Rsi

XU9 1 2 0 Gd10 0 Gdn1n nelec=0 TSET=TSETi Cg=Cgi Cd=Cdi
Cs=Csi Rd=Rdi Rs=Rsi

XU11 1 2 0 Gd21 0 Gdn1n nelec=1 TSET=TSETi Cg=Cgi
Cd=Cdi Cs=Csi Rd=Rdi Rs=Rsi

B2 2 0 I=1.60218E-19*(-V(P_1)*V(Gd_10)+V(P0)*(V(Gd0_1)-
V(Gd01))+(1-V(P_1)-

V(P0)-V(P2))*(V(Gd10)-V(Gd12))+V(P2)*V(Gd21))

Vg 1 0 0.15

XX1 1 2 0 Gt0_1 0 ggtn1n params: nelect=-1 TSETt=TSETi
Cgt=Cgi Cdt=Cdi Cst=Csi

Rdt=Rdi Rst=Rsi

XX2 1 2 0 Gt10 0 ggtn1n params: nelect=0 TSETt=TSETi
Cgt=Cgi Cdt=Cdi Cst=Csi

Rdt=Rdi Rst=Rsi

XX3 1 2 0 Gt21 0 ggtn1n params: nelect=1 TSETt=TSETi
Cgt=Cgi Cdt=Cdi Cst=Csi

Rdt=Rdi Rst=Rsi

XX4 1 2 0 Gt_10 0 ggtnn1 params: nelect=-1 TSETt=TSETi
Cgt=Cgi Cdt=Cdi Cst=Csi

Rdt=Rdi Rst=Rsi

XX5 1 2 0 Gt01 0 ggtnn1 params: nelect=0 TSETt=TSETi
Cgt=Cgi Cdt=Cdi Cst=Csi
```

```
Rdt=Rdi Rst=Rsi

XX6 1 2 0 Gt12 0 ggtnn1 params: nelect=1 TSETt=TSETi
Cgt=Cgi Cdt=Cdi Cst=Csi

Rdt=Rdi Rst=Rsi

Vd 2 0 SINE(0 0.005 7.40E3)


* block symbol definitions

.subckt ggtn1n 1 2 3 4 5

XU1 1 2 3 N001 5 Gdn1n nelec=nelect TSET=TSETt Cg=Cgt
Cd=Cdt Cs=Cst Rd=Rdt

Rs=Rst

XU2 1 2 3 4 N001 Gsn1n nelec=nelect TSET=TSETt Cg=Cgt
Cd=Cdt Cs=Cst Rd=Rdt

Rs=Rst

.ends ggtn1n


.subckt ggtnn1 1 2 3 4 5

XU1 1 2 3 N001 5 Gsnn1 nelec=nelect TSET=TSETt Cg=Cgt
Cd=Cdt Cs=Cst Rd=Rdt

Rs=Rst

XU2 1 2 3 4 N001 Gdnn1 nelec=nelect TSET=TSETt Cg=Cgt
Cd=Cdt Cs=Cst Rd=Rdt

Rs=Rst

.ends ggtnn1


.PARAM C=1 TSETi=0.8 Cgi=4.7E-19 Cdi=2.5E-18 Csi=2.5E-
18 Rdi=2.5E9 Rsi=2.5E9

;dc Vd -0.01 0.01 0.1E-3 Vg 0.115 0.235 0.02
```

```
;op accurate
;ac dec 10 1E5 1E11
.tran 0 10m 0 1.35E-06
.MEAS Iave AVG I(B2) from 1000u to 10000u
.lib Gdn1n.lib
.lib Gdnn1.lib
.lib Gsn1n.lib
.lib Gsnn1.lib
.backanno
.end
```

Gdn1n.lib

```
* Gdn1n: Tunneling rate at drain junction from n+1 to n state
* represented as a voltage source
*
* connections: GATE
* | DRAIN
* | | SOURCE
* | | | OUT1(+)
* | | | | OUT2(-)
* | | | | |
.SUBCKT Gdn1n 1 2 3 4 5 nelec=0 TSET=25 Cg=1E-18 Cd=1E-18 Cs=1E-18 Rd=1E6
Rs=1E6
*
.PARAM elec=1.6021892E-19 $ [C]
```

```
.PARAM kB=1.380662E-23 $ [J/K]
*
* TSET - Temperature [K]
* Cg - Gate Capacitance [F]
* Cd - Drain Capacitance [F]
* Cs - Source Capacitance [F]
* Rd - Tunneling Resistance of Drain Junction [ohm]
* Rs - Tunneling Resistance of Source Junction [ohm]
*
.PARAM Csgm = 'Cs+Cd+Cg'
*
B1 4 5 V =-1/elec/Rd*(Cg*V(1,3)-V(2,3)*Cg-V(2,3)*Cs-
nelec*elec-
1/2*elec)/Csgm/(1-exp((Cg*V(1,3)-V(2,3)*Cg-V(2,3)*Cs-
nelec*elec-
1/2*elec)*elec/Csgm/kB/TSET))
*
.ENDS
*****


Gdnn1.lib
* Gdnn1: Tunneling rate at drain junction from n to n+1
state
* represented as a voltage source
*
* connections: GATE
* | DRAIN
* | | SOURCE
```

```
* | | | OUT1(+)
* | | | | OUT2(-)
* | | | | |
.SUBCKT Gdnn1 1 2 3 4 5 nelec=0 TSET=25 Cg=1E-18 Cd=1E-
18 Cs=1E-18 Rd=1E6
Rs=1E6
*
.PARAM elec=1.6021892E-19 $ [C]
.PARAM kB=1.380662E-23 $ [J/K]
*
* TSET - Temperature [K]
* Cg - Gate Capacitance [F]
* Cd - Drain Capacitance [F]
* Cs - Source Capacitance [F]
* Rd - Tunneling Resistance of Drain Junction [ohm]
* Rs - Tunneling Resistance of Source Junction [ohm]
*
.PARAM Csgm = 'Cs+Cd+Cg'
*
B1 4 5 V =1/elec/Rd*(Cg*V(1,3)-V(2,3)*Cg-V(2,3)*Cs-
nelec*elec-
1/2*elec)/Csgm/(1-exp(-(Cg*V(1,3)-V(2,3)*Cg-V(2,3)*Cs-
nelec*elec-
1/2*elec)*elec/Csgm/kB/TSET))
*
.ENDS
*****
```

```
Gsn1n.lib
* Gsn1n: Tunneling rate at source junction from n+1 to
n state
* represented as a voltage source
*
* connections: GATE
* | DRAIN
* | | SOURCE
* | | | OUT1(+)
* | | | | OUT2(-)
* | | | | |
.SUBCKT Gsn1n 1 2 3 4 5 nelec=0 TSET=25 Cg=1E-18 Cd=1E-
18 Cs=1E-18 Rd=1E6
37
Rs=1E6
*
.PARAM elec=1.6021892E-19 $ [C]
.PARAM kB=1.380662E-23 $ [J/K]
*
* TSET - Temperature [K]
* Cg - Gate Capacitance [F]
* Cd - Drain Capacitance [F]
* Cs - Source Capacitance [F]
* Rd - Tunneling Resistance of Drain Junction [ohm]
* Rs - Tunneling Resistance of Source Junction [ohm]
*
.PARAM Csgm = 'Cs+Cd+Cg'
```

```
*
B1 4 5 V =-1/elec/Rs*(Cg*V(1,3)+Cd*V(2,3)-nelec*elec-
1/2*elec)/Csgm/(1-
exp(elec*(Cg*V(1,3)+Cd*V(2,3)-nelec*elec-
1/2*elec)/Csgm/kB/TSET))
*
.ENDS
*****
```

Gsnn1.lib

```
* Gsnn1: Tunneling rate at source junction from n to
n+1 state
* represented as a voltage source
*
* connections: GATE
* | DRAIN
* | | SOURCE
* | | | OUT1(+)
* | | | | OUT2(-)
* | | | | |
.SUBCKT Gsnn1 1 2 3 4 5 nelec=0 TSET=25 Cg=1E-18 Cd=1E-
18 Cs=1E-18 Rd=1E6
Rs=1E6
*
.PARAM elec=1.6021892E-19 $ [C]
. PARAM kB=1.380662E-23 $ [J/K]
*
```

```
* TSET - Temperature [K]
* Cg - Gate Capacitance [F]
* Cd - Drain Capacitance [F]
* Cs - Source Capacitance [F]
* Rd - Tunneling Resistance of Drain Junction [ohm]
* Rs - Tunneling Resistance of Source Junction [ohm]
*
.PARAM Csgm = 'Cs+Cd+Cg'
*
B1 4 5 V =1/elec/Rs*(Cg*V(1,3)+Cd*V(2,3)-nelec*elec-
1/2*elec)/Csgm/(1-exp(-
elec*(Cg*V(1,3)+Cd*V(2,3)-nelec*elec-
1/2*elec)/Csgm/kB/TSET))
*
.ENDS
```