A -31.7 dBm Sensitivity 0.011 mm2 CMOS On-Chip Rectifier for Microwave Wireless Power Transfer

electronics

MDPI

Article

A −31.7 dBm Sensitivity 0.011 mm^2 CMOS On-Chip Rectifier for Microwave Wireless Power Transfer

Takuma Hashimoto [1], Hikaru Nekozuka [2], Yoshitaka Toeda [2], Masayuki Otani [2], Yasuhiko Fukuoka [2] and Toru Tanzawa [1,*]

[1] Graduate School of Integrated Science and Technology, Shizuoka University, Hamamatsu 432-8561, Japan; hashimoto.takuma.17b@shizuoka.ac.jp
[2] Kyocera Corp., Yokohama 226-8512, Japan; hikaru.nekozuka.cy@kyocera.jp (H.N.); yoshitaka.toeda.zs@kyocera.jp (Y.T.); masayuki.otani.xm@kyocera.jp (M.O.); yasuhiko.fukuoka.xm@kyocera.jp (Y.F.)
* Correspondence: toru.tanzawa@shizuoka.ac.jp

Abstract: This paper pursued both the lower operating power limit and small area of on-chip rectifiers for microwave wireless power transfer (MWPT). RF–DC charge pump rectifiers can operate in the fast switching limit at a high frequency of 920 MHz even with a small stage capacitor C_{in} of 100 fF, which contributes to an area reduction in the on-chip rectifiers. Circuit design starts with C_{in} determined as small as possible, followed by the determination of switching transistors and the number of stages. Even at an extremely low input power of 1 µW, wiring resistance in RF inputs is critical. Routing of the RF inputs is designed in line with stage capacitors. Bonding pad structure also affects the lower input power limit. Ground-shielded pad design can reduce the lower limit. Various types of RF–DC charge pump rectifiers are fabricated in 65 nm CMOS. An ultra-low-power diode RF–DC charge pump rectifier with 32 stages had a lower input power limit of −31.7 dBm at an output voltage of 1.0 V. Its small silicon area of 0.011 mm^2 allows RF–DC rectifiers to be integrated in sensor ICs. More advanced technology providing MIM capacitors with higher capacitance density and placing switching MOSFETs under the MIM capacitors will further reduce the area of RF–DC charge pump rectifiers, allowing them to be integrated in sensor ICs.

Keywords: RF–DC; charge pump; converter; rectenna; microwave wireless power transfer; IoT; energy harvesting

Citation: Hashimoto, T.; Nekozuka, H.; Toeda, Y.; Otani, M.; Fukuoka, Y.; Tanzawa, T. A −31.7 dBm Sensitivity 0.011 mm^2 CMOS On-Chip Rectifier for Microwave Wireless Power Transfer. *Electronics* **2023**, *12*, 1400. https://doi.org/10.3390/electronics12061400

Academic Editor: Djuradj Budimir

Received: 21 February 2023
Revised: 9 March 2023
Accepted: 14 March 2023
Published: 15 March 2023

1. Introduction

In recent years, microwave wireless power transfer (MWPT) has attracted much attention as a method of powering sensor ICs of IoT devices [1]. Using 1 trillion sensor ICs per year is predicted in the near future by development of 5G and Artificial Intelligence [2]. If each of these devices is equipped with batteries, a large number of sensor ICs will need to be maintained for the battery with a significant cost increase. MWPT can reduce this cost, and ultimately, reduce this to zero. In addition, because MWPT uses electromagnetic (EM) waves for the power source, a wireless communication network can be built in the same time to receive and transmit sensed data. A MWPT system mainly consists of a transmitter for radiating EM waves and a receiver with a receiving antenna and a rectifier for capturing the radiated EM waves. This combination of receiving antenna and rectifier is called a rectenna [3]. Figure 1 shows a block diagram of a rectenna.

This research aims at extending the transmission distance focused on the rectifier part of rectenna circuit for low power application, or at reducing the lower operating power limit of rectennas, with a rectifier circuit area small enough to be integrated in sensor ICs. According to Friis's formula, transmission distance is inversely proportional to received power squared [4]. By extending the transmission distance, powering to increased sensor ICs in a wide range such as factories is enabled with only one transmitter.

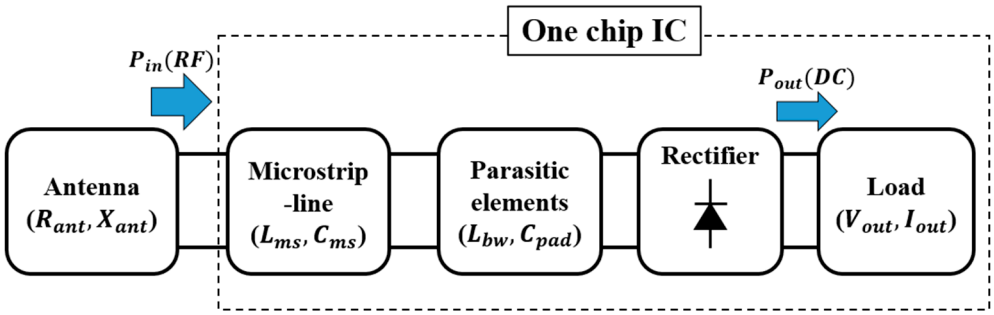


Figure 1. Block diagram of rectenna circuit for MWPT.

Research on MWPT techniques has been conducted on a wide range of topics, including optimal rectenna design methodology and improving the performance of rectifier circuits. In [5], it was reported that a circuit topology of minimizing the junction capacitance of diodes to achieve higher conversion efficiency under the condition of constant antenna impedance was used. The most significant parameter for conversion efficiency was analyzed in [6], and the circuit topology proposed in [5] in accordance with this analysis. In [7], the optimal rectenna design is conducted on considering parasitic elements generated by integration for combination of specific antenna and specific on-chip rectifier. The authors of [8] proposed the design methodology for selecting the optimum rectifier from multiple types for specific antenna types to explore a larger design space than in [5–7]. Furthermore, the authors of [9] proposed a methodology to select the best combination of multiple types of antennas and rectifiers by using the model calculation. The analysis covering a wider range of design conditions can be conducted in a shorter time than in [8]. These works focused on the optimum rectenna design. In [10], a circuit topology was proposed to cancel the threshold voltage by connecting the gates of NMOS and PMOS in each stage of the rectifier unit to the output and input terminals, respectively, because threshold voltage has a great effect on the conversion efficiency of on-chip rectifier. However, under the high-power operation condition, there is a disadvantage—reverse leakage current becomes large because of the gate bias is excessive. The authors of [11] added a second rectifying path to store excessive charges in a storage capacitor when the input power is extremely large. When the input power is not sufficient, sensor ICs are operated with the energy in the storage capacitor stored in advance. This method realized −29.0 dBm sensitivity under a 0.44 V/1.9 μA output condition. However, it is necessary to input −15.4 dBm or higher beforehand. In [12], a LC-oscillator-driven rectifier is proposed to increase the output voltage even with very low input power. A −34.5 dBm sensitivity under a 1.6 V/0.89 μA instantaneous output condition by supplying additional low DC voltage of 0.3 V is reported in this work. In [13], sensitivity was improved by using an RF–DC charge pump (CP) with 50 stages of the simplest diode-connected transistors. This work reported that a low input power of −32.1 dBm is required to obtain the output voltage 1 V for a capacitive load. The authors of [14] reported high sensitivity can be achieved with only six rectification stages by applying self-bias to the gates of rectifying transistors. Although the number of stages are not many, the area becomes large because more transistors and capacitors are needed in the bias circuit. A −30.0 dBm sensitivity is reported in this work under a 1 V output condition for a capacitive load. In [15], it is reported that high sensitivity and tolerance against temperature fluctuation and process corner variations are achieved by connecting five stages of a voltage doubler with two types of rectifying diodes. This work reports that an input power of −33.0 dBm is required to obtain the output voltage 1 V for a 1 GΩ load. Another design approach is adopting an on-chip transformer together with an on-chip rectifier [16]. With the proposed design procedure, the input impedance of the on-chip transformer can be matched with that of the antenna.

In this research, both a small rectifier circuit and high sensitivity are prioritized. The design starts with an initial assumption of a sufficiently small capacitor per stage of RF–DC CP but sufficiently large so as not to be affected by parasitic capacitance such as junction

capacitance and wring capacitance. The rest design parameters are determined one by one under the condition that the input power required to generate 1 V at the output terminal of the RF–DC CP is minimized. Section 2 shows the characteristics and schematics of rectifiers composing each stage to be optimized. Section 3 explains the optimization flow of the rectifier unit and determined optimum circuit parameters. Section 4 presents fabricated circuits and measurement results. Section 5 shows the comparison result of previous works with this work from both perspectives of area and input sensitivity. Section 6 summarizes this research.

2. Rectifying Circuits

This section explains the rectifier candidates consisting of each stage of RF–DC CP. Table 1 summarizes the circuit parameters of the rectifier. The gate width of PMOSFET is set to be twice as wide as that of NMOSFET.

Table 1. Description of parameters.

Parameter	Description	Parameter	Description
f	Frequency of input power	nf	Number of fingers of each switching transistor
V_{out}	Output voltage of RF–DC CP	C_{in}	Input capacitance per stage
l	Gate length of switching transistors	N	Number of stages
w	Gate width of NMOSFET		

Figure 2 illustrates three rectifier types considered in this research: (a) a single-diode rectifier [13], (b) a CMOS latch or cross-coupled rectifier [17], and (c) an ultra-low-power diode (ULPD) [18]. Charge pump operation is performed as follows. With CLK high and CLKB low in Figure 2a, the charges stored in the left-hand-side capacitor C_{in} are transferred to the right-hand-side C_{in}. With CLK low and CLKB high, the charges stored in the right-hand-side capacitor C_{in} are transferred to the next capacitor. Thus, the charges are transferred from one to the next every half cycle. As a result, the output voltage can be increased.

The portions enclosed by dashed lines represent one stage of the rectifiers. The CP capacitor C_{in} usually occupies a majority part of the circuit area. To have a squeezed circuit, C_{in} must be minimal. C_{in} of 100 fF is commonly assumed in this study, which is sufficiently large to disregard the impact of the parasitic capacitance such as the PN junction of switching transistors and wiring on charge transfer efficiency under low input power but sufficiently small to integrated in sensor ICs.

The single-diode rectifier has one NMOS transistor per stage, with an isolated P-well and N-well enclosing the isolated P-well connected with its source terminal together. Because of the NMOSFETs, with drain terminals that are connected with their own gate terminals in Figure 2a, a threshold voltage drop occurs per stage, which reduces the maximum attainable output voltage. To eliminate such a voltage drop at the switching MOSFETs, cross-coupled CMOS latch rectifiers were introduced. As shown in Figure 2b, the NMOSFET in the top path strongly turns on with CLK high and CLKB low, whereas the PMOSFET in the top path strongly turns off. Thus, the top capacitor is charged from the previous stage. Conversely, the NMOSFET in the bottom path strongly turns off with CLK high and CLKB low, whereas the PMOSFET in the bottom path strongly turns on. Thus, the bottom capacitor is discharged to the next stage. As a result, to turn on, the MOSFETs can operate in the linear region to eliminate the threshold voltage drop. Therefore, the CMOS latch-type rectifier is expected to have high conversion efficiency, especially in sub-threshold region operation with boosted gate voltages. The isolated P-well of NMOSFET is enclosed by the N-well of PMOSFET. Thus, those four transistors share the same N-well. A disadvantage of this rectifier type is that more transistors are needed per stage. The parasitic capacitance can be larger than the single-diode rectifier. A ULPD has one NMOSFET and one PMOSFET connected serially per stage. The PMOS gate is connected to the output terminal and the NMOS gate is connected to the input terminal, which can suppress the

reverse bias current while the forward bias current is comparable to that of the single-diode rectifier [19]. The isolated P-well of NMOSFET is enclosed by the N-well of PMOSFET. Thus, those two transistors share the same N-well.

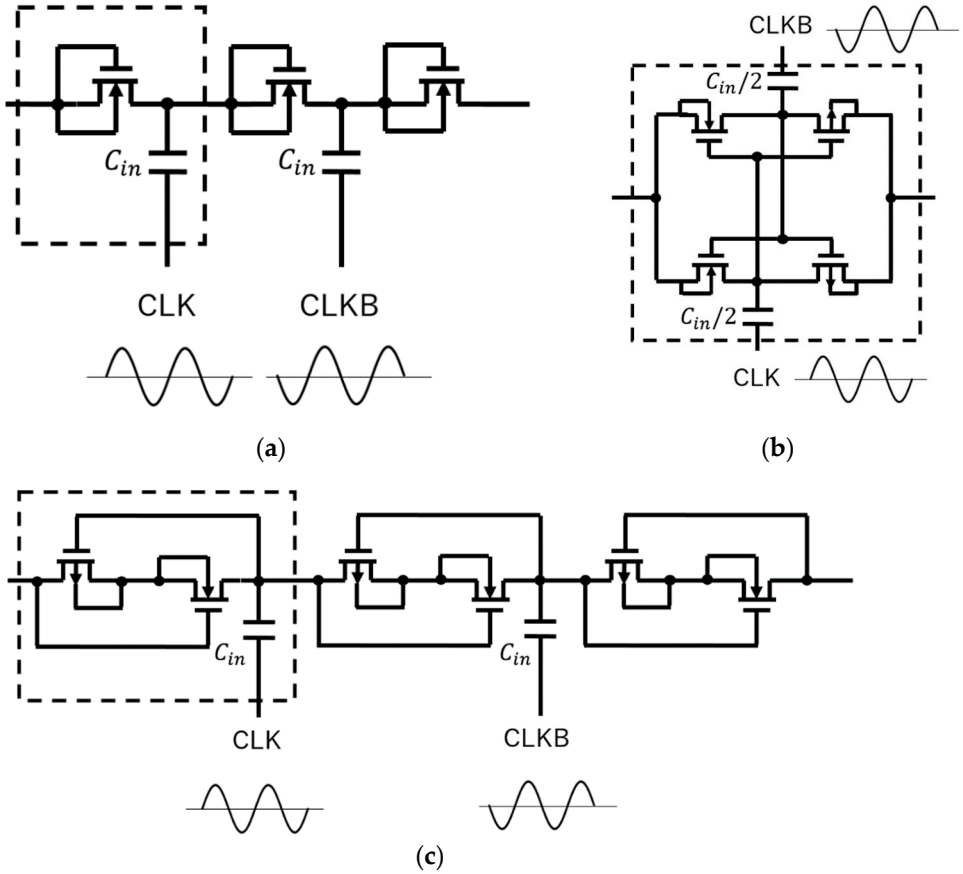


Figure 2. Schematics of (**a**) a single-diode rectifier, (**b**) a CMOS latch-type rectifier, and (**c**) an ultra-low-power diode (ULPD).

3. Optimization of Circuit Parameters and Layout Design

In this section, rectifier design parameters are determined in such a way that the input power required to generate 1 V at the output terminal of the RF–DC CP is minimized with 65 nm CMOS. The sensitivity of the rectifier is defined by the input power to achieve 100 pW at V_{out} of 1 V and f of 920 MHz in this paper. This results in $P_{in} - P_{out}$ curves with different parameter conditions at V_{out} of 1 V, as shown in Figure 3. In this example, we will call "Condition 1" optimum because its sensitivity is the lowest among the three conditions.

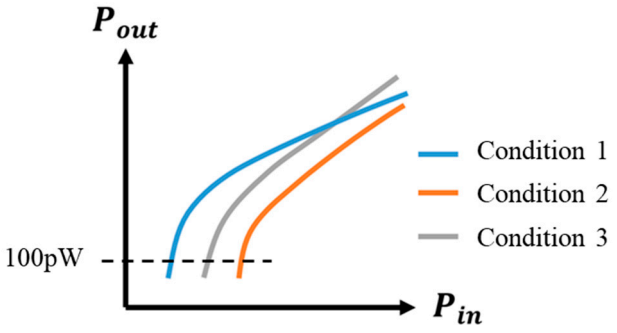


Figure 3. Determination method of the optimum parameter.

To obtain a squeezed circuit, C_{in} must be minimal. C_{in} of 100 fF is commonly assumed in this study, which is sufficiently large to disregard the impact of the parasitic capacitance of an order of 1 fF such as the PN junction of switching transistors and wires on charge transfer efficiency under low input power, but is sufficiently small to integrate in sensor ICs. Then, circuit parameters to be optimized in terms of the following: (1) transistor type, (2) threshold voltage, (3) gate width, (4) gate length, and (5) number of stages. Figure 4 illustrates a setup for SPICE simulation. The input signal source is assumed to be an ideal sinusoid with zero impedance to focus on the rectifier without antenna. The input voltage amplitude V_{amp} is swept to vary P_{in}. V_{out} is forced to DC of 1 V. P_{out} is measured per P_{in} to draw such a graph as Figure 3.

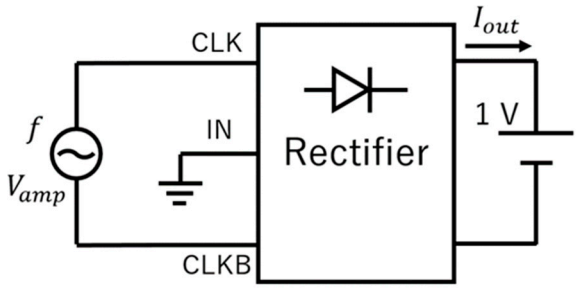


Figure 4. Schematic for SPICE simulation.

After several simulation trials, a CMOS latch-type rectifier with the optimum parameters of Table 2 is determined to have the highest sensitivity. Table 2 also includes trial values. The 65 nm CMOS provides 1 V and 2.5 V transistors. Low, standard and high V_{TH} are available for 1 V CMOS, each of which is shown by lvt, std and hvt in Table 2, respectively. When the total gate width is varied as 1.2, 10 and 20 µm, three different combinations of W and nf are used, as shown by (1), (2) and (3) in Table 2. When one of the parameters is varied, the remaining parameters are set with those of the optimum values of Table 2. $P_{in} - P_{out}$ curves for each parameter variation are shown in Figure 5. In Figure 5a, L_{min} of 280 nm is used for 2.5 V CMOS. Figure 5 indicates that P_{out} is affected by CMOS, V_{TH} and W more significantly than L, C_{in} and N, suggesting a low W/L and small C_{in} are key to achieving higher sensitivity under low input power as far as N is as many as 24 or 32.

Table 2. Optimum circuit parameters.

Parameters	Trial Values	Optimum Value
Transistor type	1 V, 2.5 V	1 V CMOS
Threshold voltage	lvt, std, hvt	lvt
l [nm]	60, 120, 240	60
w [µm]	(1) 1.2, (2) 5, (3) 5	1.2
nf	(1) 1, (2) 2, (3) 4	1
C_{in} [fF]	100, 500, 1000	100
N	16, 24, 32, 48	32

To compare the performance of RF–DC converters with different switching circuits, single diodes and ULPDs are also designed with the same design parameters, as shown in Table 2. SPICE results for $P_{in} - P_{out}$ are shown in Figure 6.

Figure 7a shows the one-stage layout of the CMOS latch rectifier. Two NMOSFETs share a common isolated P-well and four CMOS transistors share a common N-well. In this design, stage capacitors are placed outside of the transistor region. RF signal lines, as shown by CLK and CLKB, are routed with top metal over the stage capacitors to minimize the parasitic capacitance against silicon substrate. CLK/CLKB lines need to be wide enough to have sufficiently small wiring resistance. Even with careful layout design, a slight shift in the sensitivity remained, as shown by Figure 7b. Note that the impact of the parasitic elements on the sensitivity increases as P_{in} decreases.

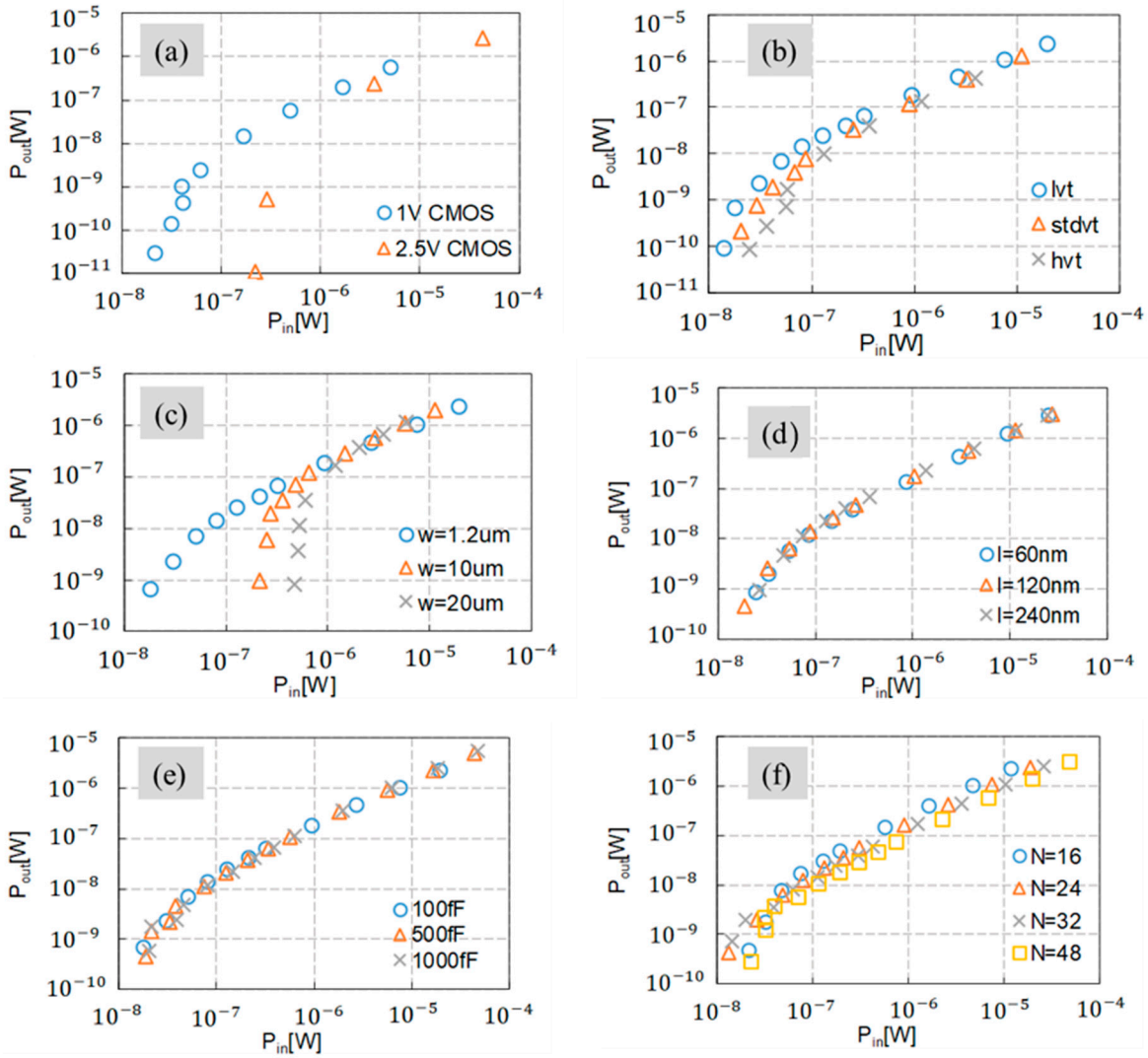


Figure 5. $P_{in} - P_{out}$ with variations of CMOS (**a**), V_{TH} (**b**), total gate width (W × nf) (**c**), L (**d**), Cin (**e**) and N (**f**).

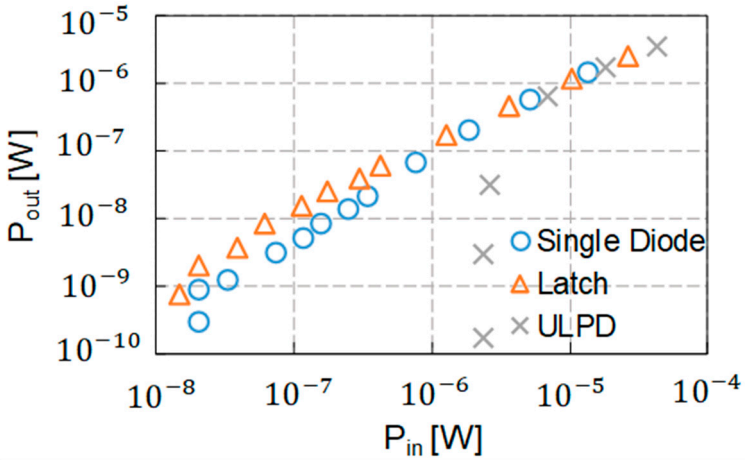


Figure 6. Comparison between rectifier candidates.

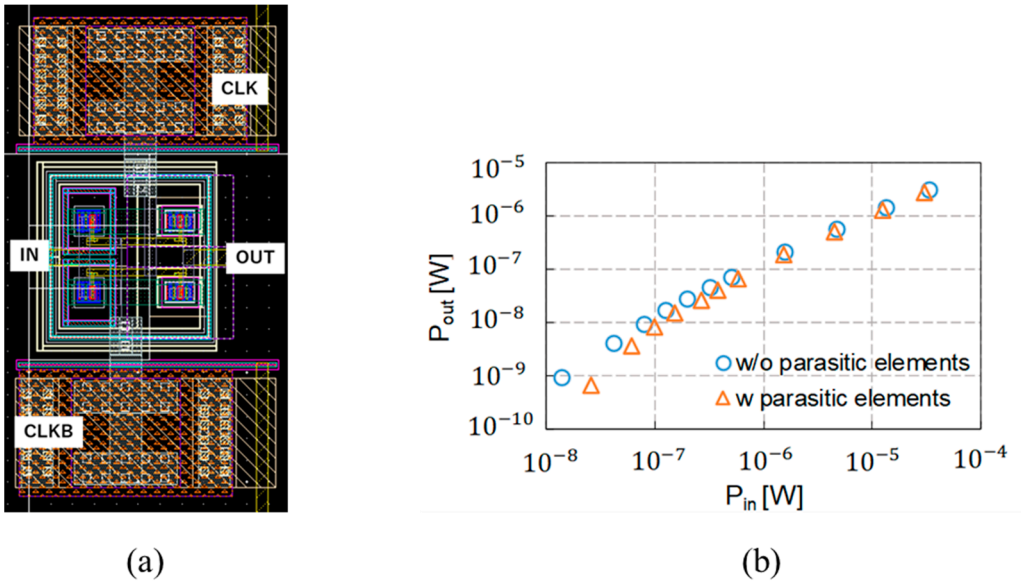


Figure 7. Stage layout of CMOS latch rectifier (**a**) and $P_{in} - P_{out}$ with and without parasitic elements of CLK/CLKB wires (**b**).

Another focus was a pad structure. With an original design [9], as shown in Figure 8a, SPICE simulation for the rectifiers with $C_{pad} - R_{sub}$ parasitic elements included showed a significant impact of R_{sub} of 6 Ω on the sensitivity, where C_{pad} is pad capacitance and R_{sub} is substrate resistance between the portion under the pad and a ground terminal. In this design, a pad structure, as shown in Figure 8b, was used. To shield the pad with ground, M1 and M2 were assigned to ground lines. To reduce the pad capacitance, M3 and M4 were left floating as dummies. As a result, the sensitivity was improved by approximately 7 dB, as shown in Figure 8b.

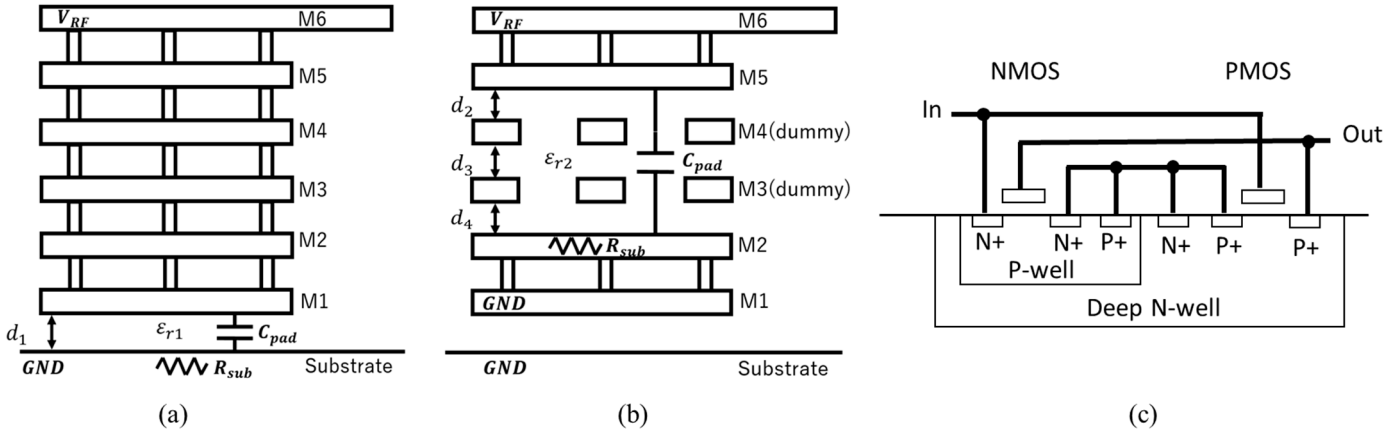
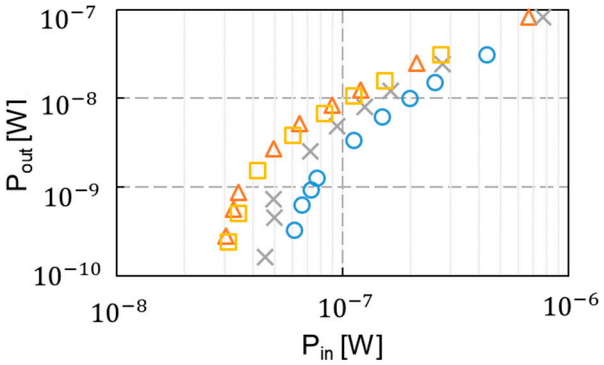


Figure 8. Cross-sectional views of the original (**a**) and revised (**b**) pads and ULPDs (**c**).

An additional simulation was performed to investigate which parameter of C_{pad} and R_{sub} was critical, as shown in Figure 9. Opt. 1 is the case where C_{pad} is as low as the proposed pad whereas R_{sub} is as high as the conventional one, and Opt. 2 is the case where C_{pad} is as high as the revised pad whereas R_{sub} is as low as the conventional one, as shown in Figure 9a. Because Opt. 2 was well matched with the case with the revised pad, it is concluded that R_{sub} is more critical than C_{pad}.

Options	○ Conv. Pad	△ Rev. Pad	× Opt.1	□ Opt.2
$C_{pad}[fF]$	234	149	149	234
$R_{sub}[\Omega]$	6	0.05	6	0.05

(a)



(b)

Figure 9. Four options (**a**) and their $P_{in} - P_{out}$ (**b**).

4. Measurement Result

Five rectifiers, as shown in Table 3, were fabricated in 65 nm CMOS. Figure 10 shows a die photo. The single-diode rectifier, the CMOS latch-type rectifier and the ULPD-type rectifier had an area of 240, 440 and 340 μm^2 per stage, respectively. If transistors and MIM capacitors were stuck, the stage area could be smaller than 200 μm^2. because capacitor area determines circuit area and the capacitor size is common to those three.

Table 3. Fabricated rectifiers.

Rectifier Name	Rectifier Type	Number of Stages
L32	Latch	32
L24	Latch	24
L48	Latch	48
S32	Single diode	32
U32	ULPD	32

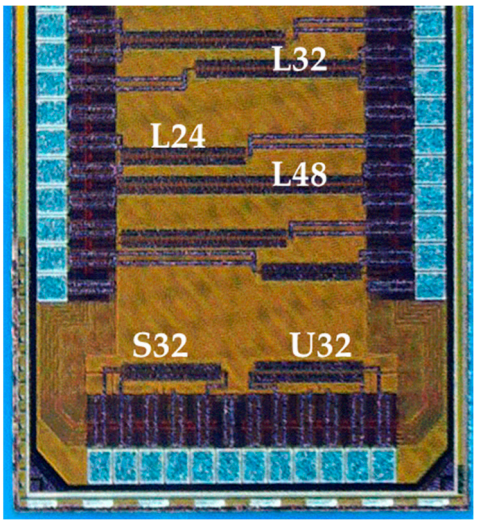


Figure 10. Die photo.

Figure 11a shows a block diagram of the measurement setup. Figure 11b shows its photo. The input power to the rectifier P_{in} is calculated based on the output power of RF generator (P_{RF}), the reflection power (P_{ref}), and loss of each of the connectors and cables [9]. Balanced–unbalanced transformation is placed on microstrip-line for rectifiers because the signal from the RF generator is an unbalanced signal.

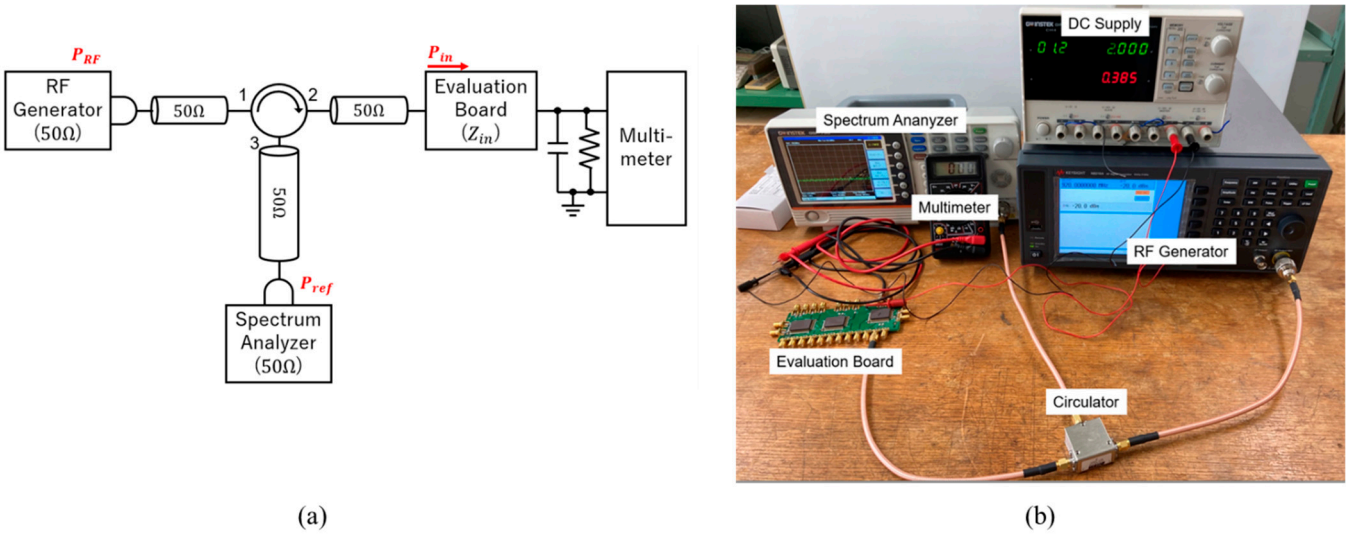


Figure 11. Block diagram of measurement setup (**a**) and its photo (**b**).

The sensitivity was measured for each rectifier at a load resistance of 10 GΩ, as shown in Figure 12. Unlike SPICE results that showed that the sensitivity of latch rectifiers is the highest, measured results showed that of ULPD rectifiers is the highest.

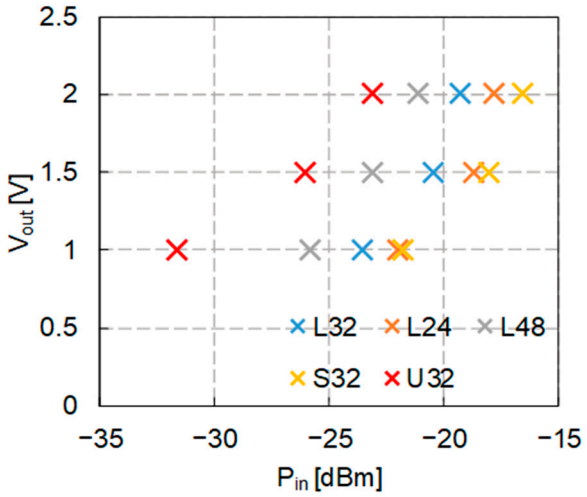


Figure 12. Sensitivity at different V_{out} with a load resistance of 10 GΩ.

To investigate the discrepancy, a more detailed netlist including parasitic elements in microstrip lines and bonding wires, as shown in Figure 13, was run. The fabricated rectifiers were measured and compared with the SPICE simulation results.

L_{ms} and C_{ms} represent the parasitic inductance and parasitic capacitance of microstrip-line, respectively. SPICE simulation was conducted with different values for L_{ms} and C_{ms} depending on the length of microstrip-line because of the length of microstrip-line on evaluation board is varied by rectifier. The parasitic inductance of bonding wire L_{BW} is estimated as 8 nH and the parasitic capacitance of bonding pad C_{pad} is 200 fF. In this SPICE simulation, the effects of wiring parasitic capacitance, parasitic resistance and well parasitic diodes of transistor were considered. Figure 14a–d compare P_{out} vs. P_{in} and η vs. P_{in} is under the condition of output voltage $V_{out} = 1\ V$.

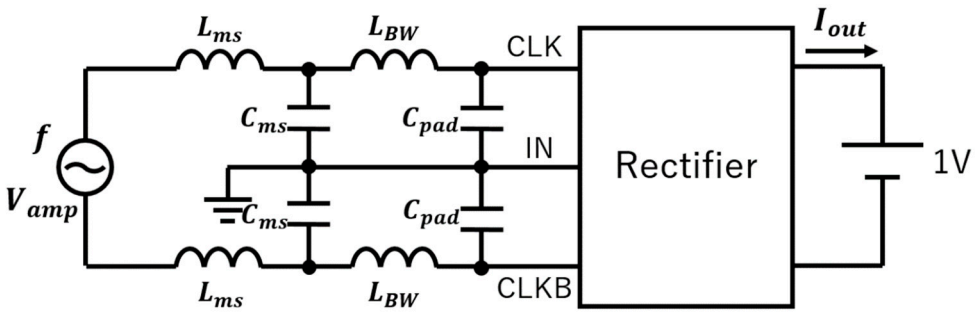


Figure 13. Schematic for SPICE simulation including parasitic elements in microstrip lines and bonding wires.

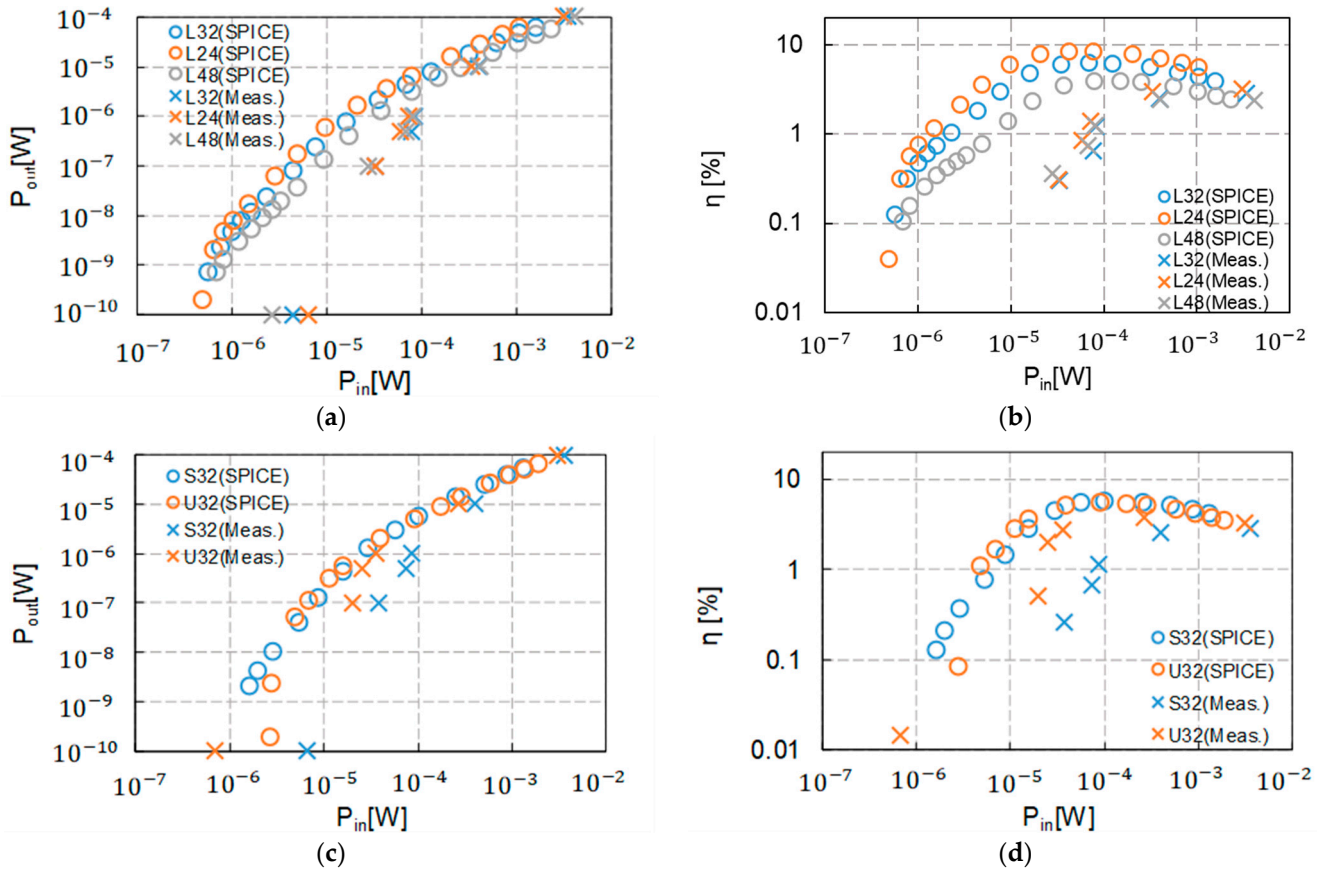


Figure 14. Comparison of input/output characteristics: (**a**) $P_{in} - P_{out}$ of L24, L32 and L48, (**b**) $\eta - P_{in}$ of L24, L32 and L48, (**c**) $P_{in} - P_{out}$ of S32 and U32, and (**d**) $P_{in} - \eta$ of S32 and U32.

Measured and simulated results are in good agreement for $P_{in} > 100$ µW or $P_{out} > 10$ µW. On the other hand, the starting points at which $P_{out} - P_{in}$ slopes become steeper are different between measured and simulated, especially in latch-type and single-diode rectifiers. We were not able to identify the root cause of the degradation. Its investigation will be needed in the future to reduce the lower bound of the input power. Table 4 summarizes the sensitivity of each rectifier. A sensitivity of −31.7 dBm was achieved with 0.011 mm^2 U32.

Table 4. Measurement result of the sensitivity of each rectifier.

Rectifier Pattern	Number of Stages	Rectifier Type	Sensitivity [dBm]	
			SPICE	Measurement
L32	32	Latch	−32.5	−23.6
L24	24	Latch	−33.2	−22.0
L48	48	Latch	−32.9	−25.8
S32	32	Single diode	−29.1	−21.8
U32	32	ULPD	−25.8	−31.7

One potential cause on the discrepancy in $P_{in} - P_{out}$ curves in the low-power region is as follows. The input impedance of the rectifiers is widely varied over input power, as shown in Figure 15. R_R and C_R are equivalent input resistance and capacitance, respectively, when the input impedance is expressed by a parallel RC circuit. In the high-input-power region, Z_{in} becomes low because C_R becomes large and R_R becomes low. In contrast, in the low-input-power region, Z_{in} becomes high because C_R becomes large and R_R becomes high. Thus, when P_{in} is swept in a wide power range, the input impedance of the rectifier largely varies. As a result, $P_{in} - P_{out}$ curves were measured without any matching circuit rather than replacing the matching circuit by P_{in} repeatedly.

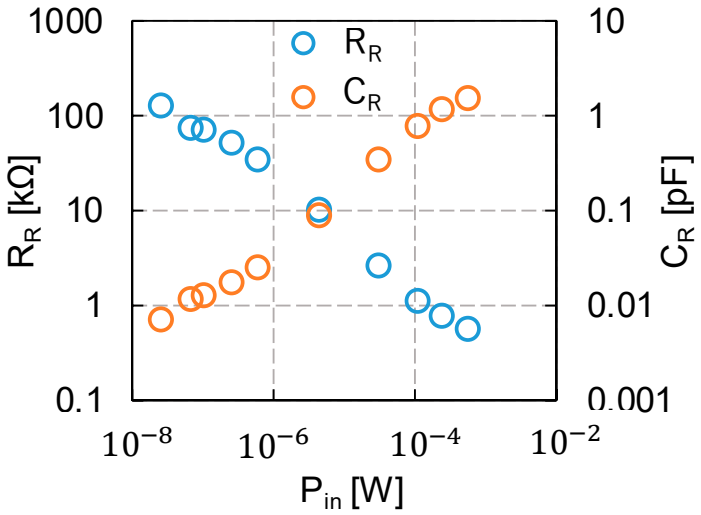


Figure 15. Input power dependence of R_R and C_R of L32.

Under a low-input-power condition, Z_{in} is far from the characteristic impedance of the coaxial cables, resulting in large reflection of power. Figure 16 explains that the ratio of the input power into the rectifier P_{in} to the output power of the RF power generator $P_{in\text{-}ic}$ depends on the reflection power $P_{ref\text{-}ic}$. As mismatch in the impedance at the interface between the connector and the rectifier increases, especially in the low-power region, $P_{in}/P_{in\text{-}ic}$ decreases significantly.

Table 5 shows the relationship between P_{in-ic}, P_{ref-ic} and P_{in} of the cases, as shown in Figure 16. Because the power resolution of the spectrum analyzer used in this research is 0.1 dB, the loss parameters extracted should have a resolution of 0.1 dB. Therefore, the discrepancy between SPICE simulation and measurement results in the low-power region can occur, as shown in Figure 14. An expected sensitivity of −31.7 dBm can be reduced to −29.6 dBm when all the loss parameters are at the worst case.

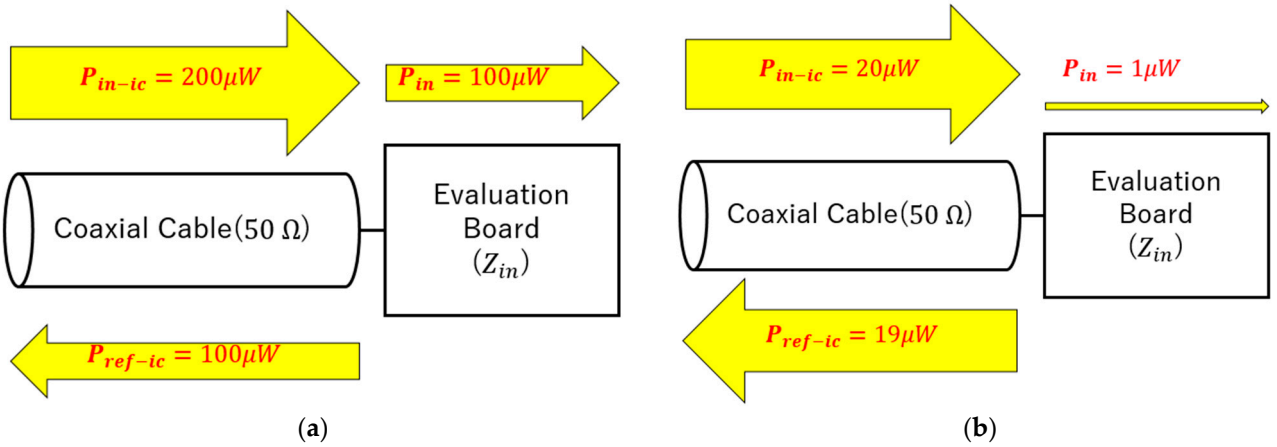


Figure 16. Difference of power reflection ratio caused by input power dependence of input impedance of the rectifier: (**a**) case of P_{in} = 100 µW; (**b**) case of P_{in} = 1 µW.

Table 5. Value of P_{in-ic} and P_{ref-ic} for each P_{in}.

P_{in} [µW]	100	1
P_{in-ic} [dBm]	−7.0	−17.0
P_{ref-ic} [dBm]	−10.0	−17.2

5. Comparison with Previous Works

This section compares the performance of the fabricated circuit with previous works in 920 MHz band. U32 achieved the highest sensitivity among the fabricated rectifiers. Comparison of this work with previous works is shown in Table 6. The comparison targets of previous works were those reported under continuous operation condition, not with intermittent operation where the ICs are driven and not driven at different times.

Table 6. Comparison with previous works.

Designs	Technology [nm]	Number of Stages	Rectifier Type	Input Signal Type	Load Condition	Area [mm^2]	Sensitivity [dBm]
This work	65	32	ULPD	Balanced	10 GΩ/1 V	0.011	−31.7
[7]	90	5	Latch	Balanced	Cap.load/1 V	0.029	−27.0
[13]	130	50	SD	Unbalanced	Cap.load/1 V	0.080	−32.1
[14]	130	6	Gate biasing	Balanced	Cap.load/1 V	0.064	−20.4
[15]	130	5	Gate biasing	Unbalanced	1 GΩ/1 V	0.02	−33.0
[16]	65	5	Latch	Balanced	Cap.load/1 V	0.28	−17.8
[19]	90	17	SD	Balanced	Cap.load/1 V	0.019	−24.0
[20]	250	36	SD	Balanced	N.A.	0.4	−22.6
[21]	300	6	SD	Unbalanced	1.5 V/0.4 µA	0.104	−14.0

Those values of area and sensitivity are plotted in Figure 17. This work achieved the smallest rectifier area and a sensitivity as close as the best candidates [15].

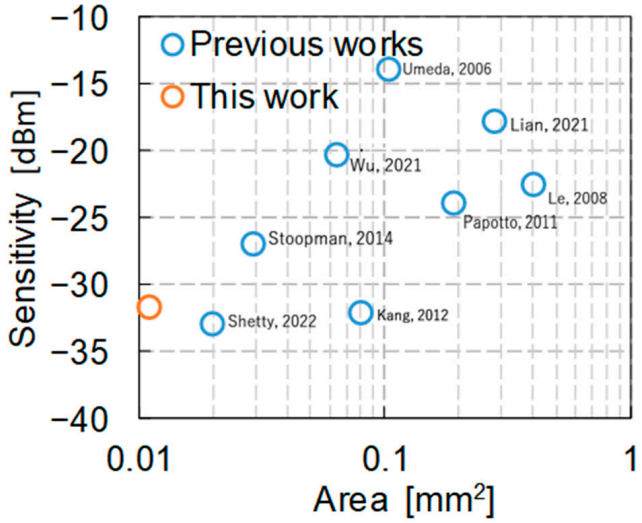


Figure 17. Comparison of area and sensitivity in this work and previous works [7,13–16,19–21].

6. Conclusions

In this work, a 32-stage ULPD rectifier in 65 nm CMOS achieved the minimum area of 0.011 mm^2 and a sensitivity of −31.7 dBm comparable to previous works. Design started with determining capacitance of a stage capacitor as small as 100 fF for a small circuit area but large enough against a parasitic capacitance of an order of 1 fF. To improve the sensitivity, the following two layout design considerations were made: (1) wide metal wires to wide boosting MIM capacitors reduced parasitic resistance in RF signal lines, and (2) a ground-shielding pad structure reduced parasitic capacitance and resistance. A CMOS latch or cross-couple rectifier was expected to be the rectifier with the highest sensitivity with SPICE, whereas a ULPD rectifier was the best one with measurement. The root cause of this discrepancy will need to be investigated in future work. More advanced technology providing MIM capacitors with a higher capacitance density and placing switching MOSFETs under MIM capacitors will further reduce the area of RF–DC charge pump rectifiers, allowing them to be integrated in sensor ICs.

Author Contributions: Conceptualization, H.N., Y.T., M.O., Y.F. and T.T.; methodology, T.H., H.N., Y.T., M.O., Y.F. and T.T.; software, T.H.; validation, T.H., H.N., Y.T., M.O., Y.F. and T.T.; formal analysis, T.H., H.N., Y.T., M.O., Y.F. and T.T.; investigation, T.H., H.N., Y.T., M.O., Y.F. and T.T.; writing—original draft preparation, T.H.; writing—review and editing, T.T.; funding acquisition, T.T. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: Data is contained within the article.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Bi, S.; Ho, C.K.; Zhang, R. Wireless Powered Communication: Opportunities and Challenges. *IEEE Commun. Mag.* **2015**, *53*, 117–125. [CrossRef]
2. Maenaka, K. Sensors in Network (5)–Future Sensor Systems in Internet of Things or Trillion Sensor Universe. *Sens. Mater.* **2016**, *28*, 1247–1254. [CrossRef]
3. Brown, W.C. The history of power transmission by radio waves. *IEEE Trans. Microw. Theory Tech.* **1984**, *32*, 1230–1242. [CrossRef]
4. Friis, H.T. A Note on a Simple Transmission Formula. *Proc. IRE* **1946**, *34*, 254–256. [CrossRef]
5. Tabuchi, Y.; Tanzawa, T. Rectenna with Serially Connected Diodes for Micro-watt Energy Harvesting. In Proceedings of the 2020 IEEE Wireless Power Transfer Conference (WPTC), Seoul, Republic of Korea, 15–19 November 2020; pp. 57–60. [CrossRef]
6. Yamazaki, Y.; Tsuchiaki, M.; Tanzawa, T. A Design Window for Device Parameters of Rectifying Diodes in 2.4 GHz Mi-cro-watt RF Energy Harvesting. In Proceedings of the 2019 IEEE Asia-Pacific Microwave Conference (APMC), Singapore, 10–13 December 2019; pp. 135–137. [CrossRef]

7. Stoopman, M.; Keyrouz, S.; Visser, H.J.; Philips, K.; Serdijn, W.A. Co-Design of a CMOS Rectifier and Small Loop Antenna for Highly Sensitive RF Energy Harvesters. *IEEE J. Solid-State Circuits* **2014**, *49*, 622–634. [CrossRef]
8. Falkenstein, E.; Roberg, M.; Popović, Z. Low-Power Wireless Power Delivery. *IEEE Trans. Microw. Theory Tech.* **2012**, *60*, 2277–2286. [CrossRef]
9. Hashimoto, T.; Tanzawa, T. Design Space Exploration of Antenna Impedance and On-Chip Rectifier for Microwave Wireless Power Transfer. *Electronics* **2022**, *11*, 3218. [CrossRef]
10. Kotani, K.; Ito, T. Self-Vth-Cancellation High-Efficiency CMOS Rectifier Circuit for UHF RFIDs. *IEICE Trans. Electron.* **2009**, *E92-C*, 153–160. [CrossRef]
11. Safarian, Z.; Hashemi, H. A Wirelessly-Powered Passive RF CMOS Transponder with Dynamic Energy Storage and Sensitivity Enhancement. In Proceedings of the 2011 IEEE Radio Frequency Integrated Circuits Symposium, Baltimore, MD, USA, 5–7 June 2011; pp. 1–4. [CrossRef]
12. Kang, J.; Chiang, P.; Natarajan, A. Bootstrapped Rectifier-Antenna Co-Integration for Increased Sensitivity in Wirelessly-Powered Sensors. *IEEE Trans. Microw. Theory Tech.* **2018**, *66*, 5031–5041. [CrossRef]
13. Oh, S.; Wentzloff, D.D. A −32dBm sensitivity RF power harvester in 130 nm CMOS. In Proceedings of the 2012 IEEE Radio Frequency Integrated Circuits Symposium, Montreal, QC, Canada, 17–19 June 2012; pp. 483–486. [CrossRef]
14. Wu, Z.; Zhao, Y.; Sun, Y.; Min, H.; Yan, N. A Self-Bias Rectifier with 27.6% PCE at −30dBm for RF Energy Harvesting. In Proceedings of the 2021 IEEE International Symposium on Circuits and Systems (ISCAS), Daegu, Republic of Korea, 22–28 May 2021; pp. 1–5. [CrossRef]
15. Shetty, D.; Steffan, C.; Bösch, W.; Grosinger, J. Sub-GHz RF Energy Harvester including a Small Loop Antenna. In Proceedings of the 2022 IEEE Asian Solid-State Circuits Conference (A-SSCC), Taipei, Taiwan, 6–9 November 2022; pp. 1–3. [CrossRef]
16. Lian, W.X.; Ramiah, H.; Chong, G.; Kishore Kumar, P.C. A Differential RF Front-end CMOS Transformer Matching for Ambient RF Energy Harvesting Systems. In Proceedings of the 2021 IEEE Asia Pacific Conference on Circuit and Systems (APCCAS), Penang, Malaysia, 22–26 November 2021; pp. 133–136. [CrossRef]
17. Gariboldi, R.; Pulvirenti, F. A 70 mΩ Intelligent High Side Switch with Full Diagnostics. *IEEE J. Solid-State Circuits* **1996**, *31*, 915–923. [CrossRef]
18. Levacq, D.; Liber, C.; Dessard, V.; Flandre, D. Composite ULP diode fabrication, modelling and applications in multi-Vth FD SOI CMOS technology. *Solid-State Electron.* **2004**, *48*, 1017–1025. [CrossRef]
19. Papotto, G.; Carrara, F.; Palmisano, G. A 90-nm CMOS Threshold-Compensated RF Energy Harvester. *IEEE J. Solid-State Circuits* **2011**, *46*, 1985–1997. [CrossRef]
20. Le, T.; Mayaram, K.; Fiez, T. Efficient Far-Field Radio Frequency Energy Harvesting for Passively Powered Sensor Networks. *IEEE J. Solid-State Circuits* **2008**, *43*, 1287–1302. [CrossRef]
21. Umeda, T.; Yoshida, H.; Sekine, S.; Fujita, Y.; Suzuki, T.; Otaka, S. A 950-MHz Rectifier Circuit for Sensor Network Tags With 10-m Distance. *IEEE J. Solid-State Circuits* **2006**, *41*, 35–41. [CrossRef]