A Calibration Technique of Capacitor Mismatch for Pipelined Analog-to-Digital Converters

2004

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This thesis describes a digital calibration technique of capacitor mismatch in pipelined A/D converters (ADC's) and CMOS chip implementation of the proposed calibration circuits.

In high-speed low-power ADC design, a main source of the non-linearity error in pipelined ADC's is the capacitor mismatch in multiplying digital-to-analog converter, especially if relatively small capacitors are used. Due to extra analog hardware for error measurements in the ADC core, the previous calibration methods may degrade the analog performances.

This work proposes a new digital calibration technique, which does not need to incorporate the error measurement circuits in the ADC core. In the proposed method, capacitor mismatch errors of the pipeline stage are estimated using an integral non-linearity (INL) plot for a ramp signal. The capacitor mismatch errors are estimated by an analytical relationship between the total error power of the INL and the mismatch error. Algorithms of the proposed method are developed for redundant radix-2 pipelined ADC's and redundant radix-4 pipelined ADC's.

The proposed calibration method is applied to two implemented chips; a redundant radix-2 10-bit pipelined ADC, and a redundant radix-2 parallel pipelined ADC. In these implementations, this method can reduce the maximum INL within 0.3LSB. The proposed method is also applied to a 14-bit radix-4 parallel ADC, and it is shown that the error correction logic can be implemented in $0.3 \times 9mm^2$ with 0.13μ m CMOS technology.