Study on SOI technologies for high performance MOSFETs

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This paper describes research in materials, processing, and device technologies for silicon-on-insulator (SOI) Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). SOI technology is promising for nanometer-scale MOSFETs, because the SOI structure reduces depletion capacitance in the channel region, which improves the electrical characteristics of devices. Even though the SOI technology has been studied for a long time, further refinement is still needed.

First, flattening process during annealing at Si-SiO2 interfaces was analyzed. The morphologies were observed at the Si-SiO2 interfaces by using the atomic force microscope, and a model, which described the interface flattening process precisely, was proposed. The time-dependent differential equation in the proposed model agreed well with the observed results.

A model of dopant redistribution during annealing was proposed to obtain the precise dopant profile in the SOI structure. The model allows the precise estimation of the threshold voltage of the SOI MOSFET.

The electrical characteristics of power devices by using SOI structure was also investigated. The author proposed a new structure of the SOI power device, and improved the electrical characteristics compared to those of the conventional structure.

As a result, the author has successfully refined material, processing, and device technologies for the SOI structure, which nowadays is used in the nanometer-scale MOSFETs.