Study on thermal instability of thin SOI layers for application to quantum dot devices

2003

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Silicon-on-insulator (SOI) structures with a thin top-Si-layer (<30 nm) are useful for the formation of future Si nano-structure devices such as single electron transistors (SETs) as well as metal-oxide-semiconductor field-effect-transistors with high-speed operation and low power consumption. However, such a thin Si layer is thermally unstable, which is a crucial problem for the device fabrication process. The purpose of this work is to investigate the thermal behavior of ultrathin single-crystalline Si (100) layers on SiO^2 using SOI substrates fabricated by our original method. Then, based on the result, the fabrication of SETs and field emitter (FE) devices with single-crystalline Si dots are proposed and realized.

It was found, for a Si layer with a thickness below 30 nm, that by annealing in an ultrahigh vacuum, the Si layer agglomerates and a number of Si islands with a sub-micrometer scale are formed on the amorphous SiO2 with an ordered alignment in the <310> directions. A model based on both surface energy and strain energy can explain the island formation and ordering phenomena. It is also found that the agglomeration readily starts to occur at a low temperature. For example, a Si layer below 10 nm thick agglomerates even at 900-1000℃. Avoiding the agglomeration, I successfully fabricated SETs and FE devices with high-density Si dots. The SETs remarkably show transistor characteristics, and they depend on the thickness of the connecting region between dots. For FE devices, I proposed a fabrication process and clarified the emission property of a protrusive Si nano-structure.

In summary, I clarified the thermal stability of the thin Si layer and successfully fabricated the Si devices with single-crystalline quantum dots.