R-2R Ladder Digital-to-Analog Converters

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Because of the small device count and the simple configuration, the R-2R ladder digital-to-analog(DA) converter is quite attractive to mixed analog and digital application-specific integrated circuits(ASICs). CMOS process is exclusively used for ASIC implementation. Therefore, the R-2R architecture suited for CMOS ASICs is exploited in this study.

One of the issues in CMOS ASICs is the power consumption. The R-2R architecture is first analyzed in terms of the power consumption, to point out that the current-mode is best suited for low power operation. The error sources associated with the current-mode R-2R ladder DA converter are resistance mismatches, switch on-resistances, and wire resistances between the ladder stage and the output terminals. The integral nonlinearities(INL) due to these error sources are then analyzed to identify the error source. Voltage and current measurements are also presented to characterize the R-2R ladder.

These characterization methods are applied successfully to the 8-bit DA converters fabricated using 0.6 μm CMOS process. The R-2R ladder consists of nMOS transistors operating in the linear region. Measured performances compared with the INL analyses indicate that the dominant error source is the wire resistance and that the INL of the ladder stage is 1.2 LSB.

The DA converter is also applicable to the multiplier and the digitally programmable attenuator. The analog bandwidth and the total harmonic distortion in these applications are 220 MHz and 0.1%, respectively. The R-2R ladder DA converter described in this thesis is therefor quite useful for a building block of the current-mode signal processing system.