A Study on High-speed Low-power parallel pipeline A/D converters.

2002

Daisuke Miyazaki

This thesis describes high-speed low-power parallel pipeline A/D converters(ADC's) and its design method to embed it into mixed analog-digital system LSI's.

For low-power pipelined ADC design, this work proposed a new low-power single-ended amplifier using a dynamic-biased ragulated cascode scheme, a pseudo differential architecture and a capacitor cross-coupled sample-and-hold(S/H) stage. The proposed pseudo differential scheme allows us to realize the power supply rejection and tolerance to cross-talk noise from digital circuits, as well as its low power characteristic. A capacitor cross-coupled sample-and-hold(S/H) stage has a high input bandwidth with reduced power. A 10bit 30MSample/s pipeline ADC chip using the proposed techniques is implemented and features about 16mW power consumption at the supply voltage of 2V. The archived low-power performance is superior to other high-speed 10b ADC's reported.

As a low-power design method for very high-speed ADC's whose sampling freauency exceeds 100MHz, this work proposed a new design method based on a model to express the relationship between the sampling frequency and the power dissipation. Parameters of architecture level and circuit level are totally optimized using a cost function given by the power and the area. This work also points out that the interleaved pipeline structure is very effective for low-power design of high-speed A/D converters whose sampling frequency is over 100MHz.

A 10bit, 200MSample/s parallel pipeline ADC is designed and the estimated power dissipation is less than 100mW at 1.8V power supply.