Acceleration techniques for constructing a large-scale circuit simulator

1999

Nobuyuki Tanaka

High-speed large-scale circuit simulators are needed for designing large-scale circuits, such as high-speed LSI chips and printed circuit boards. This thesis describes a dedicated parallel processor and two high-speed relaxation algorithms for constructing a high-speed large-scale circuit simulator. The waveform relaxation algorithm is used to partition the circuit into sub-circuits, and iterative timing analysis is used to partition the sub-circuits into smaller sub-circuits. These smaller sub-circuits are then analyzed by the direct method, which can stably solve a circuit equation. The dedicated parallel processor is used to adapt the direct method to a large-scale circuit.

This thesis is organized as follows. In chapter 1, I explain the need for large-scale circuit simulators. In chapter 2, I explain the software I used to develop the circuit simulator. I describe the proposed processor, called SMASH, in chapter 3 and evaluate the performance of a large-scale circuit simulator constructed using SMASH in chapter 4. SMASH has a special architecture for decomposing a large-scale sparse circuit matrix. A piecewise-linear diode model constructed using an ideal switch and resistros is used to reduce the model evaluation time. This model is described in chapter 5. The iterative timing analysis using the overlapped partitioning, called overlapped block relaxation newton(OBRN) method, is described in chapter 6. In the OBRN method, the nodes at the border of each sub-circuit are contained in adjacent overlapped blocks. The OBRN method is 10 to 1000 times faster than the conventional iterative timing analysis. The waveform relaxation algorithm is described in chapter 7. Its calculation time is reduced by using local iteration and window partitioning. The thesis concludes with a summary and look at future workd in chapter 8.