A study of current-mode signal processing circuits

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The performance of switched-current (SI) memory cells is dependent largely on clockfeedthrough (CFT). To reduce CFT errors, a fully-differential first-generation SI circuit is proposed. The residual CFT error is 0.025% for the input signal current ranging from -20 μ A to 20 μ A.

The CFT compensation method in second-generation SI memory cells is also proposed and applied to S^2I or S^nI cells. The method is based on the cancellation of the CFT error component in the SI memory cell by the current generated by another cell. Simulations show that the proposed technique attenuates the CFT component of the S^2I memory cell more than 60 dB and the residual CFT error of S^2I and S^nI cells are 0.002% and 0.004%, respectively, for the input signal current ranging from -180 μ A to 180 μ A.

An algorithmic AD converter using CFT compensated two-step S^2I memory cells is proposed. It accepts the input signal current twice as large as the reference current, and is suited to meet the requirement of a wide dynamic range with low power consumption. Simulations show that a conversion accuracy higher than 13-bit and a conversion rate up to 1.14 Mbps are attainable with the power dissipation less than 10mW.

Novel CMOS class A and class AB second-generation current conveyors (CCII) for wideband current-mode signal processing are also developed. In these architecture, the two input stages are coupled by current mirrors to reduce the current input impedance. Simulations show that the unity-gain bandwidth of the two CCIIs extend beyond 100MHz and THD of class AB CCII is less than 1% over the frequency range from DC to 10MHz.

Therefore, the CFT compensated SI cells, the AD converter, and the CCIIs proposed in this thesis are quite useful for current-mode versatile building blocks.