Physics and Technology of High Performance and Functional MOS Power Devices

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The thesis describes physics and technology of high performance and functional MOS power devices intended to realize low dissipation and destruction-free power device.

CONCAVE-DMOSFET, New current sensing function, ASPT(Avalanche-suppressed punch-through)-IGBT, and SiC vertical MOSFET were proposed by the author. Device physics and fundamental process of these devices were feasibly studied by computer simulation. Fabrication and evaluation technologies were developed for each device, especially stressed on the MOS gate structure and characteristics.

The CONCAVE-DMOSFET ashieved the lowest specific on-resistance of 75m $\Omega \cdot mm^2$ under 50V blocking and 16μ m cell design. LOCOS-based new process realized coexistence high channel mobility with elimination of neck resistance.

The new current sensing function, of which the sensing principle is monitoring voltage drop through the channel resistance, and lateral DMOSFET, which operates as a temperature compensation resistor, were monolithically integrated into the DMOSFET chip. Deviation of the sensitivity was within$\pm$2%(-40~125℃), resulting in high accuracy.

The ASPT-IGBT was designed and fabricated with taking account of drain breakdown not by avalanche but by minority carrier injection at substrate p^+/n^-junction. Destruction energy against drain surge of ASPT-IGBT was 1.6 times larger than that of conventional NPT(Non punch-through)-IGBT, whith is good agreement with the reciplocal maximum power density ratio of the two devices.

Application of SiC material to MOS power devise was feasibly studied. Anisotropy in thermal oxidation of 6H-SiC was found out and preferrably applied to new vertical MOS structure achieving coexistence high blocking voltage with low threshold voltage. Fabricated SiC vertical MOSFET operated in normally off mode with 250V blocking, showing possibility of high voltage SiC power MOSFET.

The physics and technology written in the thesis provide a chart for promoting high performance and functional MOS power device development.