A Study on Switched-capacitor Analog-to-Digital Converters

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With the advance in CMOS VLSI technologies, digital processing of an analog signal in a mixed analog and digital ASIC form is now prevalent. A key to integrate such an ASIC from is now prevalent. A key to integrate such an ASIC successfully is an analog-to-digital (A/D) converter for interfacing the real analog world with the digital world of signal processing. The purpose of this study is to develop the A/D converters which can be integrated onto a small chip area and operate with the small power consumption.

Accuracy of A/D converters using switched-capacitor techniques is limited by nonideal effects of components involved. To solve such problems, switched-capacitor circuits are developed to compensated for the nonideal effects. These circuits can suppress the clock-feedthrough charge, and are also insensitive to parasitic capacitances and offset voltage of an op-amp or a unity-gain buffer (UGB) used for the arithmetic operation. Successive-approximation, cyclic, and pipeline A/D converters described are composed, based on these circuits.

First, successive-approximation A/D converters are presented which incorporates a serial digital-to-analog (D/A) converter. Error analyses and SPICE simulations show that a conversion accuracy higher than 11 bits, a sampling rate up to 50 ksps (sample per second) with 10-bit resolution are attainable with the monolithic implementation using present CMOS technologies.

Second, cyclic A/D converters, especially op-amp's gain-insensitive converter, are described. It consists of three 1-bit quantizers connected in a loop. Error analyses and SPICE simulations show that a conversion accuracy higher than 12 bits and sampling rate up to 380 ksps are attainable with the CMOS monolithic implementation.

Third, a 1-bit quantizer using UGB, a pipeline A/D converter connecting the quantizer in cascade, and a cyclic A/D converter consisting of the two 1-bit quantizers in a loop, are described. Error analyses and SPICE simulations show that a conversion accuracy higher than 10 bits and sampling rate up to 10 Msps for the pipeline architecture are attainable with the monolithic implementation.

The higher sampling rate will be possible using finer linewidths. The A/D converters described herein are suited for signal processing in a facsimile and for the interfaces of the sensors.