Study on Unipolar-type Static Induction Transistors with a High-purity Region

March, 1993

Koji Yano

When a high-purity semiconductor material of low doping concentration, comparable to an intrinsic carrier concentration, is used for the channel region of the static induction transistor (SIT), a large accumulation area of majority carriers is formed in the channel region near each of the source and drain junctions. In this thesis, in order to develop new SITs using the accumulation effect, a two-dimensional simulation is carried out. The simulation has made it clear that the operational mechanism of the SIT having the high-purity channel is dominated by the current transport by the accumulated carriers, different from the conventional SIT with the channel of relatively large doping concentration. In order to use this current transport efficiently, a new normally-on SIT having the high-purity channel in which the p^+ gate region is shielded by a thin n layer, called a "shielded gate SIT", has been proposed. The comparison of the electrical characteristics of the shielded gate SITs with those of the conventional SITs has proved the large gate controllability of the high current due to the accumulated carriers for the shielded gate SITs. Optimum design methods of the shielded gate SIT have been obtained by evaluation of its static and high-frequency characteristics. Moreover, it has been shown that the introduction of the backgate region into the high-purity channel MOSSIT can realize a normally-off unipolar SIT operation with the transport of the accumulated carriers. The optimization of the gate-backgate length is an effective approach to fabricate high-power and high-frequency MOSSITs. Optimum backgate structures and effects of a backgate bias are also insighted.