A Study on Switched-Capacitor Date Converters

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The purpose of this thesis is to develop switched-capacitor analog-to-digital (A/D) converters in instrumentation and measurement field.

First, a novel floating-point A/D converter has been developed based on the dual-slope integration. This converter increases the resolution and the conversion speed.

The dual-slope and charge-balancing A/D converters requires 2^N clock cycle for N-bit resolution. To improve the conversion speed, an integration-type high-speed A/D converter has been developed. The conversion process consists of the charge-balancing A/D conversion to determine the upper M bits of an N-bit resolution and subsequent single-slope conversion to determine the remaining lower N-M bits. The speed improvement as high as $2^{(N/2)-1}$ times is possible when M=N/2.

The cyclic A/D conversion is faster than the integration conversion and acquires medium resolution. A switched-capactor cyclic A/D converter has been proposed using analog arithmetic and sample/hold circuits. The whole operation is insensitive to offset voltages of op amps and parasitic capacitances.

The method for improving the conversion accuracy of conventional A/D converters is proposed. The triangular wave superposed on the analog input signal is sampled and the resultant digital outputs are averaged.

Furthermore,signal processing circuits for capacitive sensors based on the switched-capacitor cyclic and floating-point A/D converters are presented. Their digital output capability and fabrication process compatible with IC sensors are best suited for the built-in interfaces of intelligent capacitive sensors.