Study of Circuit and Monolithic Integration Technologies for Grading-up The Operation Speed and Repeater Spacing of Digital Optical Transmission Systems

Kiichi Yamashita

February, 1987

Wideband analog/high-speed digital circuit techniques and monolithic integration technology have been developed for grading-up the capacity and repeater spacing of digital optical transmission systems. Two line coding schemes were also developed to ensure the stable operation of optical repeaters against any long period pattern transients. Major attained results were summarized as follows.

1) As line codes, two-level alternate mark inversion and modified duobinary codes were proposed and the stable operation of fabricated optical repeaters against long period pattern transients, for example, a 1/12-11/12 mark ratio variation with a 8 ms period was ensured by introducing these line codes.

2) A simple resistor-capacitor circuit which can grade-up three times the modulation speed of light emitting diode (LED) was proposed and LED transmitter operating at 400 Mb/s or more can be realized by using this new circuit.

3) A preamplifier with a variable transimpedance and a 3-stage gain control method using this preamplifier were proposed to expand optical dynamic range of repeaters. As a result, a 1.55 μm 565 Mb/s monolithically integrated optical repeater with a 33.2 dB optical dynamic range was implemented, which is about 10 times superior in the dynamic range to convetional repeaters.

4) A 2-mode frequency divider with a direct feedback logic configuration was proposed to grade-up the function and operation speed of timing circuit for multiplexer/demultiplexer and monolithically integrated by using 3 μm Si-bipolar IC technology. Consequently, it was confirmed that the proposed frequency divider is abont 2 times superior in operation speed to conventional frequency divider.