Fine Pattern Device Isolation Technology for VLSI process

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In this paper, fine pattern device isolation technology, which will become an important VLSI process in the future, has been studied. The intention is to propose and evaluate a novel isolation structure, based on fine pattern formation and selective silicon epitaxial growth. The fine pattern is formed by an anisotropic dry etching method. It was found that Si etching profiles and selectivities over SiO_2 were affected by reactive gases for a reactive ion etching (RIE). That is, SF_6 gas had isotropic pattern profiles and CCl_3F gas had anisotropic profiles. Also, $SiCl_4$ gas showed excellent profiles with carbon contaminations, as is was long as used in controlled vacuum.

Selective epitaxial growth (SEG) of Si was achieved under 50 Torr pressure using SiH_2-Cl_2-H_2-HCl gas system. The defect density and facet formation markedly depended on growth conditions, sidewall materials and pattern side direction. The electrical characteristics for MOSFETs, which were fabricated on the SEG layer surrounded with SiO_2 film were induced to fine pattern isolation potentiality and less narrow channel effect.

Finally, the SEG isolation technology were applied to scaled CMOS process. A buried well was formed by an ion implantation before the SEG process. High latchup immunity was obtained by low well resistance and isolation geometries with high aspect ratio. It was confirmed that the SEG isolation could solve severe problems for the scaled CMOS. The fine pattern formation and device isolation technology are promising for future VLSI fabrication.