Novel Solid-State Imaging Devices with Inherent MNOS Memory Gate

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This dissertation describes novel solid-state imaging devices with inherent MNOS memory gate which is capable of signal processing on the image plane.

For the purpose of clarifying the optical writing operation, optical writing model is established by extending the operation theory of an MNOS capacitor developed by Chang and Lundström et al. The model is confirmed by the experimental results. It is found that a bias charge transferred into the MNOS memory capacitor from photodiode, in addition to the signal charge is important to improve the writing of the low light inputs. Both enhanced writing and wide dynamic range are obtained under the following optimum bias condition: a preset photodiode voltage of 5V, a memory pulse voltage of 35V amplitude, and a 1-10 μs duration. Moreover, it was found that the stored charge signal could be nondestructively readout from drain output under a given bias light, provided the drain voltage V_D was biased higher than the surface potential ϕ_{MG} below the memory gate. If $V_D < \phi_{MG}$, however, incoming light signals are detected regardless of shifts in the flat-band voltage optically induced during the writing process. The reproduced images of readout and incoming light signals are demonstrated using a 5×5 2-D array.

A simple model is also developed which is capable of predicting the product of incoming irradiance and the flat-band voltage shift of the memory gate, which is proportional to the exposing light signal in the previous write cycle. Preliminary experimental results are presented which confirm the model. The optical multiplication feature leads to a real-time two-dimensional image processor through through which spatial convolution or correlation can be obtained.