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A Clock-Feedthrough and Offset Compensated Fully-Differential Switched-Current Circuit

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SUMMARY A fully-differential switched-current (SI) circuit provided with clock-feedthrough (CFT) and common mode rejection and offset compensation schemes is described. Different from a conventional SI memory cell, it takes the difference between two differential inputs to deliver the balanced differential currents. Transistor level simulations and error analyses are given to demonstrate its performance.

key words: *fully-differential switched-current circuit, SI memory cell, clock-feedthrough*

1. Introduction

The clock-feedthrough (CFT) and common mode rejection (CMR) of interference signals and the offset compensation are essential when switched-current (SI) circuits are used for high accuracy analog signal processing in noisy digital environments. Many schemes are proposed for such a task [1]-[3], but the most promising candidate is the fully-differential structure. However, the fully-differential structures proposed so far are limited only to the SI memory cells which deliver the delayed replicas of balanced differential input currents [4], [5].

As known from switched-capacitor circuit experience, a substantial rejection of all error factors including the power rail fluctuation is possible only when the circuit has a truly differential architecture which takes the difference between two balanced inputs to deliver the balanced outputs.

This letter describes such an architecture designed based on the CFT-compensated memory cell.

2. Circuit Description and Operation

Figure 1 shows the circuit diagram of the memory cell used for the fully-differential SI circuit. The cell is designed based on the conventional circuit [1], but the circuit configuration is modified such that the output current has the same polarity as the input and that the CFT cancellation can be realized with the smaller current-mirror ratio. In the cell, the CFT error is caused by the capacitive coupling of the clock signal ϕ through parasitics and the charge transfer from the switch transistor channels to the gate capacitances of the memory transistors. In a first-order approximation, the error voltage is inversely proportional to the gate capacitance [6]. Let the CFT voltage at the gate of M_1 be V_c. The CFT vlotages V_{CFT2} and V_{CFT3} appearing at the gate of M_2 and M_3, respectively, when M_{S1} and M_{S2} are turned off are then represented by

$$V_{CFT2}=V_C/\alpha_1, \tag{1}$$

$$V_{CFT3}=V_C/\alpha_2, \tag{2}$$

where the current-mirror ratios α_1 and α_2 are assumed realized by scaling the gate widths of M_2 and M_3 appropriately. The CFT voltages given by (1) and (2) are superposed upon the gate voltages stored in the preceding phase, and thus $v_{GS2}=v_{GS1}-V_C/\alpha_1$ and $v_{GS3}=v_{GS1}-V_C/\alpha_2$. Assuming that all transistors except the switches operate in the saturation region and the channel length modulation is negligible, the drain currents can be written as

$$i_{D1}=J+i_{in}=\frac{\beta_1}{2}(v_{GS1}-V_T)^2, \tag{3}$$

$$i_{D2}=i_{D4}=i_{D5}=\alpha_1(J+i_{in})$$
$$=\alpha_1\frac{\beta_1}{2}\left(v_{GS1}-V_T-\frac{1}{\alpha_1}V_C\right)^2, \tag{4}$$

$$i_{D3}=\alpha_2(J+i_{in})=\alpha_2\frac{\beta_1}{2}\left(v_{GS1}-V_T-\frac{1}{\alpha_2}V_C\right)^2, \tag{5}$$

where J is the bias current, $\beta_1=\mu C_{OX}(W/L)_1$, and $V_{T1}=V_{T2}=V_{T3}=V_T$ is assumed. The output current is then given by

$$i_{out}=i_{D5}-i_{D3}-(\alpha_1-\alpha_2)J$$

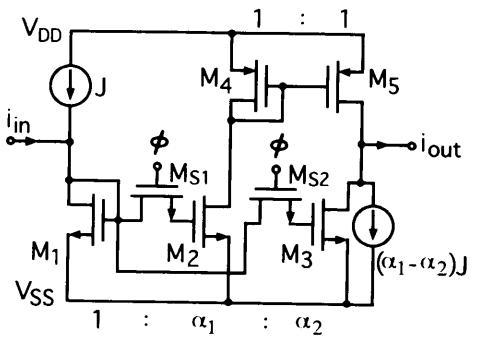

Fig. 1 Circuit diagram of the SI memory cell.

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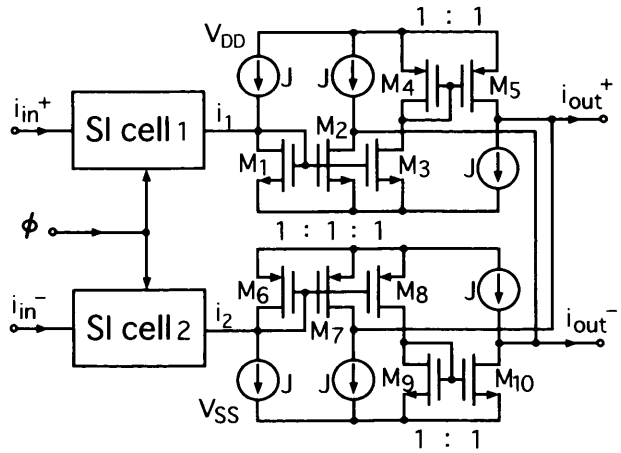

Fig. 2 Proposed fully-differential SI circuit.

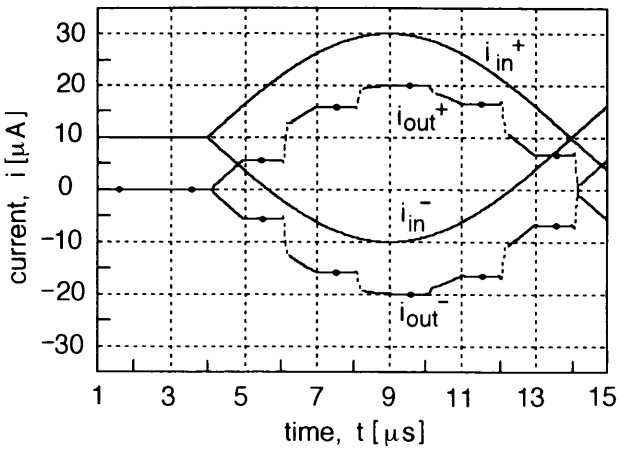

Fig. 3 Simulation results of output currents.

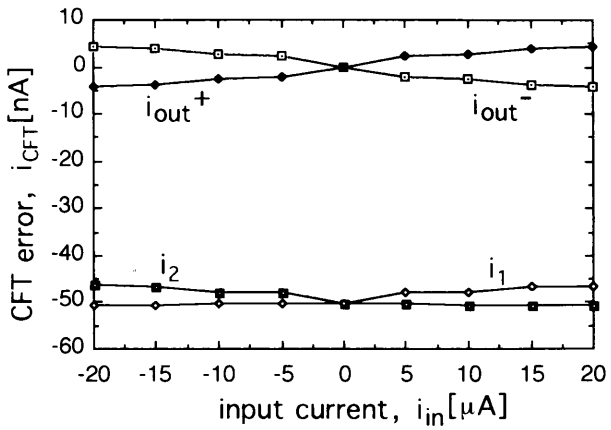

Fig. 4 Simulation results of CFT errors.

$$= (\alpha_1 - \alpha_2)\, i_{in} + \left(\frac{1}{\alpha_1} - \frac{1}{\alpha_2}\right)\frac{\beta_1}{2}\, V_C^2. \tag{6}$$

It should be mentioned that while the memory cell cancells the signal-dependent CFT component, the constant CFT component is left uncancelled.

Figure 2 shows the proposed fully-differential SI circuit. It consists of the two SI memory cells described above and current summing circuits which take the difference between i_1 and i_2. Assuming matched memory cells and matched summing circuits, the output currents are given by

$$i_{out}{}^+ = i_1 - i_2 = (\alpha_1 - \alpha_2)\,(i_{in}{}^+ - i_{in}{}^-), \tag{7}$$

$$i_{out}{}^- = i_2 - i_1 = -(\alpha_1 - \alpha_2)\,(i_{in}{}^+ - i_{in}{}^-), \tag{8}$$

where $i_{in}{}^+$ and $i_{in}{}^-$ are the differential input signals including the common-mode (CM) component. The current summing circuits thus cancel the constant CFT component and CM signal. The signal-dependent CFT component has been already cancelled by the memory cells. Therefore, the fully-differential SI circuit in Fig. 2 eliminates all the error sources, as requested for high performance analog signal processing applications.

3. Performance Estimates

The operation of the proposed circuit has been simulated using SABER, with level 2 MOS transistor model for a 1.2 μm standard CMOS process. All switches have the dimensions 1.2/1.2 μm (W/L) while the diode-connected transistor M_1 100/10 μm. The current mirror ratios α_1 and α_2 are set to 1 and 0.5, respectively. All simulations were performed supposing a 5 V power supply and a bias current $J = 100$ μA. Figure 3 shows the balanced output currents for balanced sinusoidal inputs with 20 μA amplitude and 10 μA CM offset. The sampling frequency is 500 kHz. It can be seen that the circuit outputs are well-balanced due to a substantial reduction of the CM and CFT components. Figure 4 shows more detailed measurements of the CFT errors. The input is the PWL signal sampled at 100 kHz frequency. The lower traces show the CFT errors in the memory cells. Differing from (6), the errors contain the signal-dependent component. This is because Eq. (1) gives only the first order approximation. The upper traces show that the constant CFT components are completely cancelled and no offset errors appear at the outputs when $i_{in}{}^+ = i_{in}{}^- = 0$. The residual CFT errors are less than 0.05% over the range from -20 μA to 20 μA. This residual error decreases with increasing bias current.

In a practical condition, non-ideal effects such as transistor gain error and threshold mismatch degrade these simulated performances. Their effect on the CMR can be estimated in terms of the mismatch error in current mirrors involved in the memory cells and the current summing circuits. Referring to (7) and noting that the CM input signal i_{CM} is defined by

$$i_{CM} = (i_{in}{}^+ + i_{in}{}^-)/2, \tag{9}$$

one can derive the following expression for the residual CM component δi_{CM} in the output current:

$$\delta i_{CM} = (\varepsilon_M + \varepsilon_S)\, i_{CM}/2, \tag{10}$$

where ε_M denotes the mismatch between the current transfer gains of the memory cells and ε_S is that of the

current summing blocks. These errors are independent each other and are evaluated to be 0.4% and 0.2%, respectively, from the current-mirror ratio error [4]. Therefore, the CMR in a practical environment is estimated to be 53 dB.

The non-ideal current mirrors in the memory cells also produce the uncancelled signal-dependent CFT component δi_{CFT} which is given, to first order, by

$$\delta i_{CFT} = \frac{2\varepsilon_{45}(J + i_{in})\, V_C}{v_{GS1} - V_T} \tag{11}$$

where ε_{45} is the current-mirror ratio error between M_4 and M_5 in Fig. 1. A typical values of ε_{45} is 0.14% [4]. By substituting the parameter values used in the simulations, δi_{CFT} is evaluated to be 7 nA. Because of the two uncorrelated memory cells, the signal-dependent CFT current of 10 nA is superposed on i_{out}^+ and i_{out}^- in Fig. 4. The SNR when $i_{in}=20$ μA is therefore estimated to be 63 dB in practice.

4. Conclusions

A new architecture for fully-differential SI circuit was proposed. Because of its high rejection capabilities of CFT and CM errors, it will be quite useful as a building block for filters, D/A and A/D converters. Adopting the folded cascode structure will further improve its performance.

References

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