LETTER *Special Section of Papers Selected from ITC-CSCC '96*

A Clock-Feedthrough Compensated Switched-Current Memory Cell

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SUMMARY A clock-feedthrough (CFT) compensation technique using a dummy cell is valid when the CFT current from a switched-current (SI) memory cell is signal-independent. Based on this idea, a SI dummy cell appropriate for the S^2I cell is developed. Simulations show that the CFT rejection ratio as high as 60 dB is attainable over the temperature range from $-30°C$ to $80°C$ with this architecture. The CFT-compensated SI cell proposed here is, therefore, quite useful for high-accuracy, current-mode signal processing.

key words: *current-mode signal processing, S^2I memory cell, clock-feedthrough compensation*

1. Introduction

A switched-current (SI) cell is an op-amp equivalent in current-mode, sampled-analog signal processing [1], [2]. The performance of the second-generation SI cell as a building block can be measured in terms of the input/output conductance ratio and the error current due to clock-feedthrough (CFT) [3]. The design technique to realize the high conductance ratio has been established by the regulated cascode configuration, and thus reducing the CFT error is now essential for high-accuracy signal processing.

The CFT error in a SI cell originates from those portions of the control signal and the channel charge of a switch transistor which charge the gate-to-source capacitor C_{GS} of a memory transistor. The resultant shift in the gate-source voltage produces the erroneous drain current referred to as the CFT current. This voltage-to-current conversion is nonlinear when a memory transistor operates in the saturation region, which makes the CFT current highly dependent on the input signal and invalidates the CFT compensation methods proposed for switched-capacitor circuits [4].

To eliminate the signal-dependence is the most crucial for substantial rejection of the CFT current, because the signal-independent component can be cancelled by the dummy cell method [5], [6]. Such first-generation SI cells have already been developed [7], [8]. This paper describes a CFT-compensated second-generation SI cell designed based on the above idea. The basic block is the S^2I cell [9]. A dummy stage appropriate for the S^2I cell is combined to substantially reduce the CFT error. The operation and the performance estimates will be described in the followings.

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2. CFT-Compensated S^2I Cell

Figure 1 (a) shows a basic SI cell and the principles of CFT cancellation. The basic cell samples the input signal current i_{in} in the sample phase when ϕ_s = "1," holds it during ϕ_s = "0," and delivers it to the load when ϕ_h = "1." The current i_M delivered to the load includes the error component δ_M which is caused by the CFT charge stored into C_{GS} of a memory transistor M_1. If δ_M is signal-independent and can be regarded as the offset current, it can be cancelled by providing the dummy cell whose output current δ_C counterbalances δ_M. A typical configuration of the dummy cell is shown in Fig. 1 (b).

A CFT-compensated SI cell designed based on the above-mentioned principles of CFT cancellation is shown in Fig. 2 (a). Here, M_1 and M_6 form the coarse stage, and M_2 and M_5 form the fine 1 stage of the S^2I cell with the cascode configuration. M_3 and M_4 form the fine 2 stage which functions as the dummy cell mirrored with the fine 1 stage. The fine 2 stage takes the same configuration as that of the fine 1 stage so that its output current i_2 cancels the CFT current from the fine 1 stage over the wide temperature range. The cascode current mirror M_7–M_{10} is provided for polarity inversion of i_2. All the stages and the current mirror are assumed operating in the saturation region. S_1, S_4, S_6, and S_7 are nMOS switches, while S_2, S_3, and S_5 are pMOS switches. These switches are controlled by clock signals whose timing is shown in Fig. 2 (b).

The operation of each stage is as follows:

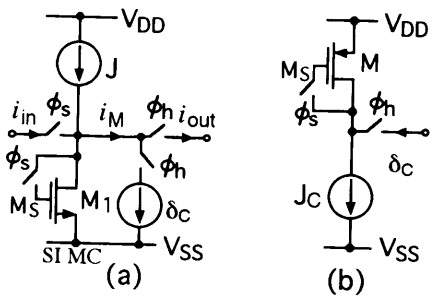

Fig. 1 A schematic diagram of a CFT-compensated SI cell (a) and a dummy-cell configuration (b).

(i) $\phi_1 = \phi_{1a}$ = "1" phase: The coarse stage samples i_{in}. Mirrored with the fine 2 stage, the fine 1 stage operates as current source to provide the bias current J_1 to the coarse stage. The fine 2 stage operates as the load of the current source J_1. The drain current of each stage is thus given by

$$i_{D1} = J_1 + i_{in}, \quad i_{D2} = J_1, \quad i_{D3} = J_1 \tag{1}$$

(ii) $\phi_1 = \phi_{1b}$ = "1" phase: Since S_1 is turned off, the coarse stage generates the CFT current δ_1. S_4 is still "on" to keep i_{in} flowing through the coarse stage. The fine 1 stage is now isolated from the fine 2 stage because S_5 is "off," and operates as the load of the coarse stage since S_2 is turned on. The fine 2 stage keeps the operation in the preceding phase. The current of each stage is therefore

$$i_{D1} = J_1 + i_{in} - \delta_1, \quad i_{D2} = J_1 - \delta_1, \quad i_{D3} = J_1 \tag{2}$$

(iii) ϕ_2 = "1" phase: The coarse stage is now isolated from the signal source and operates as the sink current source. Since S_2 and S_3 are turned off, the fine 1 and fine 2 stages generate the CFT current δ_2 and δ_3, respectively. The current flowing each stage is then given by

$$i_{D1} = J_1 + i_{in} - \delta_1, \quad i_{D2} = J_1 - \delta_1 + \delta_2,$$
$$i_{D3} = J_1 + \delta_3, \text{ and } i_2 = \delta_3. \tag{3}$$

The current mirror stage consisting of M_7 and M_{10} delivers the polarity-inverted i_2 to the output terminal. The output current i_{out} is therefore

$$i_{out} = i_{D2} - i_{D1} - i_2 = -i_{in} + \delta_2 - \delta_3. \tag{4}$$

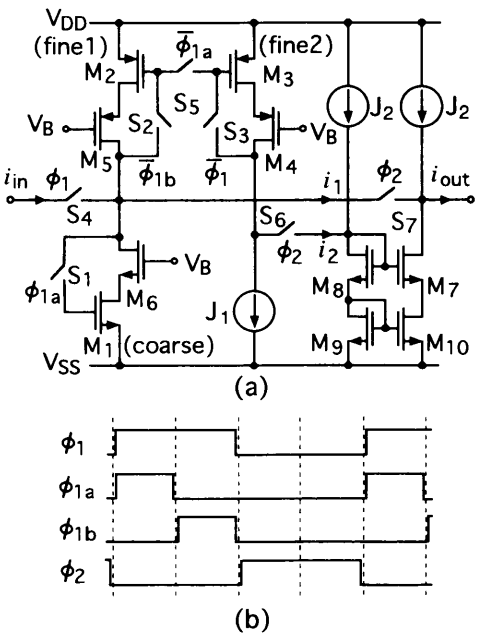

Fig. 2 The circuit diagram of the CFT-compensated SI cell (a) and timing diagram of clock signals (b).

It should be noted that the signal-dependent CFT δ_1 does not appear at the output. δ_2 is given by

$$\delta_2 = \sqrt{2\beta_2 i_{D2}}\left(\frac{Q_{f2}}{C_{GS2}}\right) - \frac{\beta_2}{2}\left(\frac{Q_{f2}}{C_{GS2}}\right)^2, \tag{5}$$

where $i_{D2} = J_1 - \delta_1$, β_2 is the gain factor of M_2, and Q_{f2} is the CFT charge stored in C_{GS2}. δ_3 is also given by (5) with the subscript 2 replaced by 3. Since $J_1 \gg \delta_1$, δ_2 is hardly dependent on the input signal. Therefore, using matched transistors for the fine 1 and 2 stages, one can substantially reduce the CFT error with this architecture.

3. Performance Estimates

The performance of above-described CFT-compensated SI cell have been simulated using SABER [10], with level-2 MOS transistor model for a 1.2 μm standard CMOS process. The aspect ratio of each transistor is listed in Table 1. Supply and bias voltages are: $V_{DD} = 5$ V, $V_{SS} = 0$ V, and $V_B = V_{DD}/2$. The current sources J_1 and J_2 are composed of the cascode current mirrors, and their values are set to 200 μA and 50 μA, respectively. The frequency of clock ϕ_1 is 2 MHz.

Figure 3 shows waveforms observed in the CFT-compensated cell when the input signal current is 180 μA. It can be seen that the current i_{D1} flowing through the coarse stage is $J_1 + i_{in} = 380\,\mu$A in the $\phi_1 = \phi_{1a}$ = "1" phase and decreases by the CFT current in the subsequent phase. In the ϕ_2 phase, the coarse and fine 1 stages deliver $i_1 = i_{in} + \delta_2 = 182.26\,\mu$A, and the fine 2 stage delivers $\delta_3 = 2.26\,\mu$A which counterbalances the CFT component $\delta_2 = 2.26\,\mu$A in i_1. The resultant output i_{out} is the exact replica of i_{in}. This observation confirms the operation described in the previous section.

Figure 4 shows the CFT current δ_2 from the fine 1 stage and the residual error $\Delta\delta = \delta_2 - \delta_3$ as a function of the input signal current. Figure 5 shows their temperature dependence when $i_{in} = 40\,\mu$A. Due mainly to the variation in the threshold voltage, δ_2 increases with temperature with the coefficient of 4,400 ppm/°C. The fine 2 stage also has the same temperature dependence, because of the identical configuration, to reduce the temperature coefficient of $\Delta\delta$ to 2 ppm/°C over the

Table 1 Transistor dimensions used for simulation.

Transistor	W(μm)	L(μm)
M1	36	4.8
M2	64	4.8
M3	64	4.9
M4, M5	60	1.2
M6	20	1.2
M9, M10	100	10
M7, M8	30	2
S1 ~ S3, S5	1.2	1.2
S4, S6, S7	12	1.2

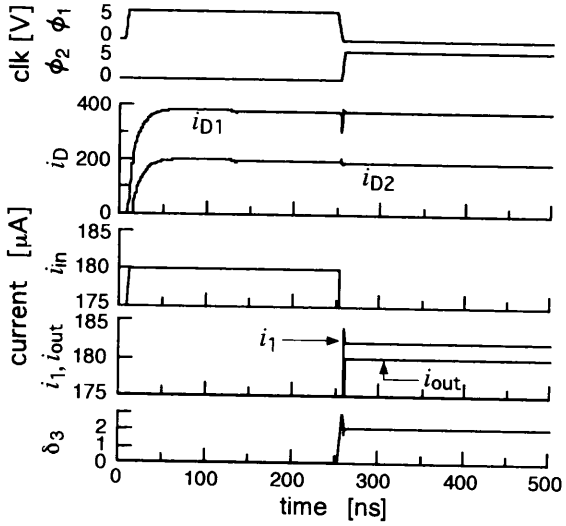

Fig. 3 Current waveforms observed in the CFT-compensated SI cell.

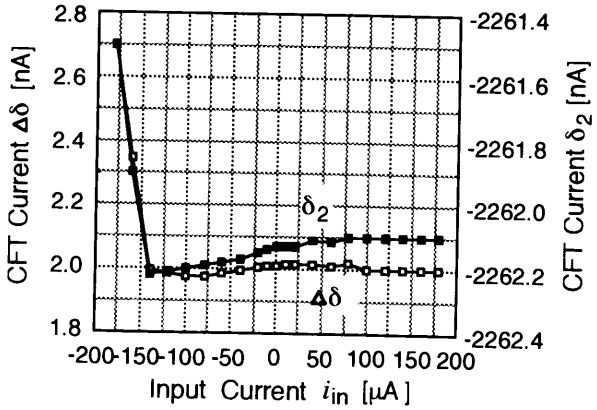

Fig. 4 CFT currents as a function of the input signal current.

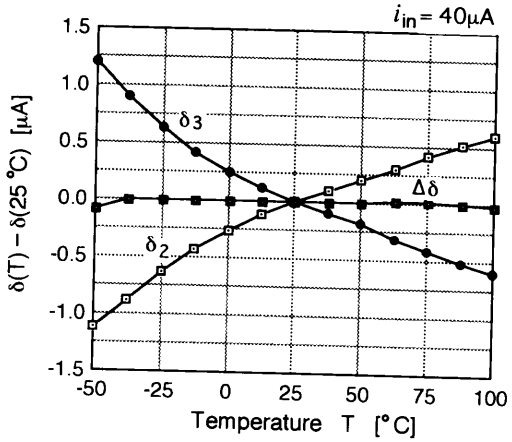

Fig. 5 Temperature dependence of CFT currents.

range from −30°C to 80°C. These results indicate that the CFT rejection ratio, defined as $\delta_2/\Delta\delta$, as high as 60 dB is achievable with the proposed SI cell over the wide dynamic and temperature ranges.

The above simulations assume 2% mismatch between M_2 and M_3, as can be seen in Table 1. The mismatch between S_2 and S_3 and the gain error of the current mirror also degrade the CFT rejection capability. Their effects are also simulated using typical values [11]. Simulations show that 1% mismatch between S_2 and S_3, which is an optimistic value for a recent process, degrades the CFT rejection to 40 dB, while each 0.2% mismatch in the current mirror and in the current sources J_2 [2], which is typical for the transistor dimensions quoted in Table 1, to 50 dB. It follows therefore that the careful arrangement of the fine 1 and 2 stages is essential for the high CFT rejection.

4. Conclusions

A CFT-compensated second-generation SI cell using a dummy cell was described. Simulations have shown that the high CFT rejection is possible with this architecture over the wide dynamic and temperature ranges. The performance is amenable to transistor mismatches, however, and a careful layout is essential for substantial reduction of CFT errors. The cell has just been fabricated using a 0.6 μm CMOS process. Its performances will be reported elsewhere.

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