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# Class A CMOS Current Conveyors

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**SUMMARY** The second-generation CMOS current conveyors are developed for high-frequency analog signal processing. It consists of a source follower for the voltage input and a regulated current mirror for the current input and output. The voltage and current input stages are also coupled by a current mirror to reduce the impedance of the current input port. Simulations show that this architecture provides the high input/output conductance ratio and the inherent voltage and current transfer bandwidths extending beyond 100 MHz. The prototype chips fabricated using 0.6 μm CMOS process have confirmed the simulated performances, though the voltage and current bandwidth are limited to 20 MHz and 35 MHz, respectively, by the built-in capacitances of the bonding pads.

***key words***: *current-mode signal processing, CMOS integrated circuit, current conveyor*

## 1. Introduction

A current-mode approach is quite attractive to high-frequency signal processing, because it can be relieved of the gain-bandwidth limitation accompanying with the voltage-mode signal processing. A versatile building block for current-mode signal processing in the continuous time-domain is the current conveyor [1], [2]. Toward its monolithic implementation, many architectures of the second-generation current conveyors (CCIIs) based on op-amps followed by current mirrors have been proposed in the early stage of development [3]. These evolutionary architectures and their applications have happily proved that any function ever performed in the voltage domain is possible with the current-mode approach [4], but their performances have failed to surpass their voltage-mode counterparts [5]-[7].

Current-mode processing features inherent wide bandwidth capability. To fully enjoy this advantage, the innovative architecture of CCII has been exploited and many architectures which do not involve op-amps have been reported. Though different in details, their input stages can be classified into two basic architectures; one based on the push-pull stage derived from the Wilson current mirror [8]-[14] and the other on the differential stage [15]-[19]. In the former configuration, the wideband voltage and current transfer characteristics are achievable, but the finite impedance at the current input port invalidates the virtual ground concept. In the latter configuration, on the other hand, the impedance at the current input port can be reduced to a negligibly small value by the negative feedback, but the bandwidth is still comparable to that of an op-amp. This comparison of key performance features implies that an ideal CCII could berealized by applying the negative feedback to the push-pull architecture. Based on this idea, a new architecture of CCII is developed [20]. Compared to the recently proposed CCII which uses a cascode stage to keep the potential at the current input node constant [21], this architecture uses the feedback stage which consists of a simple current mirror. The operation of the feedback stage is independent of the bias current and thus it is applicable to class AB CCIIs. In the followings, its circuit configuration, simulated and measured performances of the prototype chips fabricated using 0.6 μm CMOS process will be described.

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## 2. Circuit Description

Figure 1 shows the circuit diagram of the CMOS current conveyor. Transistor $M_2$, $M_3$, $M_4$, and $M_6$ form the regulated current cell for the current input and $M_1$ forms the source follower for the voltage input. $M_3$, $M_5$, and $M_7$ form the cascode current mirror to transfer the current $i_x$ flowing into the node $X$ to the node $Z$. Assume for the moment that $M_3$, $M_4$, and $M_5$ and two current sources J are matched. Then,

$$i_z = i_x. \tag{1}$$

The same amount of the current also flow through $M_1$. Therefore, the following relation holds.

$$g_{m1}(v_y - v_s) = g_{m2}(v_x - v_s) = -v_y/R_x, \tag{2}$$

where $g_{mi}$ ($i$ =1, 2) is the transconductance of $M_i$, $v_S$ is the source potential of $M_1$, and $R_x$ is the load resistor connected to the node $X$. From (2), we have

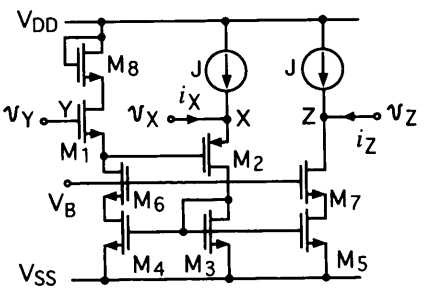


**Fig. 1** The circuit diagram of CCII+.

$$v_x = \frac{g_{m1}g_{m2}R_x v_y}{g_{m1} - g_{m2} + g_{m1}g_{m2}R_x}. \quad (3)$$

If $g_{m1}=g_{m2}$, or $g_{m1}g_{m2}R_x \gg g_{m1}-g_{m2}$, which is reasonable in practice, then $v_x$ follows exactly $v_Y$. The output impedance $r_z$ is given by

$$r_z = r_o // \left(g_{m7} r_{ds7} r_{ds5}\right), \quad (4)$$

where $r_o$ is the internal resistance of the current source $J$ and $r_{dsi}$ ($i$ =5, 7)is the drain/source resistance of $M_i$. If the current source $J$ consists of the cascode mirror, then $r_z$ is so high that $i_z$ is not affected by the load. No current flows through the node $Y$; $i_Y$=0. The input impedance $r_x$ at the node $X$ is given by

$$r_x = \frac{1}{g_{m2}} - \frac{g_{m4}g_{m6}}{g_{m1}g_{m3}} \frac{1}{g_{m6} + 1/r_{ds4}}. \quad (5)$$

In deriving (5), $g_{mi}r_{dsi} \gg 1$ is assumed. The second term in the right-hand-side arises from the cascode current mirror formed by $M_3$, $M_4$, and $M_6$ which regulates the source voltage of $M_2$. With the proper design of the regulator the input impedance $r_x$ can be made negligibly small and the node $X$ is virtually grounded when $v_Y$=0.

Summarizing the circuit operations described above, one can express the input-output relations as follows:

$$\begin{bmatrix} i_x \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}. \quad (6)$$

This matrix representation indicates that the circuit shown in Fig. 1 is the CCII+ itself. The CCII- can be realized by inverting $i_z$ by means of a cross-coupled current mirror.

## 3. Performances

The CCII+ and CCII- based on Fig. 1 were fabricated using 0.6 μm CMOS process. The complete circuit diagram is shown in Fig. 2 and transistor dimensions are listed in Table 1. The terminal connection shown in Fig. 2 is for the CCII+. For the CCII-, terminals ⓐ and ⓑ are connected to ③ and ④, respectively. A microphotograph of the CCII+ is shown in Fig. 3. All PMOS transistors can be seen implanted into the n-well in the upper part except $M_2$ which is implanted independently into the n-well in the lower central part. Performances of these prototype chips were measured under the bias condition; $V_{DD}$=–$V_{SS}$=2.5 V, $V_B$= –0.5 V, and $J$=100 μA which was set by the external resistor connected between $N_1$ and $V_{SS}$. Measured performances were compared with those simulated using HSPICE with level 47 transistor model.

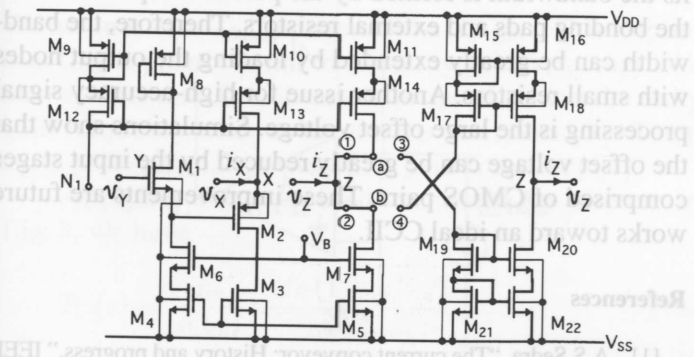


**Fig. 2** The complete circuit diagram of CCII fabricated using 0.6 μm CMOS process.

Figure 4 shows the current-voltage characteristics at the node $X$ when nodes $Y$ and $Z$ are short-circuited. The input impedance $r_x$ and the offset voltage at node $X$ are 350 Ω and –0.43 V, respectively. These measured values differ largely from those simulated ones, 30 Ω and –0.33V, respectively. The differences are attributed to incorrect body-effect paramters. Introducing the diode-connected PMOS and NMOS transistors in series with $M_1$ and $M_2$, respectively, one can greatly reduce the offset voltage [19]. Figure 5 shows the current transfer characteristics between $i_x$ and $i_z$ when the node $Y$ is short-circuited and the node $Z$ is virtual-grounded by the

**Table 1** Transistor dimensions in CCIIs.

| Transistor | W(μm) | L(μm) |
|---|---|---|
| $M_1$ | 30 | 1.8 |
| $M_2$ | 120 | 1.8 |
| $M_3 \sim M_5$ | 40 | 3 |
| $M_6 \sim M_{14}$ | 60 | 1.8 |
| $M_{19} \sim M_{20}$ | 50 | 1.8 |
| $M_{21} \sim M_{22}$ | 30 | 1.8 |

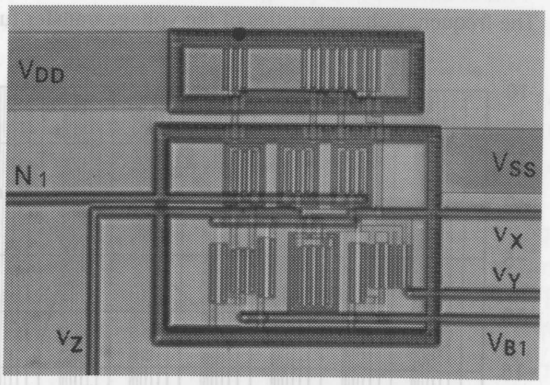


**Fig. 3** A microphotograph of CCII+.

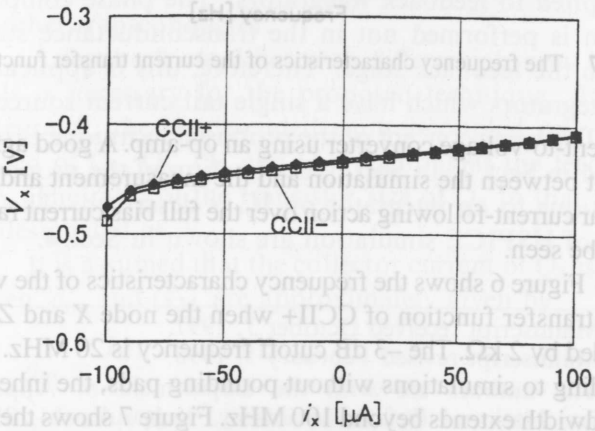


**Fig. 4** The input characteristics at the node $X$.

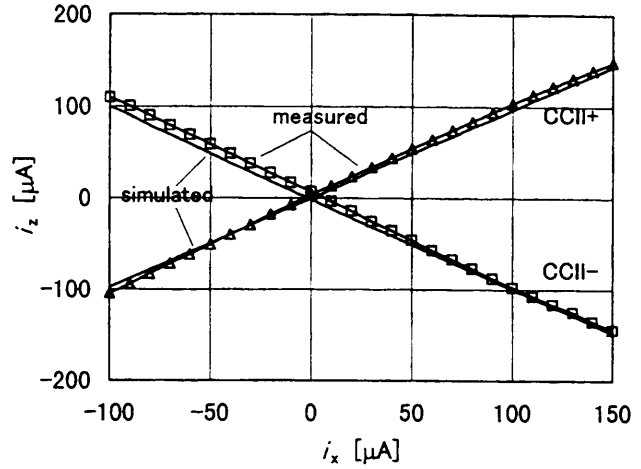


**Fig. 5** The $i_z$ vs. $i_x$ characteristics.

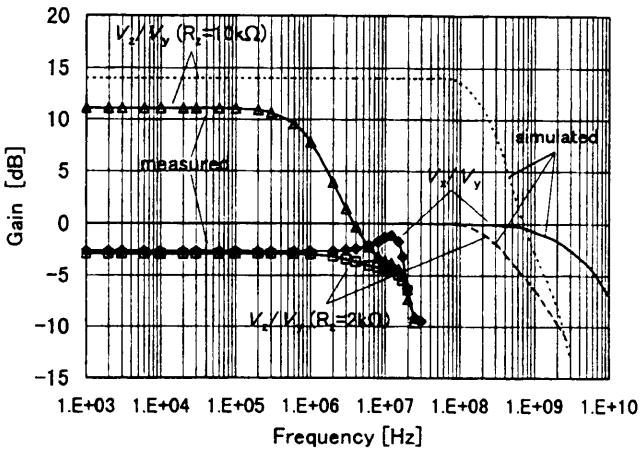


**Fig. 6** The frequency characteristics of the voltage transfer function.

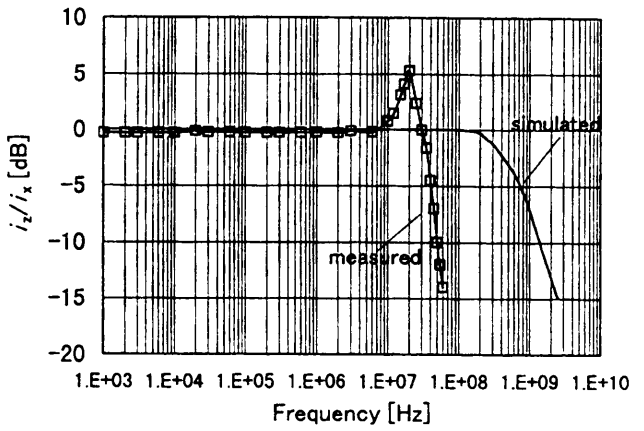


**Fig. 7** The frequency characteristics of the current transfer function.

current-to-voltage converter using an op-amp. A good agreement between the simulation and the measurement and the linear current-following action over the full bias current range can be seen.

Figure 6 shows the frequency characteristics of the voltage transfer function of CCII+ when the node $X$ and $Z$ are loaded by 2 kΩ. The –3 dB cutoff frequency is 20 MHz. According to simulations without pounding pads, the inherent bandwidth extends beyond 100 MHz. Figure 7 shows the frequency characteristics of the current transfer function of

**Table 2** Measured performances of CCIIs.

| | Class A CCII+ (CCII-) |
|---|---|
| Technology | 0.6 μm n-well CMOS process |
| Supply voltage | 5 V or +2.5 V to -2.5 V |
| Power dissipation | 2 mW (3 mW) |
| Impedance at node X | 350 Ω |
| Impedance at node Y | Ω |
| Impedance at node Z | 6 MΩ |
| Offset voltage ($v_x$ vs. $v_y$) | -0.43 V |
| Offset current ($i_x$ vs. $i_z$) | 1.9 μA (1.1μA) |
| Voltage dynamic range | -0.5 V to +1.5 V |
| Current dynamic range | -100 μA to +150 μA |
| 3-dB cutoff frequency of ($v_x/v_y$) when $R_x$=10 kΩ | 20 MHz |
| 3-dB cutoff frequency of ($v_z/v_y$) when $R_x$=$R_z$=10 kΩ | 18 MHz |
| 3-dB cutoff frequency of ($i_z/i_x$) | 35 MHz |
| Active chip area | 0.2 × 0.2 [mm²] |

CCII+. The measured bandwidth is 35 MHz whereas the simulated bandwidth extends beyond 300 MHz. These differences in the frequency response between simulations and measurements in Figs. 6 and 7 are attributed to the parasitic poles created by the stray capacitance of the bonding pads which is not taken into the simulation. The pad capacitance is estimated experimentally to be 15 pF. Figure 6 also shows the frequency characteristics of CCII+ when used as a voltage amplifier with nodes $X$ and $Z$ terminated by 2 kΩ and 10 kΩ, respectively. The –20 dB/decade roll-off characteristics indicate that the bandwidth is limited again by the pad capacitances. To confirm these experimental observation, the frequency characteristics including the pad capacitances are simulated. The results are in good agreement with measured characteristics and also confirm that the high frequency peaking appearing in the frequency response of the current transfer function is due to the pad capacitances. The same frequency responses were also observed in CCII-.

## 4. Conclusions

Circuit configurations and performances of CCIIs fabricated using 0.6 μm CMOS process were described. Measured performances are summarized in Table 2. These performances, especially the bandwidth, are insufficient for enjoying current-mode signal processing. The dominant pole which limits the bandwidth is formed by the parasitic capacitances of the bonding pads and external resistors. Therefore, the bandwidth can be greatly extended by loading the output nodes with small resistors. Another issue for high-accuracy signal processing is the large offset voltage. Simulations show that the offset voltage can be greatly reduced by the input stages comprised of CMOS pairs. These improvements are future works toward an ideal CCII.

### References

[1] A.S.Sedra, "The current conveyor: History and progress," IEEE ISCAS Proc., pp.1567-1571, 1989.
[2] A.S.Sedra, G.W.Roberts, and F.Gohn, "The current conveyor:

History, progress and new results," IEE Proc., vol.137, Pt. G, pp.78-87, April 1990.

[3] C.Toumazou, F.J.Lidgey, and P.Y.K.Cheung, "Current-mode analogue signal processing circuits– A review of recent developments," IEEE ISCAS Proc., pp.1572-1575, 1989.

[4] C.Toumazou, F.J.Lidgey, and C.A.Makris, "Extending voltage mode op-amps to current-mode performance," IEE Proc., vol.137, Pt. G, pp.116-130, April 1990.

[5] G.W.Roberts and A.S.Sedra, "All current-mode frequency selective circuits," Electron. Lett., vol.25, pp.759-762, June 1989.

[6] C.Toumazou, F.J.Lidgey, and D.G.Haigh, eds., "Analogue IC Design: The current-mode approach," chap.4, Peter Peregrinus, London, 1990.

[7] G-H.Wang, K.Watanabe, and Y.Fukui, "A dual transformation approach to current-mode filter synthesis," IEICE Trans. Electron., vol.E75-C, pp.729-735, June 1992.

[8] A.Fabre, "Wideband translinear current conveyor," Electron. Lett., vol.20, pp.241-242, March 1984.

[9] Z.Wang, "Wideband class AB (push-pull) current amplifier in CMOS technology," Electron. Lett., vol.26, pp.543-545, April 1990.

[10] C.Toumazou, F.J.Lidgey, and D.G.Haigh, eds., "Analogue IC Design: The current-mode approach," chap.15, Peter Peregrinus, London, 1990.

[11] C.Toumazou, J.B.Hughes, and N.C.Battersby, eds., "Switched-Currents an analogue technique for digital technology," chap.7, Peter Peregrinus, London, 1993.

[12] E. Bruun, "CMOS current-conveyors," IEEE ISCAS'94 Tutorials, chap.11.5.

[13] A.Piovaccari, "CMOS integrated third-generation current conveyor," Electron. Lett., vol.31, pp.1228-1229, July 1995.

[14] A.Fabre, O.Saaid, F.Weist, and C.Boucheron, "High frequency applications based on a new current controlled conveyor," IEEE Trans. Circuits and Systems, Pt-1, vol.43, pp.82-91, Feb. 1996.

[15] Th.Laopoulos, S.Siskos, M.Bafleur, and Ph.Givelin, "CMOS current conveyor," Electron. Lett., vol.26, pp.543-545, April 1990.

[16] M.C.H.Cheng and C.Toumazou, "3V CMOS current conveyor cell for VLSI technology," Electron. Lett., vol.29, pp.317-318, Feb. 1993.

[17] R.H.Zele, D.J.Allstot, and T.S.Fiez, "Fully balanced CMOS current-mode circuits," IEEE J. Solid-State Circuits, vol.28, pp.569-574, May 1993.

[18] W.Chiu, S-I.Liu, H-W.Tsao, and J-J.Chen, "CMOS differential difference current conveyors and their applications," IEE Proc. Circuits Devices Syst., vol.143, pp.91-96, April 1996.

[19] H.O.Elwan and A.M.Soliman, "A novel CMOS Current conveyor realization with an electronically tunable current mode filter suitable for VLSI," IEEE Trans. Circuits and Syst., Pt. II, vol.43, pp.663-670, Sept. 1996.

[20] H-W.Cha and K.Watanabe, "Wideband CMOS current conveyor," Electron. Lett., vol.32, pp.1245-1246, July 1996.

[21] O.Oliaei and J.Porte, "Compound current conveyor (CCII+ and CCII-)," Electron. Lett., vol.33, pp.253-254, Feb. 1997.