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PAPER

A CMOS Rail-to-Rail Current Conveyor

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SUMMARY This paper presents a second-generation CMOS current conveyor (CCII) consisting of a rail-to-rail complementary n- and p-channel differential input stage for the voltage input, a class AB push-pull stage for the current input, and current mirrors for the current outputs. The CCII was implemented using a double-poly triple-metal 0.6 μm n-well CMOS process, to confirm its operation experimentally. A prototype chip achieves a rail-to-rail swing ± 2.3 V under ± 2.5 V power supplies and shows the exact voltage and current following performances up to 100 MHz. Because of its high performances, the CCII proposed herein is quite useful for a building block of current-mode circuits.

key words: *current conveyor, CMOS integrated circuit, rail-to-rail, class AB, wideband*

1. Introduction

A recent trend toward a large electronic system on a chip drives CMOS process to the submicrometer feature size. One of the biggest problems associated with the high density packing by the reduced feature size is the power dissipation, and electronic circuits are obliged to operate under the low supply voltage. To meet such requirements as the wide dynamic range and the wide bandwidth operations under the low supply voltage, current-mode analog signal processing is receiving much attention as a voltage-mode alternative. An op-amp equivalent in current-mode circuits is the second-generation current conveyor (CCII), and its CMOS realization is highly requested to facilitate the analog circuit design in a mixed analog and digital CMOS ASIC [1], [2].

The CCII is a three-terminal device whose terminal relations can be expressed by the following matrix representation:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}, \quad (1)$$

where v_y, i_x, and v_z are the excitations applied to the voltage input terminal Y, the current input terminal X, and the current output terminal Z, respectively, and i_y, v_x, and i_z are the responses to these excitations. The element ± 1 in the matrix assumes $+1$ if the direction of i_z is the same as that of i_x and -1 otherwise.

The ideal characteristics given by (1) indicate that the CCII is characterized in terms of the terminal impedances and the voltage- and current-following performances [3], [4]. These performances can be achieved by a source follower and a current mirror. The CCII can thus be realized by combining these simple circuits such that the output of the source follower be the input of the current mirror. Such an architecture exhibits an excellent current-following action over the wide bandwidth, but suffers from the poor voltage-following performance due to the high output impedance of the follower [5]–[9]. To reduce the output impedance, the constant potential and current feedback techniques have been proposed [10], [11], but the output swing limited by the source follower remains unsolved.

Much better voltage-following performance can be realized by the op-amp with unity-gain configuration. The rail-to-rail input and output capabilities can also be provided with the op-amp under class AB operation [12]–[17]. Based on this idea, a CMOS rail-to-rail CCII is developed. Its circuit configuration, simulated performances, and a prototype chip fabricated using 0.6 μm CMOS process will be described in the followings.

2. Circuit Description

The circuit configuration of the CMOS rail-to-rail CCII is shown in Fig. 1, where Y is the voltage input terminal, X is the voltage/output current input terminal, and $\pm Z$ are the current output terminals. It comprises five blocks; the rail-to-rail input stage consisting of the

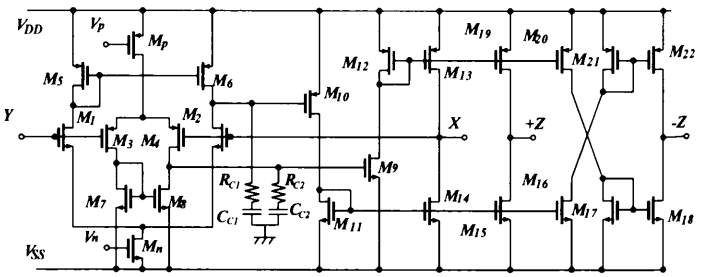

Fig. 1 The circuit diagram of the proposed rail-to-rail CCII.

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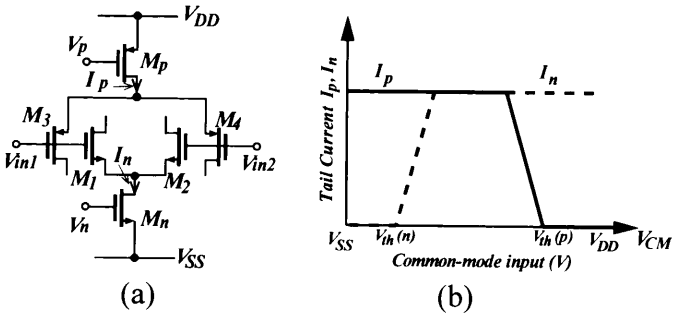

Fig. 2 (a) An input stage model of the rail-to-rail input stage. (b) The tail currents in the rail-to-rail input stage.

complementary n- and p-channel differential pairs (M_1–M_8) for the voltage input v_y, the phase compensation and the level shift stage (R_{C1}, R_{C2}, C_{C1}, C_{C2}, M_9–M_{12}), the rail-to-rail class AB push-pull stage (M_{13}, M_{14}) for the voltage output/current input i_x, the current mirrors (M_{15}–M_{22}) for the current outputs $i_{\pm z}$, and the bias stage. The differential input, level shift, and class AB push-pull stages form the operational transconductance amplifier (OTA).

2.1 Complementary Input Stage

The schematic of the complementary input stage is shown in Fig. 2(a), where n- and p-channel differential pairs are connected in parallel. The operation can be divided into three regions shown in Fig. 2(b): The positive rail region where only nMOS pair is active, the mid-rail region where both nMOS and pMOS pairs are active, and the negative rail region where only pMOS pair is active. The transconductance g_m of the input stage therefore depends on the input voltage. The dependence may cause the harmonic distortion, but the common-mode feedback to make g_m independent of the input voltage is not incorporated. This is because the OTA forms the voltage follower by the fully feedback configuration and this configuration reduces the harmonic distortion by a factor of the open-loop gain of the OTA.

2.2 Voltage Following Operation

Regarding the voltage and current input stages as the input and output stages of the OTA, respectively, one can model the input stage as shown in Fig. 3(a). Figure 3(b) shows the small-signal equivalent circuit. Referring to this model, one obtains the voltage transfer gain A_v from the node Y to the node X:

$$A_v = \frac{v_x}{v_y} = \frac{(g_{m9}A_p + g_{m10}A_n)R}{1 + (g_{m9}A_p + g_{m10}A_n)R}, \tag{2}$$

where A_n and A_p are the gains of the n- and p-channel differential stages, g_m is the transconductance of MOS transistor and R is a load resistor at the node X. A_v is very close to 1 since $(g_{m9}A_p + g_{m10}A_n)R \gg 1$ holds usually. Therefore, v_x exactly follows v_y.

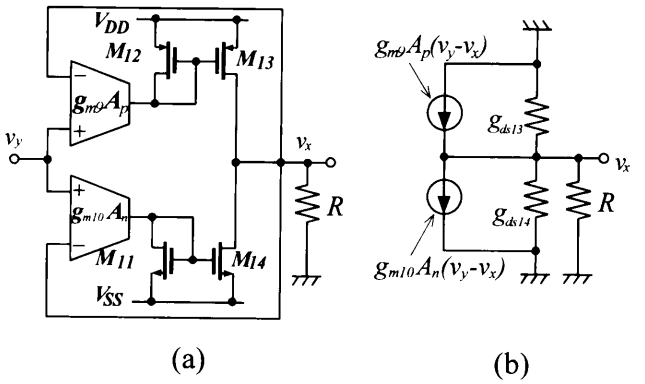

Fig. 3 The input stage model of the CCII (a) and its small-signal equivalent circuit (b).

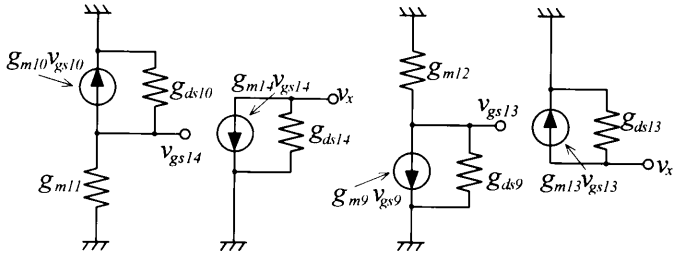

Fig. 4 The small-signal equivalent circuits at the drains of M_{13} and M_{14}.

2.3 Input/Output Impedance at Node X

Figure 4 shows the small-signal equivalent circuits at the node X. Referring to Fig. 4, the impedance r_{xn} presented by M_{14} is given by

$$r_{xn} = \frac{1}{g_{ds14} + \dfrac{g_{m14}g_{m10}A_n}{g_{m11} + g_{ds10}}}, \tag{3}$$

where g_{ds} is the drain-source conductance of MOS transistor.

Similarly, the impedance r_{xp} presented by M_{13} is given by

$$r_{xp} = \frac{1}{g_{ds13} + \dfrac{g_{m13}g_{m9}A_p}{g_{m12} + g_{ds9}}}. \tag{4}$$

The impedance r_x at the node X is the parallel connection of r_{xn} and r_{xp}, and thus

$$\begin{aligned} r_x &= \frac{1}{g_{ds14} + \dfrac{g_{m14}g_{m10}A_n}{g_{m11} + g_{ds10}}} // \frac{1}{g_{ds13} + \dfrac{g_{m13}g_{m9}A_p}{g_{m12} + g_{ds9}}} \\ &= \frac{1}{\dfrac{g_{m13}g_{m9}A_p}{g_{m12}} + \dfrac{g_{m14}g_{m10}A_n}{g_{m11}}} = \frac{1}{g_{m9}A_p + g_{m10}A_n}. \end{aligned} \tag{5}$$

In deriving the last expression, $g_{ds} \ll g_m$, $g_{m12} = g_{m13}$, and $g_{m11} = g_{m14}$ are assumed.

Equation (5) indicates that the impedance at the node X of a basic CCII is reduced by the open loop gain of the differential stage. With the simple configuration shown in Fig. 1, the gain higher than 40 dB can be realized. It follows therefore that the node X in Fig. 1 is virtually grounded when the node Y is grounded.

2.4 Rail-to-Rail Class AB Output Stage

Referring again to Figs. 1 and 4, one obtains the following expressions for the current flowing through M_{13} and M_{14}:

$$i_{d13} = J + g_{ds13}v_{d13} - \frac{g_{m9}g_{m13}A_p(v_y - v_x)}{g_{m12} + g_{ds9}}, \quad (6)$$

$$i_{d14} = J + g_{ds14}v_{d14} + \frac{g_{m10}g_{m14}A_n(v_y - v_x)}{g_{m11} + g_{ds10}}, \quad (7)$$

where

$$v_{d13} = V_{DD} - v_x, \quad (8)$$

$$v_{d14} = v_x - V_{SS} \quad (9)$$

In (6) and (7), the same quiescent current J is assumed flowing through M_{13} and M_{14}. Because of the exact voltage-following action $v_y = v_x$ and $g_{ds} \ll 1$, the ac components in (6) and (7) are much smaller than the quiescent current. Then

$$\begin{aligned} v_{gs14} + v_{gs13} &= \sqrt{\frac{i_{d13}}{K_{13}}} + V_{th13} + \sqrt{\frac{i_{d14}}{K_{14}}} + V_{th14} \\ &\approx \sqrt{\frac{J}{K}}\left(2 + \frac{g_{ds}(V_{DD} - V_{SS})}{2J}\right) + V_{th13} + V_{th14} \\ &= \text{const.} \end{aligned} \quad (10)$$

where K_{13} and K_{14} are the transconductance parameters of M_{13} and M_{14}, respectively, and $K_{13} = K_{14} = K$ and $g_{ds13} = g_{ds14}$ are assumed to derive the last expression. Equation (10) indicates that M_{13} and M_{14} operate under the push-pull mode.

The current i_x applied to the node X is shared between M_{13} and M_{14}. Taking the push-pull condition (10) into account, one can derive the following expressions for i_{d13} and i_{d14}:

$$i_{d14} = J - i_x/2 + i_x^2/16J, \quad (11)$$

$$i_{d13} = J + i_x/2 + i_x^2/16J. \quad (12)$$

Equations (11) and (12) indicate that the push-pull operation continues until i_x reaches $\pm 4J$ where the single-ended operation starts, as shown in Fig. 5. The maximum current is limited by the voltage headroom in the push-pull stage.

2.5 Current Following Operation

Figure 6 shows the lower half section of the current

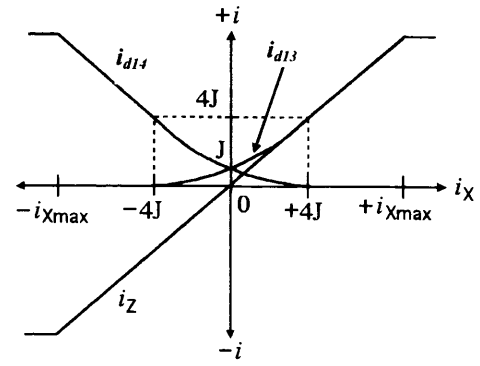

Fig. 5 The current transfer characteristics.

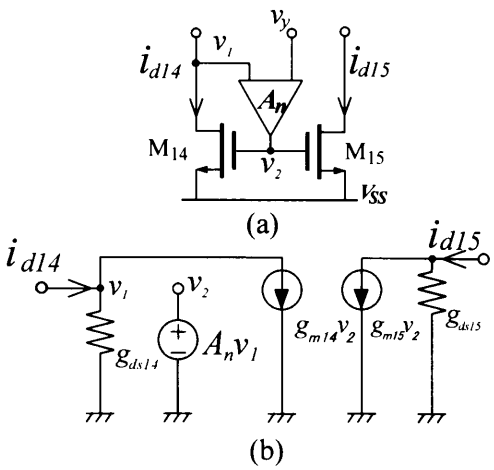

Fig. 6 The active current mirror (a) and its small-signal equivalent circuit (b).

input and output stages. The differential stage A_n, M_{14}, and M_{15} form the active current mirror [18]-[20]. Referring to the equivalent circuit shown in Fig. 6(b), one can derive the following expression for the current transfer:

$$\frac{i_{d15}}{i_{d14}} = \frac{\dfrac{1}{g_{ds14}}}{\dfrac{1}{g_{ds14}} + \dfrac{1}{A_n \times g_{m15}}}. \quad (13)$$

where $g_{m14} = g_{m15}$ is assumed. Equation (13) indicates that the active current mirror achieves the exact mirror operation by reducing the input impedance effectively by the differential stage gain. The similar relation also holds true of the upper half section of the current input and output stages. Thus, under the quite reasonable assumption $A_n g_{m15} \gg g_{ds14}$, we have

$$i_z = i_{d19} - i_{d16} = i_{d13} - i_{d14} = i_x. \quad (14)$$

2.6 Phase Compensation

The OTA in Fig. 1 has three poles; the dominant pole P_1 presented by M_8 (M_6), the second pole P_2 by M_9 (M_{10}), and the third pole P_3 by the output node X. The Bode diagram when the OTA is loaded by 1 kΩ is

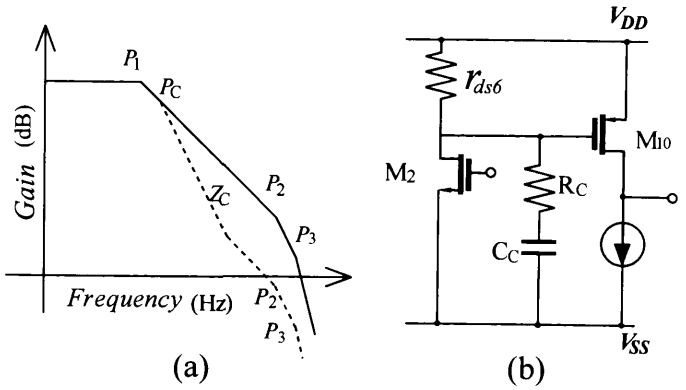

Fig. 7 Bode diagrams of the OTA (a) and the phase compensation network (b).

sketched in Fig. 7(a). The two high-frequency poles P_2 and P_3 are located closely in this configuration. Such a pole location invalidates the pole-splitting and phase-lead techniques for the phase compensation, and the phase-lag method is applied though it degrades the high-frequency performance. The compensated Bode diagram is shown by the dotted line in Fig. 7(a) and the compensation network is shown in Fig. 7(b). The pole f_{PC} and zero f_{ZC} frequencies introduced by the network are given by

$$f_{PC} = \frac{1}{2\pi C_c(r_{ds6} + R_C)}, \tag{15}$$

$$f_{ZC} = \frac{1}{2\pi C_c R_C}. \tag{16}$$

Locating f_{PC} and f_{ZC} between P_1 and P_2 stabilizes the OTA, as shown in Fig. 7(a), because the open-loop gain crosses 0 dB with the slope −20 dB/Decade.

3. Performances

3.1 Simulations

Performances of the CCII shown in Fig. 1 are simulated using HSPICE. Transistor dimensions and the compensation elements are listed in Table 1. The parameters used for the simulations assume 0.6 μm CMOS process. Supply voltages are $V_{DD} = -V_{SS} = 2.5$ V and J is set to 50 μA. Simulated performances are shown by solid and dotted lines in the following figures.

Figure 8 shows the total harmonic distortion (THD) in the voltage follower when 1 V_{p-p} sinusoidal signal is applied to the node Y and the node X is terminated by $R_X = 1\,\text{k}\Omega$. THD is lower than −75 dB in the low-frequency region, but increases with frequency in the high-frequency region above 1 MHz. This is attributed due to the gain reduction in the differential stage which invalidates the push-pull condition (10).

The Bode diagram of the OTA when the output node X is terminated by 1 kΩ is shown in Fig. 9. The dc gain is 49 dB. The unity gain frequency is 100 MHz and the phase margin is 60°.

Table 1 Transistor dimensions and the compensation elements.

Transistor	W (μm)	L (μm)
M_1, M_2, M_7, M_8	24	1.2
M_3- M_6	60	1.2
M_9, M_{11}, M_{14}- M_{18}	42	1.2
M_{10}, M_{12}, M_{13}, M_{19}- M_{22}	126	1.2
Element values	(kΩ)	(pF)
R_{C1}, R_{C2}	2	-
C_{C1}, C_{C2}	-	1

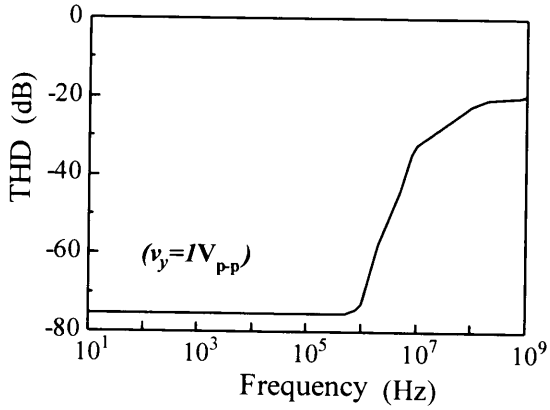

Fig. 8 THD of the CCII.

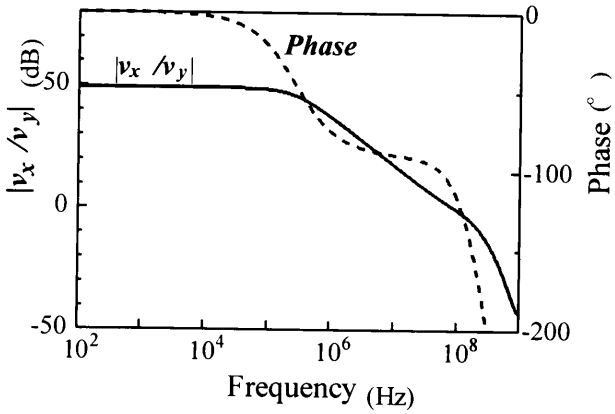

Fig. 9 The Bode diagram of the OTA.

Figure 10 shows the input characteristics at the node X. The positive sign in the current indicates the current flowing into the node and the minus sign the current flowing out of the node. The impedance r_x is 6.67 Ω in the push-pull region and decreases slightly in the single-ended region.

Figure 11 shows the voltage transfer characteristics from the node Y to the node X when the node Z is short-circuited to ground. The exact voltage-following performance and the rail-to-rail input and output capabilities are demonstrated. The offset voltage at the node X when the node Y is grounded is less than 1.7 mV.

Figure 12 shows the current transfer characteristics from the node X to the node Z. The transfer gains

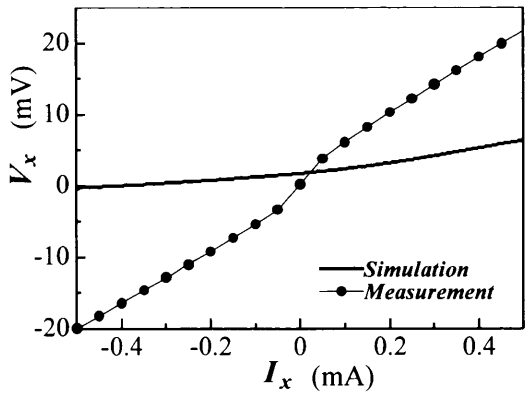

Fig. 10 The V_x versus I_x characteristics.

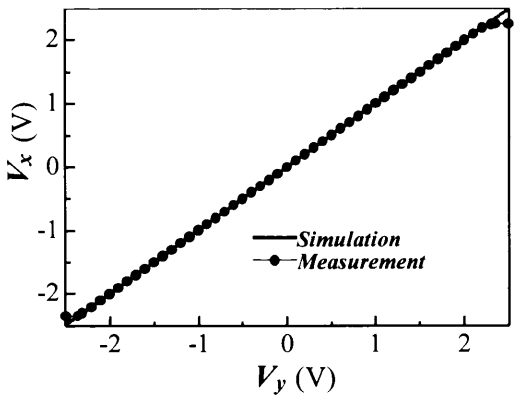

Fig. 11 The voltage transfer characteristics of the CCII.

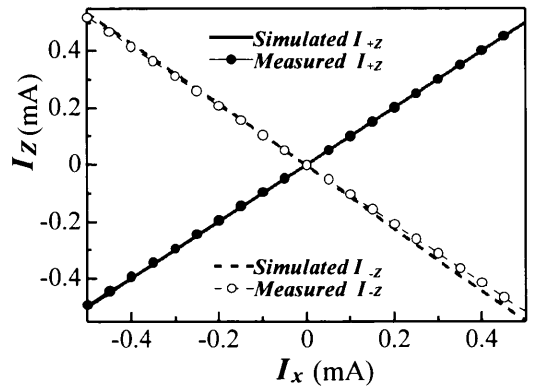

Fig. 12 The current transfer characteristics.

I_{+z}/I_x and I_{-z}/I_x are 1.00 and -1.08, respectively, and the offset currents in I_{+z} and I_{-z} are 31.1 nA and 2.96 nA, respectively.

The frequency characteristics of the voltage gain when the node X is terminated by $R_X = 1\,\mathrm{k}\Omega$ are shown in Fig. 13. The -3 dB bandwidth extends beyond 200 MHz.

Figure 14 shows the frequency characteristics of the current transfer gain. The bandwidth extends again beyond 150 MHz and no degradation due to the differential stage is observed.

Figure 15 shows the frequency dependence of the input impedance at the node X when the nodes Y and Z are grounded. Similarly to THD, the input impedance

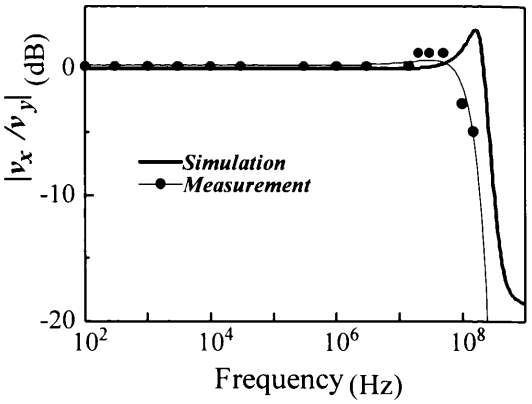

Fig. 13 The frequency characteristics of the voltage transfer gain.

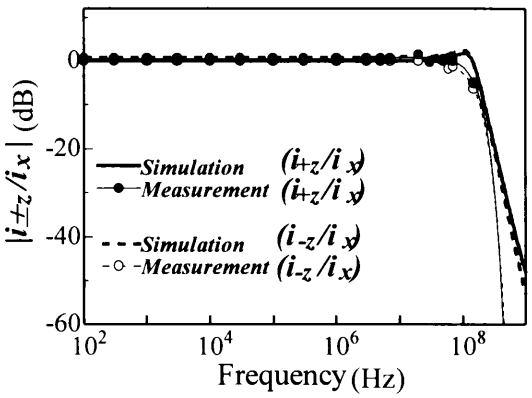

Fig. 14 The frequency characteristics of the current transfer gains.

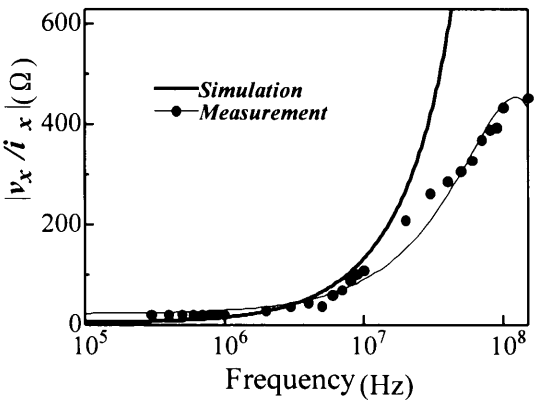

Fig. 15 The frequency dependence of the input impedance.

increases with frequency in the frequency region above 1 MHz. This is also due to the gain reduction in the differential stage.

3.2 Measured Performances

The proposed CCII was implemented using a double-poly, triple-metal 0.6 μm n-well CMOS process. The microphotograph of the prototype chip is shown in Fig. 16. The chip measures 250 μm $\times$ 150 μm. All the measurements are done under ± 2.5 V supplies. The static current is 300 μA. Measured performances are in-

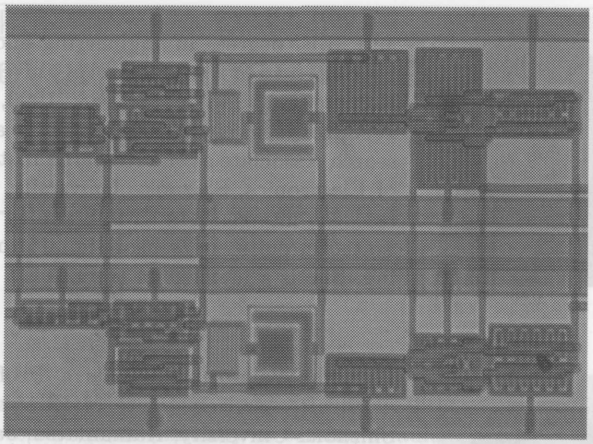

Fig. 16 A microphotograph of the prototype chip.

dicated by dots in the relevant figures.

The I_x versus V_x characteristics are plotted in Fig. 10. The measured input impedance r_x is 41.7 Ω in the push-pull region. The simulated value is 6.67 Ω. The large difference is attributed to the wire resistance between the node X and the ponding pad. The voltage transfer characteristics are plotted in Fig. 11, which demonstrates the exact voltage-following performance and the rail-to-rail input and output capabilities. The offset voltage at the node X when the node Y is grounded is less than 30 μV.

The current transfer characteristics are plotted in Fig. 12. The exact current-following performances in good agreement with the simulations can be seen over the wide current range. The transfer gains I_{+z}/I_x and I_{-z}/I_x are 1.00 and −1.03, respectively. The offset currents in I_{+z} and I_{-z} when the node Y is grounded are 85 nA and 4 nA, respectively.

The frequency characteristics of the voltage gain when the node X is terminated by $R_X = 1\,\mathrm{k}\Omega$ are plotted in Fig. 13. The −3 dB bandwidth of the voltage gain v_x/v_y extends beyond 100 MHz. The frequency characteristics of the current transfer gains are plotted in Fig. 14. The bandwidth extends again beyond 100 MHz.

The frequency dependence of the input impedance at the node X is plotted in Fig. 15. In the low frequency range, the measured input impedance is higher than the simulated one. This is due to the wire resistance from the node X to the ponding pad, as explained earlier. In the high frequency range, on the other hand, the measured impedance is lower than the simulated one. This is due to the parasitic capacitance of the ponding pad.

4. Conclusions

A rail-to-rail CCII developed for wideband signal processing under low power operation was described. Performances measured in the prototype chip fabricated using 0.6 μm CMOS process are summarized in Table 2, together with those of the CCII proposed earlier [21]. Comparison demonstrates that the prototype chip is quite useful for wideband current signal processing. The operation under the single supply voltage as low as 1 V has been confirmed experimentally. Such a low-voltage operation and the small device-count are also quite attractive to ASICs. The commercial chip is now under fabrication using a standard digital CMOS process.

Table 2 Performances of a prototype chip compared with those of the CCII proposed in [21]. *: Simulated performances.

	Prototype chip	CCII in [21]
Input /output voltage range	4.6V(5V*)	2.4V*
Supply voltage	5V	3V
Impedance r_x @DC	41.7Ω(6.67Ω*)	34Ω*
Offset voltage	30μV(1.7mV *)	0.5mV*
Offset current	I_{+z} : 85nA (31.1nA*) I_{-z} : 4nA (2.96nA *)	I_{+z} : 450nA* -
−3 dB bandwidth in voltage transfer	120MHz(250MHz *)	18MHz*
−3 dB bandwidth in current transfer	120MHz(170MHz *)	25MHz*

Acknowledgments

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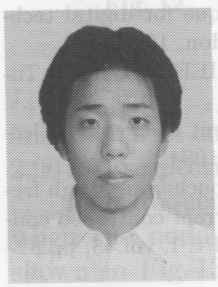

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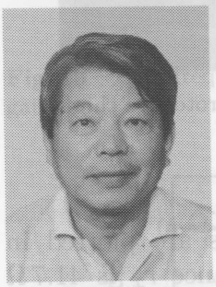

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