Transactions Briefs

A Switched-Capacitor Multiplier/Divider with Digital and Analog Outputs

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Abstract—A novel switched-capacitor circuit is proposed for digital multiplication and division. The inputs (two binary numbers) are first converted to analog charges by means of binary-weighted capacitor arrays. Then, multiplication or division is performed between these charges to provide the product or ratio in the form of an analog voltage. Finally, the resulting analog voltage is converted to a binary number by successive-approximation analog-to-digital (A/D) conversion. An error analysis using the charge conservation equation has shown that a 10-bit accuracy is obtainable using this technique with presently available MOS technology. An experimental circuit was built and tested. The results confirmed the principles of operation.

Manuscript received April 8, 1984; revised September 23, 1983. This paper was based on work supported in part by the National Science Foundation under Grant ECS-8105166.

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I. Introduction

The use of digital techniques to perform the processing of analog signals is common practice. In the present work, an attempt is made to perform the reverse; an analog circuit is described which can perform the multiplication or division of two digital signals. Used simply as a digital multiplier or divider, the circuit is inferior to an all-digital stage performing the same function in terms of operating speed. Also, it may require as much or more silicon area (in spite of its simpler structure) as its digital counterpart. It is, however, much more versatile: the same circuit can multiply or divide two digital numbers, and the output is available in both analog and digital forms. In addition, the circuit can perform as a programmable amplifier, or either a digital to analog (D/A) or an analog to digital (A/D) converter.

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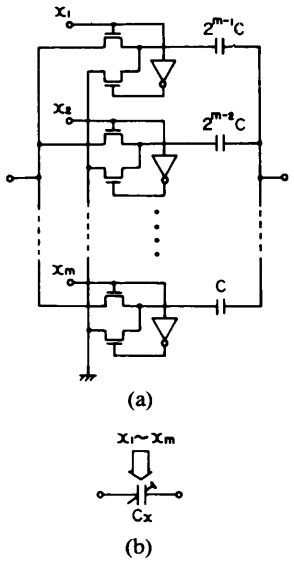

Fig. 1. An m-bit programmable binary-weighted capacitor array (a) and its symbol (b).

Finally, it can readily be modified to act as a high-accuracy capacitance bridge with digital read-out, as will be described in a forthcoming publication.

It is hoped that this circuit will also serve as an illustration of the potentials of high-accuracy MOS analog circuitry in general signal processing, analog, digital, or hybrid.

II. Circuit Description

In what follows, x and y are binary numbers m-bit and n-bit long, respectively, in the forms

$$x = x_1 \cdot 2^{-1} + x_2 \cdot 2^{-2} + \cdots + x_m \cdot 2^{-m} \tag{1}$$

$$y = y_1 \cdot 2^{-1} + y_2 \cdot 2^{-2} + \cdots + y_n \cdot 2^{-n}. \tag{2}$$

The signs of x and y are represented by the additional bits x_{m+1} and y_{n+1}, respectively, which assume the value "1" when x and y are negative and "0" when they are positive. The operation executed is $x \cdot y$ or x/y. When multiplication is carried out, x is the multiplicand and y is the multiplier. The product z is stored in a register of $(m+n)$-bit length. When division is performed, x is the dividend and y is the divisor. To avoid an overflow, the divisor y is normalized so that its MSB, y_1, is 1. The ratio is truncated to $(m+n)$ bits, and is stored in the z register. Each number can be converted to the appropriate charge by means of a binary-weighted capacitor array [1], as shown in Fig. 1. This conversion is the basis of the digital operation involved here.

Fig. 2(a) shows the schematic diagram of the overall circuit. It consists basically of three parts; the D/A converter, the successive-approximation A/D converter, and the sample and hold (S/H) circuit. The D/A converter is formed by the capacitor arrays C_x, C_y, and C_z, the feedback capacitors C_1 and C_2, and the op-amp A_1. This converter also forms the successive-approximation A/D converter in conjunction with op-amp A_2 and the $(m+n)$-bit shift register (z register).

The circuit can be in one of two states; the XEC (execute) state during which the digital operation is being executed, or the OUT (output) state during which the result is available in the z register. The XEC state is further divided into the DA and AD sub-states during which the D/A conversion and the successive-approximation A/D conversion are performed, respectively. The corresponding "state" signals and the selection signal SS of the reference sources control the operation of the circuit. Their timing is shown in Fig. 2(b). The operation cycle is initiated by

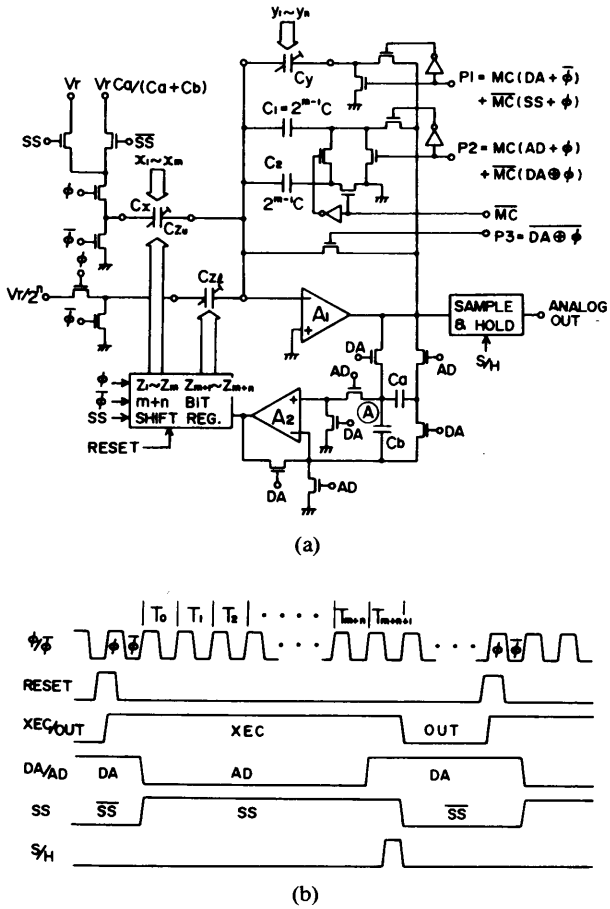

Fig. 2. (a) The schematic diagram of the switched-capacitor digital multiplier/divider, where AD, DA, and SS are the state signals controlling its operation. Their timing sequence is shown in (b).

the RESET signal sent from an external device to inform the circuit of the receipt of the previous result. Upon receiving this signal, the circuit clears the z register and, at the rising edge of the ϕ clock signal immediately following it, terminates the OUT state and initiates the DA substate of the XEC state. This substate lasts only one clock period, to be followed by the AD substate. The AD state lasts $m+n+1$ clock period. After one clock period in the DA state, the circuit returns again to the OUT state. This state continues until the next RESET signal starts a new cycle of operation.

The mode control MC signal in Fig. 2(a) selects the actual operation performed. When MC = 1, the circuit executes multiplication, and when $\overline{\text{MC}} = 1$, it performs division. The detailed description of the operation is given next.

A. Multiplication

Since now $\overline{\text{MC}} = 0$, the capacitors C_1 and C_2 (Fig. 2(a)) are connected in parallel to form a feedback capacitor C_F of value $2^m C$. The circuit configuration in the DA and AD states are thus as shown in Fig. 3(a) and (b), respectively.

A-1. Operation in the DA State

The multiplicand x programs the array C_x to set its value to $2^m Cx$. Op-amp A_1 with capacitors C_x and C_F forms an offset-free D/A converter [2], [3]. It converts the value of x into the analog voltage V_x by charging C_x to the scaled reference voltage $C_a V_r/(C_a + C_b)$ in the $\phi = 1$ phase and then discharging it into C_F in the $\bar{\phi} = 1$ phase. The output voltage of A_1 is then

$$V_x = \frac{C_x}{C_F} \cdot \frac{C_a V_r}{C_a + C_b} = x \frac{C_a V_r}{C_a + C_b}. \tag{3}$$

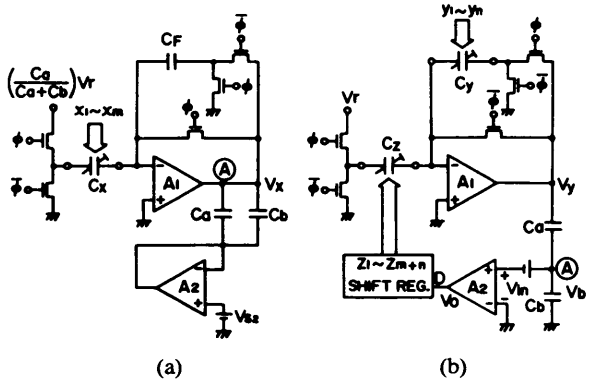

Fig. 3. Circuit configurations for multiplication: (a) The D/A converter (DA state). (b) The successive-approximation A/D converter (AD state).

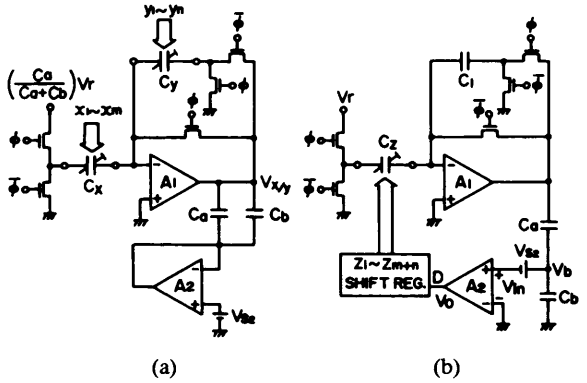

Fig. 4. Circuit configurations for division: (a) The D/A converter (DA state). (b) The successive-approximation A/D converter (AD state).

V_x is applied to the top terminal of the parallel-connected capacitors C_a and C_b.

Op-amp A_2 is connected as a voltage follower with a grounded input. Its output is thus its own input-referred offset voltage V_{s_2} and this is applied to the bottom terminals of C_a and C_b. The voltage V_b across C_b is $V_x - V_{s_2}$, which will be applied, in series with the offset voltage of A_2, to the noninverting input terminal of A_2 in the subsequent AD state.

A-2. Operation in the AD State

The multiplier y programs the array C_y to set its value to $2^m Cy$. The array C_x is now accessed by the m MSB's of the z register. The remaining n bits of the z register program the array C_{zl}. These two arrays form in combination the array C_z for the product z. Op-amp A_1 and the arrays C_z and C_y now form an offset-free D/A converter. The capacitors C_a and C_b are in this state connected in series; their initial voltage is V_b, as acquired in the previous DA state. Op-amp A_2 operates as a comparator. The whole circuit, including the z register, now forms a successive-approximation multiplying A/D converter (Fig. 3(b)).

The conversion begins after C_F is discharged in the T_0 period (Fig. 2(b)). In time slot T_1, the capacitance of the array C_z is set to $2^{m-1}C$ by assuming temporarily $z_1 = 1$ and is charged to the reference voltage V_r in the $\phi = 1$ phase. The input voltage V_{in} of the comparator is then the weighted sum of the present output V_y of A_1, the voltage across C_b, and the offset voltage of A_2:

$$V_{\text{in}} = \frac{C_a}{C_a + C_b} V_y + V_b + V_{s_2} = \frac{C_a V_r}{C_a + C_b}\left(\frac{C_x}{C_F} - \frac{2^{m-1}C}{C_y}\right). \quad (4)$$

The offset voltage of A_2 does not appear in (4) because it is cancelled. The offset voltage of A_1 is not included either, because of the offset-free D/A conversion. The comparison process is, therefore, offset free. Depending on the polarity of V_{in}, the comparator A_2 keeps z_1 as 1 (if V_{in} is positive) or resets z_1 to 0 (if V_{in} is negative).

In the next time slot T_2, the capacitor of the array C_z corresponding to z_2 is accessed similarly, while the value of z_1 is stored. V_{in} is now

$$V_{\text{in}} = \frac{C_a V_r}{C_a + C_b}\left(\frac{C_x}{C_F} - \frac{z_1 \cdot 2^{m-1}C + 2^{m-2}C}{C_y}\right). \quad (5)$$

A_2 keeps z_2 as 1 if V_{in} is positive and resets z_2 to 0 otherwise. This process is repeated $(m+n)$ times, until a charge balance is reached on C_b so that

$$\frac{Q_x}{C_F} = \frac{Q_z}{C_y} \quad (6)$$

holds, where

$$Q_x = C_x V_r \quad (7)$$

$$Q_z = C_{zu} V_r + C_{zl} V_r / 2^n = \left(z_1 \cdot 2^{-1} + z_2 \cdot 2^{-2} + \cdots + z_{m+n} \cdot 2^{-(m+n)}\right) 2^m C \cdot V_r = C_z V_r. \quad (8)$$

The $(m+n)$-bit shift register thus stores the product $z = x \cdot y$.

B. Division

In this operation, $\overline{\text{MC}} = 1$ and, therefore, the capacitor C_2 is short-circuited. The circuit configurations in the DA and AD states are then as shown in Fig. 4(a) and (b), respectively. During the DA state, the arrays C_x and C_y are set to the values $2^m Cx$ and $2^m Cy$, respectively. These two arrays and op-amp A_1 form an offset-free D/A converter which converts the ratio x/y into the analog voltage $V_{x/y}$ by charging C_x to the scaled reference voltage $C_a V_r/(C_a + C_b)$ in the $\phi = 1$ phase and then discharging it into C_y in the $\bar{\phi} = 1$ phase. The output voltage of op-amp A_1 is then

$$V_{x/y} = \frac{C_a V_r}{C_a + C_b} \cdot \frac{C_x}{C_y}. \quad (9)$$

Thus $V_b = V_{x/y} - V_{s_2}$ is generated as described in Section II-A-1.

In the subsequent AD state, the analog voltage $V_{x/y}$ is converted to an $(m+n)$-bit number z by the successive-approximation A/D converter shown in Fig. 4(b). The conversion process is the same as that described in the multiplier and is again practically offset-free if the open-loop gains of A_1 and A_2 are very high. The charge on C_b is now approximately balanced so that

$$\frac{Q_x}{C_y} \simeq \frac{Q_z}{C_F} \quad (10)$$

holds, where $C_F = C_1 = 2^{m-1}C$ and Q_x and Q_z are given by (7) and (8), respectively. The ratio z rounded to $(m+n)$ bits is stored in the z register.

The circuit in Fig. 4 can accomplish other functions as well. If, e.g., an analog signal V_s is applied at the terminal where the scaled reference voltage $C_a V_r/(C_a + C_b)$ was previously connected, then noninverting amplification with a programmable gain x/y is obtained by the circuit of Fig. 4(a). The successive-approximation A/D converter shown in Fig. 4(b) then provides a digital output z such that

$$V_s = \left(\frac{y}{x} \cdot \frac{2C_a}{C_a + C_b}\right) z V_r \quad (11)$$

holds. Therefore, if x and y are set so that the parenthesized

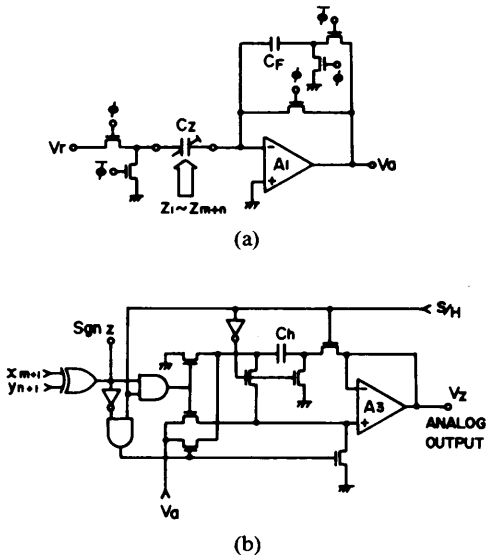

Fig. 5. Circuit configurations for analog output: (a) The D/A converter in the T_{m+n+1} period. (b) The sample and hold circuit.

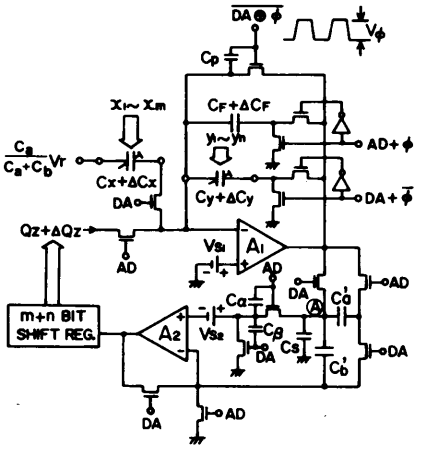

Fig. 6. The schematic diagram of the multiplier circuit including the important parasitic elements.

factor equals 1, the divider accomplishes an $(m+n)$-bit A/D conversion.

III. Analog Output

In either multiplication or division operation, the circuit returns to the DA state at the onset of the T_{m+n+1} period. The circuit diagram of the stage containing A_1, valid in this period, is shown in Fig. 5(a). It is an offset-free $(m+n)$-bit D/A converter, providing the analog voltage $V_a = |z|V_r$ which can be sampled and held by the added circuit shown in Fig. 5(b). This circuit forms a voltage follower when the sign of the product or the ratio, sgn z, is positive. When sgn z is negative, it forms a voltage inverter switch [4] and provides the output with a negative polarity. In either connection, the output is offset-free because the offset voltage of A_3 is detected and held in the holding capacitor C_h in the "sample" period, and then cancelled in the subsequent "hold" period. The clock feedthrough has no effect on the output either, since each node is connected either to a voltage source or to ground.

III. Accuracy

The charge balance relations given in (6) and (10) do not take into account nonideal circuit conditions such as capacitance mismatch, the offset voltages and the finite gains of the op-amps, parasitic capacitances, and the feedthrough from the clock signals. In this section, the charge balance equation valid under practical conditions is given, to obtain an estimate of the accuracy of the operation.

The circuit shown in Fig. 2(a) contains, in fact, many parasitic capacitances not shown in the figure. Those parasitic capacitances, however, which are connected or switched only between a voltage source and ground have no effect on the operation. This is also true for those gate–source and gate–drain feedthrough capacitances of the MOS switches which are connected between voltage sources and ground only. Furthermore, some of these feedthrough capacitances are connected to the same nodes and driven by the complementary clock signals, such as C_α and C_β in Fig. 6. These paired capacitances can be also neglected to a first-order approximation. On the basis of the above, we obtain the circuit in Fig. 6 as the practical circuit model of Fig. 2(a).

Referring to Fig. 6, we can obtain the expanded charge balance equation

$$\frac{C_x'V_r\cdot C_a/(C_a+C_b)+C_pV_\phi+\left(C_x'+C_F'+C_p\right)V_{s_1}/(1+A_1)}{C_F'\left(1+\frac{1}{A_1}\left(1+\frac{C_x'+C_p}{C_F'}\right)\right)}+\frac{V_{s_2}}{1+A_2}$$

$$-\frac{C_a'}{C_a'+C_b'+C_s}\cdot\frac{Q_z+\Delta Q_z-C_pV_\phi-\left(C_z'+C_y'+C_p\right)V_{s_1}/(1+A_1)}{C_y'\left(1+\frac{1}{A_1}\left(1+\frac{C_z'+C_p}{C_y'}\right)\right)}=0. \quad (12)$$

Here, V_ϕ is the amplitude of the clock signal applied to the reset switch. The primed capacitances (C_x', C_F', etc.) denote the actual values including the inaccuracies, while ΔQ_z represents the error in Q_z and hence in the output z due to the nonideal factors.

A detailed analysis of the terms contributing to ΔQ_z, omitted in the interest of brevity (but available from the authors upon request), reveals that the expected circuit yield for a 10-bit accuracy is about 38 percent; for a 9-bit accuracy, about 68 percent; and for an 8-bit accuracy, about 95 percent. Identical conclusions hold for the accuracy when the circuit is used as a divider.

IV. Experimental Verification

A 4×4-bit multiplier/divider, based on the scheme of Fig. 2(a), has been constructed using CMOS transmission gates, an LM347 JFET op-amp, and discrete capacitors. All arrays consisted of 2, 1, 0.5, and 0.25 nF capacitors. All other capacitances were chosen to 2 nF. The supply voltages were ±6 V.

Fig. 7 shows the waveforms observable when the digital multiplication $(-0111)\times(1100)$ was executed. The zero level, the circuit states, and the timing are also indicated in the figure. The reference voltage V_r was 3.6 V. The upper trace shows the voltage V_A at node Ⓐ during the XEC state (Fig. 2). The initial value is the small offset voltage of A_1 appearing at node Ⓐ during the

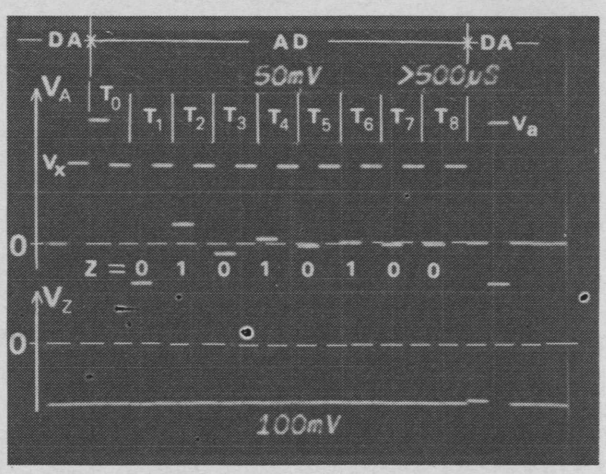

Fig. 7. Waveforms appearing when the digital operation $(-0111)\times(1100)$ was executed. *Upper trace:* The voltage at node (A) during the XEC state. *Lower trace:* The output voltage of S/H circuit. (The actual vertical scale is ten times that indicated in the figure, since a 10:1 oscilloscope probe was used.)

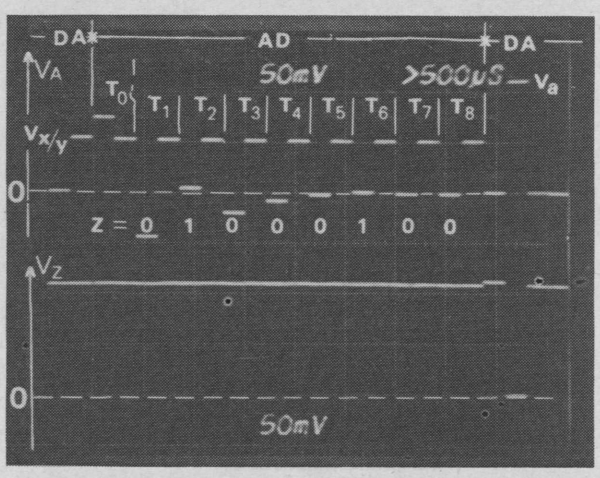

Fig. 8. Waveforms appearing when the digital operation $(1000)\div(1111)$ was executed. *Upper trace:* The voltage at node (A) during the XEC state. *Lower trace:* The output voltage of S/H circuit. (The actual vertical scale is ten times that indicated in the figure, since a 10:1 oscilloscope probe was used.)

$\phi=1$ phase in the DA substate of XEC. In the next $\bar{\phi}=1$ phase, the multiplicand (7/16) is converted to the analog voltage $V_x = (7/16)\times(3.6/2) \simeq 0.79$ V. Notice that during the subsequent AD substate, this voltage is held in C_b and V_A is the sum of V_x and half of the output voltage of op-amp A_1. During the $\phi=1$ phase in T_0, 0.5 V can be seen superposed on V_x due to the discharge of C_F caused by $P_2=1$. In the $\phi=1$ phase in T_1, z_1 is tested. The voltage V_A in this phase is $0.79-(2/3)\times3.6/2 \simeq -0.41$ V, thus the value "0" is assigned to z_1. Inspecting the voltage levels in the subsequent seven $\phi=1$ phases, we can read the product (01010100), as indicated in the Figure. This is the correct answer. The circuit now returns to the DA substate and, in the $\bar{\phi}=1$ phase, converts the product (21/64) into the analog voltage $V_a=1.18$ V. The lower trace is the output V_z of op-amp A_3 (Fig. 5), showing how V_a is sampled, inverted since the sgn z is negative, and held by the S/H circuit.

Fig. 8 shows the waveforms observable when the digital division $(1000)\div(1111)$ was executed. In division, the output voltage of A_1 can be as high as $2V_r$ because the ratio z can assume the maximum value 2. Therefore, the reference voltage V_r was reduced to 2 V to prevent the op-amp A_1 from being saturated. The timing of the trace is the same as that in Fig. 7. The upper trace (the voltage V_A at node (A)) shows the process producing the ratio (01000100). This ratio is correct up to 8 bits. The lower trace shows how the ratio V_z in analog form is sampled and held by the S/H circuit.

V. Conclusion

A switched-capacitor circuit was presented for the multiplication or division of two digital numbers. The output is available in both analog and digital forms. The principles of operation have been confirmed experimentally. The design criteria for IC realization are summarized as follows:

1) The gains of the op-amps do not directly affect the accuracy. This is because the charge balance is achieved by the iterative use of one op-amp. Therefore, the reduction of the offset voltage should be emphasized in the design of the op-amps, rather than a very high gain which would also degrade the slew rate.

2) To make the unit capacitors in the arrays small, and thereby to save the chip area, clock feedthrough cancellation [5], [6] should be provided with the reset switches.

3) The holding capacitors C_a and C_b should be made as large as practical. With these precautions, the accuracy is limited only by the mismatches in the capacitor arrays. Numerical calculations using available data on MOS capacitors indicate that 8, 9, or 10-bit accuracy is obtainable with 95, 68, or 38 percent yields, respectively.

The main advantage of the proposed circuit over a conventional digital multiplier is its versatility: It can perform, besides digital and hybrid multiplication and division, also programmable amplification as well as D/A and A/D conversion. The main disadvantage is the lower operating speed, estimated as 2 to 3 times slower than that of a serial–parallel CMOS digital multiplier. In addition to its versatility, the proposed circuit can be implemented by using a relatively small number of components. Counting a unit capacitor as being equivalent to a MOSFET, a 4×4-bit multiplier can be built by about 500 MOSFET's. A conventional 4×4-bit serial-parallel multiplier, on the other hand, requires about 700 devices [7], [8]. The proposed circuit, however, may require a slightly larger area when integrated on Si chip because the analog MOSFET's involved in the op-amps require larger gate areas than digital devices. This can be remedied by using the much simpler dynamic op-amps first suggested by Copeland and Rabaey [9].

Acknowledgment

The authors are grateful to Prof. Ken Martin of UCLA for useful discussions. The first author also thanks the Ministry of Education, Japan, for supporting his stay at UCLA.

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