An Autoranging Switched-Capacitor Analog-to-Digital Converter

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Abstract—**A novel switched-capacitor serial analog-to-digital (A/D) converter is developed based on the dual-slope integration. The analog voltage being converted is first accumulated into the capacitor in the form of charge. The quantized reference charge is then extracted from the accumulated signal charge until the voltage across the capacitor becomes zero. To increase the resolution, the autoranging function is incorporated which changes the charge accumulation count in 2's geometric progression manner according to the input analog voltage. The resultant counts in charge accumulation and extraction give the exponent and the mantissa, respectively, of the floating-point binary representation. A resolution of 10 bits with the additional $2\frac{1}{2}$ bits for the exponent is achieved by the prototype converter built using discrete components.**

I. Introduction

BY VIRTUE OF its excellent zero stability, linearity, and absolute accuracy, the dual-slope analog-to-digital (A/D) converter has made great impact on low-speed precision instrumentation and measurement [1]. Its monolithic implementation is desired highly to reduce the cost, but is difficult, if not impossible, with the presently available bipolar technology because of the large integration time constant involved. To solve this problem, the CMOS realization which replaces a conventional *RC* integrator with the switched-capacitor integrator has been proposed [2]. Such a simple replacement, however, requires the capacitance ratio of 2^n for n-bit resolution. In addition, the lower conversion speed is inevitable because of the slower switching speed of CMOS circuitry.

To alleviate these difficulties, the floating-point technique is applied to the switched-capacitor dual-slope A/D converter. A novel method is used to eliminate the programmable-gain amplifier which would otherwise be required for scaling the input analog voltage. Following this introductory section, the paper describes its circuit configuration, the principles of operation, and the experimental results obtained by the prototype converter.

II. Circuit Description

Fig. 1 shows the circuit diagram of the switched-capacitor dual-slope A/D converter. Here, V_x is the analog voltage to be converted into a binary number with reference to V_r. V_{ar} is the threshold voltage for autoranging. The whole circuit consists of three main blocks; the switched-capacitor integrator, comparator, and digital control circuit. The offset-free and parasitic-insensitive configuration is adopted for the integrator [3], [4]. The circuit operation is divided into three states; the 'Polarity' (POL) state to detect the polarity of an input analog voltage, the 'Accumulation' (ACC) state to accumulate the signal charge into the capacitor C_2, and the 'Extraction' (EXT) state to extract the quantized reference charge from the accumulated signal charge. The operation in each state is controlled by the nonoverlapping two phase clocks ϕ and $\bar{\phi}$. Their timing diagram is shown in Fig. 2. In this diagram, $\phi_a(n)$ is the autoranging pulse generated by the counter when it counts 2^n ($n = 0, 1, \cdots, 4$) clocks in 'ACC' state. The leading reset signal resets the integrator and the counter, thereby initiating the A/D conversion. The operation in each state will be described in detail in the following.

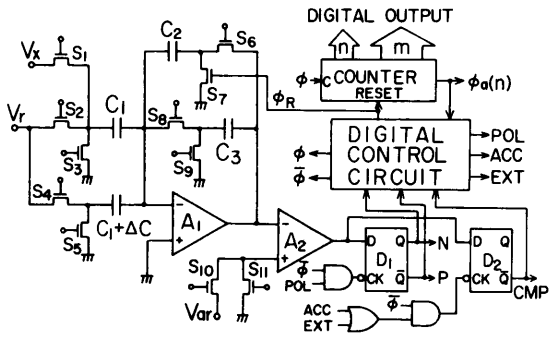

Fig. 1. The circuit diagram of the autoranging A/D converter.

A. Operation in 'POL' State

In this state, S_{11} is kept "on", and S_2, S_4, S_5, and S_{10} are kept "off." The analog circuitry valid in this state thus becomes as shown in Fig. 3. Op amp A_1 and capacitors C_1, C_2, and C_3 form a noninverting amplifier, to amplify the analog input voltage V_x. The output voltage of A_1 is thus

$$V_o = (C_1/C_2)V_x. \tag{1}$$

Op amp A_2 and the D flip-flop D_1 form a comparator to test the polarity of V_o. If it is positive, then P is set to 1. Otherwise, N is set to 1. This completes the operation in this state and the circuit turns into 'ACC' state.

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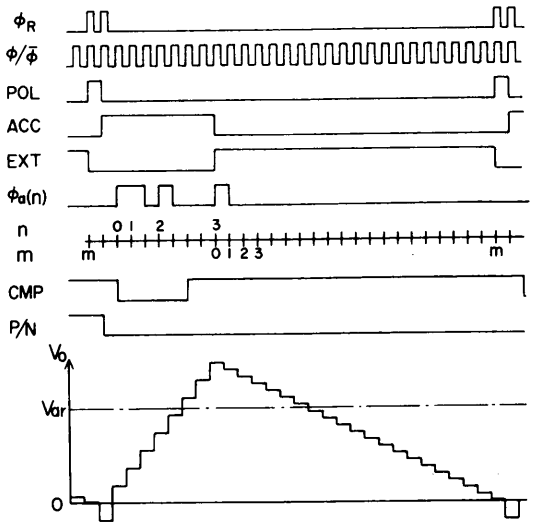

Fig. 2. The timing diagram of digital control signals and the output waveform of op amp A_1.

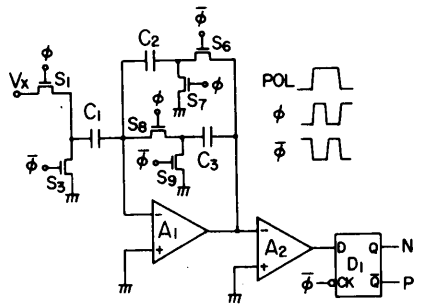

Fig. 3. The analog circuitry in the 'POL' state.

B. Operation in 'ACC' State

The switch S_{10} is kept "on," while S_2, S_4, S_5, and S_{11} are kept "off" during this state. The analog circuitry valid in this state thus becomes as shown in Fig. 4. Op amp A_1 and capacitors C_1 and C_2 now form the noninverting integrator if $P = 1$ and the inverting integrator if $N = 1$. After discharging the charge stored in C_1 and C_2 in the preceding 'POL' state, the integrator accumulates the incremental signal charge C_1V_x onto the feedback capacitor C_2, to produce the positive output voltage V_o, as shown in Fig. 2. The capacitor C_3 is incorporated to hold the integrator output voltage and thereby to make the integrator operation insensitive to the open-loop gain of op amp A_1 [3]. The integrator output V_o in the ϕ phase is compared with the threshold voltage V_{ar} by the comparator A_2. If $V_o < V_{ar}$, then the comparator output CMP is kept low, to continue the charge accumulation. When $V_o \geqq V_{ar}$, the autoranging pulse $\phi_a(n)$ becomes effective to stop the charge accumulation. Therefore, if the input analog voltage V_x is in the range between $V_{ar}/2^n$ and $V_{ar}/2^{n-1}$, the charge accumulation is repeated 2^n times. The signal charge Q_{acc} accumulated upon C_2 is thus

$$Q_{acc} = 2^n C_1 V_x. \tag{2}$$

It should be noticed here that the charge accumulation count 2^n corresponds to the binary-weighted programmable gain of a conventional floating-point A/D converter.

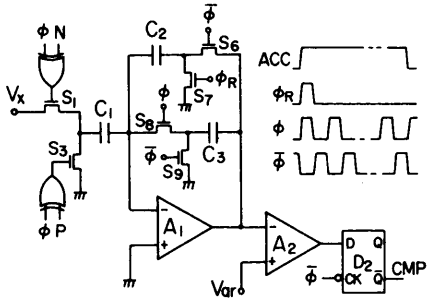

Fig. 4. The analog circuitry in the 'ACC' state.

C. Operation in 'EXT' State

In this state, S_{11} is kept "on," while S_1, S_7, and S_{10} are kept "off." The analog circuitry valid in this state thus becomes as shown in Fig. 5. Op amp A_1 and capacitors C_1, $C_1 + \Delta C$, and C_2 form the integrator. The reference voltage V_r is now applied, in place of V_x, to the integrator. In each $\bar{\phi}$ phase, the capacitor C_1 deposits the charge C_1V_r upon C_2, while the capacitor $C_1 + \Delta C$ draws the charge $(C_1 + \Delta C)V_r$ out of C_2. Thus the net charge Q_r, referred here to as the quantized reference charge, extracted from C_2 in each $\bar{\phi}$ phase is ΔCV_r. This charge extraction continues until the integrator output voltage becomes zero.

Let the quantized reference charge be extracted m times. Then the total charge extracted is

$$Q_{ext} = m\Delta CV_r. \tag{3}$$

Since $Q_{acc} = Q_{ext}$, one obtains

$$V_x = \frac{m}{2^n} \cdot \frac{\Delta C}{C_1} \cdot V_r = (m_1 2^{-1} + m_2 2^{-2} + \cdots + m_M 2^{-M}) 2^{-n} \cdot V_{FS} \tag{4}$$

where $V_{FS} = 2^M(\Delta C/C_1)V_r$ is the full scale voltage of the A/D converter with M-bit resolution. Therefore, for given capacitance ratio $\Delta C/C_1$ and reference voltage V_r, the floating-point binary number with n and m as its exponent and mantissa, respectively, measures the input analog voltage. The A/D conversion insensitive to the capacitance ratio $\Delta C/C_1$ is also possible with this circuit, which will be described in the Appendix.

III. Conversion Accuracy

The switched-capacitor integrator is configured such that the offset voltage of op amp and parasitic capacitances have no effect upon its operation. The finite open-loop gain of op amp reduces the charge transfer efficiency. The reduction is, however, common to both the signal and quantized reference charges. Thus the finite open-loop gain does not disturb the charge balance, either. The main error source which limits the resolution of the present A/D converter is, therefore, the feedthrough of clock signals through gate–source and gate–drain capacitors of MOS switches.

Let the feedthrough charge referred to the inverting input terminal of op amp A_1 be Q_f. Then, the total charge, including the contribution of Q_f, accumulated upon C_2 in

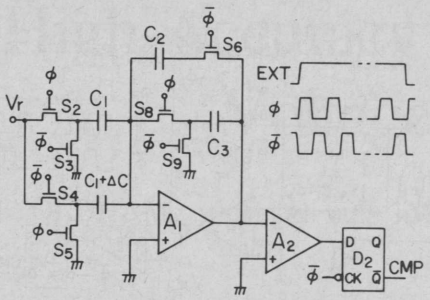

Fig. 5. The analog circuitry in the 'EXT' state.

the 'ACC' state is $2^n(C_1V_x + Q_f)$, while the total extracted charge is $m'(Q_r - Q_f)$, where m' is the erroneous count caused by the feedthrough charge. Since these charges balance, we have

$$2^n(C_1V_x + Q_f) = m'(Q_r - Q_f). \tag{5}$$

Equation (5) is plotted in Fig. 6 together with the ideal transfer function. It is evident by inspection that the feedthrough charge in the 'ACC' state causes the offset error and that in the 'EXT' state causes the gain or scale error.

For the offset error to be less than 1LSB, the following condition should be satisfied:

$$Q_f < Q_r/(2^n + 1). \tag{6}$$

The scale error ϵ_s (in %) and the differential nonlinearity ϵ_d (in 1LSB unit) are given by

$$\epsilon_s = \epsilon_d = Q_f/(Q_r - Q_f). \tag{7}$$

In an IC realization using advanced MOS technologies, the feedthrough charge Q_f can be reduced to 5 fQ by accommodating the clock feedthrough cancellation scheme [5], while the signal charge as large as 500 pQ could be stored in C_2. Choosing $Q_r = 0.5$ pQ and $n \leqq 4$, one can obtain the resolution of 10 bits and the dynamic range of 84 dB with no offset error. While this dynamic range is sufficient for most application, the scale error amounts to 1 percent. In addition, the uncertainty of the capacitance ratio $\Delta C/C_1$ also causes the scale error. This error, however, can be eliminated, without degrading the differential linearity, by adjusting the reference voltage V_r.

IV. Experimental Results

To confirm the principles of operation, a prototype converter was built using discrete components. The capacitors were: $C_1 = 3.34$ nF, $C_2 = 3.34$ nF, and $C_3 = 5.62$ nF. The op amp used was LF347. The reference voltage V_r and the threshold voltage V_{ar} were set to 1 V and 3 V, respectively.

Fig. 7 shows the waveform observed at the output of op amp A_1 when the analog voltage $V_x = -0.5$ V was applied to the converter. The large capacitance difference $\Delta C = 360$ pF was intentionally chosen so that the waveform demonstrates the operation in each state. In the 'POL' state, the negative polarity of V_x is detected and N is set to 1. In the 'ACC' and 'EXT' states, $n = 3$ and $m = 37$ are measured, respectively. The measured voltage

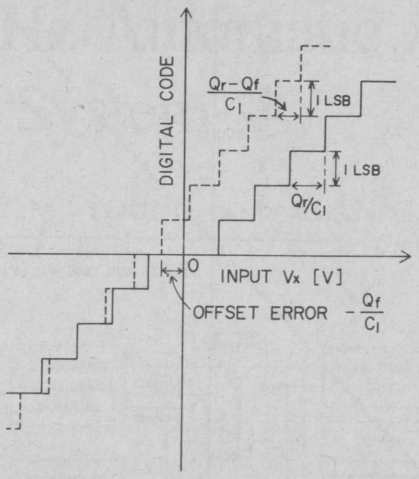

Fig. 6. The ideal (solid line) and erroneous (dotted line) input–output characteristic of the present A/D converter.

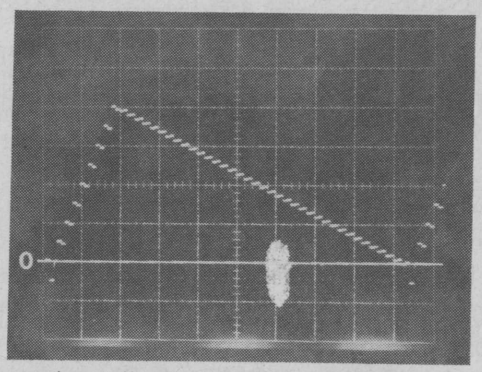

Fig. 7. The experimentally observed output waveform of the prototype A/D converter. Horizontal scale: 0.2 ms/div; Vertical scale: 1 V/div.

V_x is thus $-(37/2^3) \times (360/3340) \times 1 = -0.499$ V, which agrees with the applied voltage.

The digital outputs and the nonlinearity error of the prototype converter obtained for the analog voltage ranging from -5 to $+5$ V are shown in Fig. 8(a) and (b), respectively. The capacitance difference ΔC is set to 5 pF. Good linearity with the nonlinearity error less than $\frac{1}{2}$ LSB can be seen. The resolution of 10 bits with additional $2\frac{1}{2}$ bits for the exponent confirms the accuracy estimate.

V. Conclusions

An autoranging serial A/D converter based on the dual-slope integration was described. The chip area required for the implementation is very small because of small device count involved. Therefore, as low cost and high precision A/D converter, it will find wide application in instrumentation and measurement field.

Appendix

The digital output given by (4) depends on the capacitance ratio of $\Delta C/C_1$. This dependence can be eliminated by slightly modifying the circuit operation in the 'ACC' state as shown in Fig. 9. Op amp A_1 and capacitors C_1, $C_1 + \Delta C$, and C_2 form the integrator. Switches S_1 and S_5 are driven by $\bar{\phi}$, while S_3 and S_4 are driven by ϕ, if $P = 1$. If $N = 1$, on the other hand, S_1 and S_5 are driven by ϕ, while S_3 and S_4 are driven by $\bar{\phi}$. Therefore, the capacitor C_1 draws the positive charge C_1V_x from C_2, while the

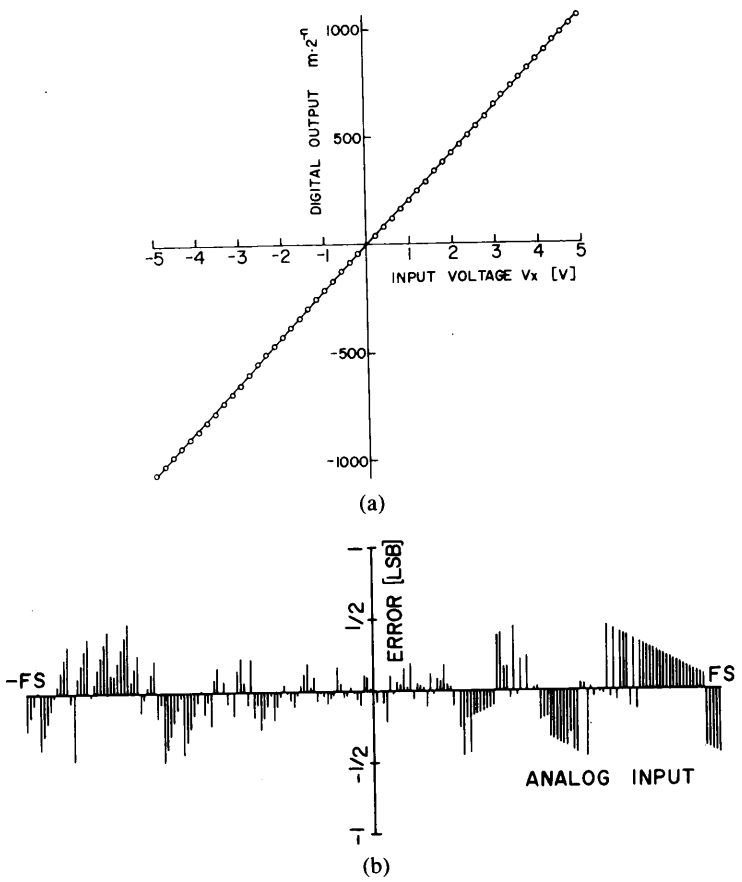

Fig. 8. (a) The digital outputs, and (b) the nonlinearity error of the prototype A/D converter.

capacitor $C_1 + \Delta C$ deposits the positive charge $(C_1 + \Delta C)V_x$ upon C_2. Thus the net charge accumulated onto the capacitor C_2 is ΔCV_x. The signal charge Q_{acc} accumulated upon C_2 is thus

$$Q_{acc} = 2^n \Delta C V_x. \tag{A-1}$$

The circuit operation in the 'EXT' state is the same as before and extracts the charge

$$Q_{ext} = m\Delta C V_r. \tag{A-2}$$

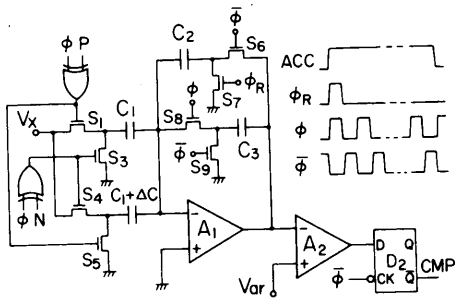

Fig. 9. The analog circuitry in the 'ACC' state modified for the ratio-independent A/D conversion.

Since $Q_{acc} = Q_{ext}$, one obtains

$$V_x = \frac{m}{2^n} V_r. \tag{A-3}$$

The A/D conversion based on (A-3) was also confirmed by a prototype converter built using discrete components.

Acknowledgment

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