A Relaxation-Oscillator-Based Interface for High-Accuracy Ratiometric Signal Processing of Differential-Capacitance Transducers

Kouji Mochizuki, Kenzo Watanabe, *Fellow, IEEE*, Takashi Masuda, and Motoyasu Katsura

***Abstract*—For high-accuracy signal processing of differential-capacitance transducers, an interface circuitry is developed based on a relaxation oscillator. Two capacitors of the transducer are multiplexed by diode switches to form the op-amp-based integrator. The duty ratio of the oscillator output then measures the ratio of two capacitances. A circuit analysis shows that the interface can detect the capacitance change as small as 0.01% of the total capacitance. Experimental results are also given to confirm the analysis.**

***Index Terms*—Analog circuit, capacitive transducer, intelligent transducer, pressure measurement, relaxation oscillator, signal processing.**

I. Introduction

DIFFERENTIAL capacitance transducers consisting of ganged two capacitors are widely used for detecting pressure difference, linear displacement, and rotational angle [1], [2]. Their principles of detection are based on the complementary changes of two capacitors with the measurand. The capacitance change may be linear or nonlinear. In either case, the accurate and linear representation of the measurand can be obtained by dividing the capacitance difference between two capacitors by their sum. Several techniques have so far been proposed for such a ratiometric signal processing, including switched-capacitor analog-to-digital (A/D) [3], [4], capacitance-to-frequency [5], [6], capacitance-to-phase [7], and capacitance-to-voltage conversion [8].

This paper describes yet another simple interface for the ratiometric signal processing. The interface is basically a relaxation oscillator. Such a configuration has been applied widely to capacitive sensors to detect their capacitance change in the frequency form [5], [6]. Different from these applications, the interface presented here detects the ratio of two capacitances in the form of the duty ratio. This signal processing in the time domain allows high-speed measurements. In the followings, the interface configuration, the ratiometric operation, the accuracy estimate, and experimental results will be described.

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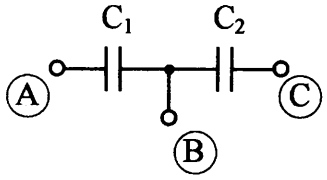

Fig. 1. An equivalent circuit of a differential capacitance transducer.

II. Transducer Model

A differential capacitance transducer can be represented by two capacitors with a common electrode, as shown in Fig. 1 [8].

In a linear displacement encoder, the areas of the electrodes change linearly with the displacement x. The capacitances C_1 and C_2 can then be expressed as follows:

$$C_{1,2} = \frac{C_0}{2}(1 \pm x) \tag{1}$$

where C_0 is a total capacitance of the transducer. In a differential pressure transducer, on the other hand, the spacings between the electrodes change linearly with the pressure difference x. Therefore, C_1 and C_2 are expressed as

$$C_{1,2} = \frac{C_0}{2}\frac{1}{1 \mp x}. \tag{2}$$

Whether the capacitance change is linear or hyperbolic, the measurand x can be detected independently of the total capacitance C_0 by the following ratiometric operation:

$$x = \frac{C_1 - C_2}{C_1 + C_2} = \frac{2C_1}{C_1 + C_2} - 1. \tag{3}$$

III. Interface Circuitry

The circuit diagram of the interface circuit to perform the ratiometric operation is shown in Fig. 2. The interface consists of an integrator followed by a comparator. The output of the comparator is fed back to the integrator to sustain the relaxation oscillation.

Two capacitors C_1 and C_2 of a differential capacitance transducer are multiplexed by diodes D_1 and D_2 to form the integrator A_1. The multiplexing is made automatically depending on the outputs V_1 and V_4 of the integrator and the comparator, respectively.

For the moment, diodes are assumed to be ideal switches. This assumption is reasonable because the diodes are incorporated into the feedback path of the op-amp A_1. $R_1 = R_2 = R_3$

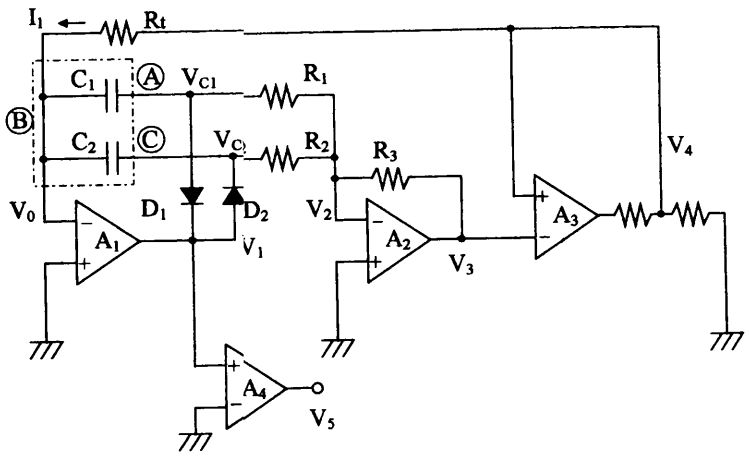

Fig. 2. The circuit diagram of the interface.

is also assumed. Op-amp A_2 then forms the adder with the weight -1. The adder operates, in fact, as the inverting voltage follower, because D_1 and D_2 never turn on simultaneously.

Depending on the switch conditions, the operation of the oscillator is divided into four states $T_i (i = 1, 2, 3, 4)$. The integrator and waveforms in each state are shown in Figs. 3 and 4, respectively.

In the T_1 state, when the output of the comparator is high ($V_4 = V_u$) and the output of op-amp A_1 is positive, the capacitor C_2 is charged through R_t with the polarity opposite to that shown in Fig. 3(a). The output of A_1 thus decreases linearly, as shown in Fig. 4. This operation continues until the output of A_1 is zero and D_2 is switched off. The initial voltage of C_2 is V_d. The duration T_1 is then given by

$$T_1 = C_2 R_t V_d / V_u. \tag{4}$$

The diode D_1 is now forward-biased and the operation is switched to the T_2 state. The integrator on this state charges C_1 with the polarity shown in Fig. 3(b). This decreases the output of A_1 until it reaches $-V_u$, the threshold voltage of the comparator. T_2 is thus given by

$$T_2 = C_1 R_t. \tag{5}$$

T_2 is independent of the voltage, because the integrator is driven by the threshold voltage of the comparator.

When the output of A_1 reaches the threshold voltage, the output of the comparator changes to $-V_d$, and the operation is switched to the T_3 state. In this state, the integrator charges C_1 with the polarity shown in Fig. 3(c). This operation continues until the output of A_1 is zero and D_1 is switched off. T_3 is then given by

$$T_3 = C_1 R_t V_u / V_d. \tag{6}$$

When V_1 reaches zero, D_2 is now forward-biased, and the operation is switched to the T_4 state. The integrator in this state charges C_2 with the polarity shown in Fig. 3(d). This increases the output of A_1 until it reaches V_d, the threshold voltage of the comparator. T_4 is given by

$$T_4 = C_2 R_t. \tag{7}$$

T_4 is also independent of the voltage.

The comparator A_4 performs the triangular-to-rectangular waveform conversion, to produce the output of the interface. The high-level duration T_H and the low-level duration of the output pulse are given by

$$T_H = T_1 + T_4 = C_2 R_t (V_d + V_u)/V_u \tag{8}$$

$$T_L = T_2 + T_3 = C_1 R_t (V_d + V_u)/V_d. \tag{9}$$

The duty ratio D is thus

$$D \equiv \frac{T_H}{T_L + T_H} = \frac{C_2}{C_1 + C_2}(1 + \varepsilon_V) \tag{10}$$

where

$$\varepsilon_V = \frac{C_1\left(1 - \dfrac{V_u}{V_d}\right)}{C_1 \dfrac{V_u}{V_d} + C_2}. \tag{11}$$

If $V_u = V_d$, then ε_V is zero and the duty ratio corresponds exactly to the capacitance ratio. The duty ratio can be measured easily by means of gating a high-frequency clock. The measurement is accomplished in one cycle of the output pulse. Therefore, the interface shown in Fig. 2 allows the high-speed signal processing of a differential capacitance transducer. The analog equivalent of the capacitance ratio can also be obtained, if desired, by low-pass filtering the output pulse.

IV. Accuracy

Error sources involved in the interface are the voltage unbalance V_u/V_d, mismatch between R_1 and R_2, bias current I_B of op-amp A_1, and offset voltages V_{off} of op-amps and comparators. To eliminate the voltage unbalance effect, the interface is modified as shown in Fig. 5. The modification is based on the fact that T_2 and T_4 given by (5) and (7), respectively, do not depend on the voltage. This configuration has another advantage that nonideal performances of diode switches have no effect on the accuracy, either.

Waveforms observed in the improved interface are depicted in Fig. 6. In the figure, T_5 is defined as the period during which the comparators A_3 and A_4 both assume the high level, while T_6 as the period during which A_3 and A_4 both assume the low level. During T_5, the integrator A_1 keeps charging C_1 by the current $\{(V_u - V_{\text{off1}})/R_t - I_B\}$ and V_3 slews from $(\alpha V_u - V_{\text{off4}})$ up to $(V_u - V_{\text{off3}})$. T_5 is thus given by

$$T_5 = \frac{C_1 R_1 R_t}{R_3} \cdot \frac{(1-\alpha)V_u - V_{\text{off3}} + V_{\text{off4}}}{V_u - V_{\text{off1}} - R_t I_B}. \tag{12}$$

During T_6, on the other hand, the integrator A_1 keeps drawing the current $\{(V_d + V_{\text{off1}})/R_t + I_B\}$ from C_2 and V_3 slews from $(-\alpha V_d - V_{\text{off4}})$ down to $(-V_d - V_{\text{off3}})$. T_6 is thus given by

$$T_6 = \frac{C_2 R_2 R_t}{R_3} \cdot \frac{(1-\alpha)V_d - V_{\text{off3}} + V_{\text{off4}}}{V_d - V_{\text{off1}} - R_t I_B}. \tag{13}$$

From (12) and (13), one can obtain the first order expression of the capacitance ratio

$$\frac{T_5}{T_5 + T_6} = \frac{C_1}{C_1 + C_2}(1 + \varepsilon) \tag{14}$$

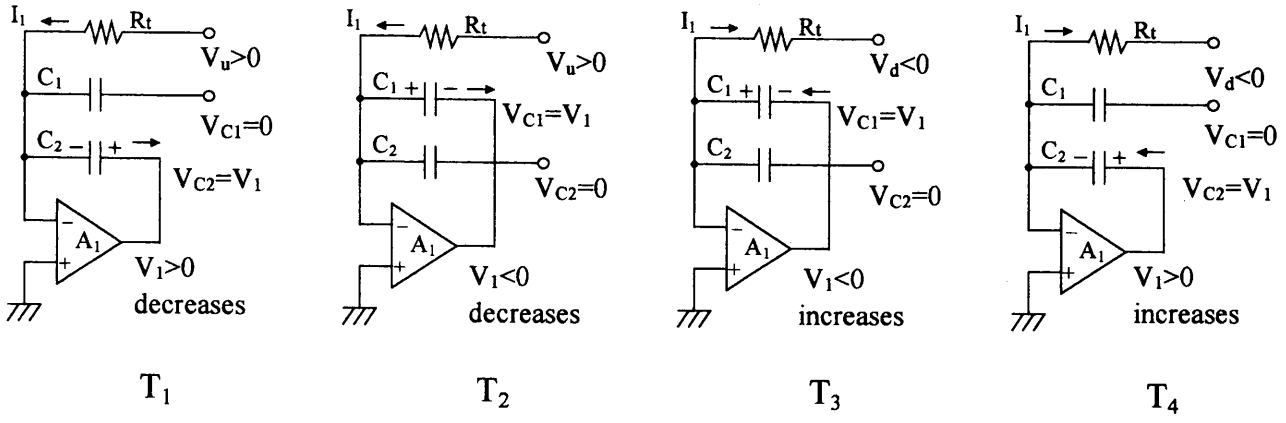

Fig. 3. The integrator in each state.

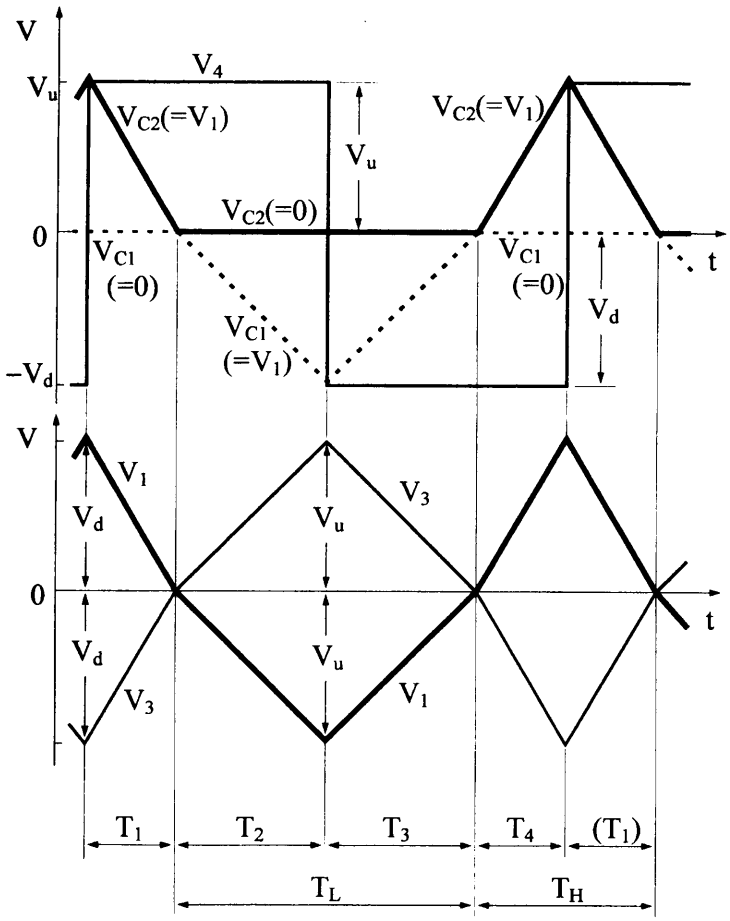

Fig. 4. Waveforms, observed in the interface.

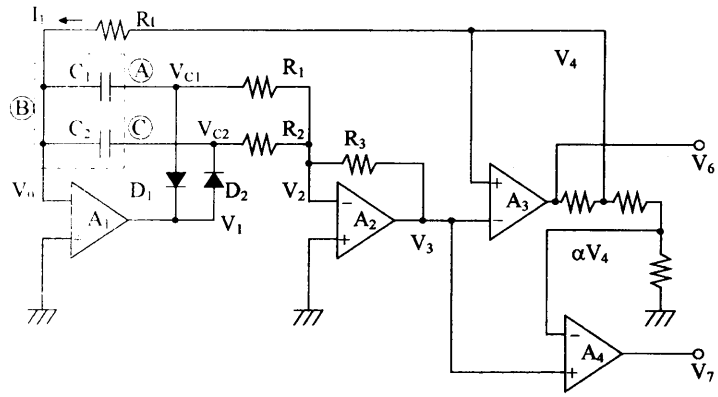

Fig. 5. An improved circuit.

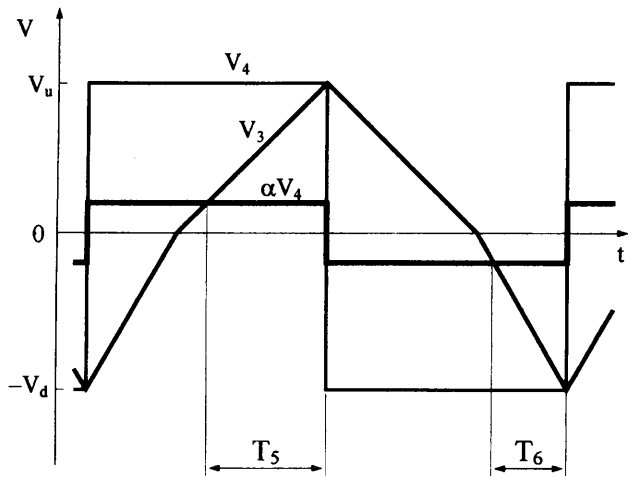

Fig. 6. Waveforms observed in the improved interface.

where

$$\varepsilon = \frac{C_2}{C_1 + C_2}\varepsilon_R + \frac{2C_2}{C_1 + C_2} \cdot \left\{ \frac{R_t I_B}{V_u} + \frac{V_{\text{off}1}}{V_u} - \frac{V_{\text{off}3} - V_{\text{off}4}}{(1-\alpha)V_u} \right\} \quad (15)$$

$$\varepsilon_R = \frac{R_1 - R_2}{R_1}. \quad (16)$$

The first term represents the error due to the resistance mismatch and the second term due to the offset voltages. The error due to each source is evaluated for x ranging from -0.5 to 0.5 using following typical values; $V_d = V_u = 10$ V, $R_1 \cong R_2 \cong R_3 = 1$ kΩ, $R_t = 125$ MΩ, $C_0 = C_1 + C_2 = 2$ pF, $\alpha = 0.1$. The results are listed in Table I, indicating that a resolution higher than 0.1% can be expected from this simple interface.

V. Prototype Interface

A prototype interface based on Fig. 2 was breadboarded using off-the-shelf op-amps (LF411). To evaluate its performance, a ganged parallel plate capacitor was used as a

TABLE I
ESTIMATED ERRORS

Error source	ε_{max}
$\varepsilon_R = 1 \times 10^{-3}$	0.75×10^{-3}
$I_B = 15$ pA	0.28×10^{-3}
$V_{off} = 0.3$ mV	0.15×10^{-3}

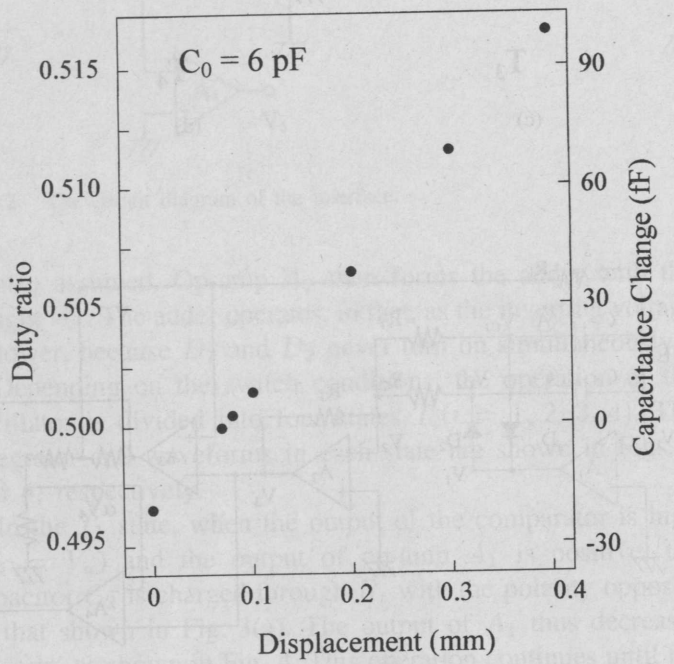

Fig. 7. Experimentally measured capacitance change and duty ratio.

transducer [8]. The 30 MHz clock was used for the duty ratio measurement.

The capacitances C_1 and C_2 are given by (2) with x being the displacement of the inner electrode from the center of two outer electrodes. The total capacitance C_0 is 3 pF or 6 pF.

Fig. 7 shows typical measurement results when $C_0 = 6$ pF. The oscillation frequency when $C_1 = C_2$ is adjusted to be 0.5 kHz by means of R_t. Dots plotted in the figure are averaged values of 20 measurements at each displacement. The displacement is adjusted by a micrometer screw with the finest scale of 10 μm.

To evaluate the resolution, measurements are repeated with C_0 being 3 pF. The standard deviation in the capacitance evaluated from the duty ratio measurements is 60 aF, which corresponds to $2 \times 10^{-3}\%$ resolution. These results confirm the accuracy estimate in the previous section.

VI. CONCLUSIONS

An interface circuitry was presented for ratiometric signal processing of a differential capacitance transducer. Circuit analyzes have shown that a resolution higher than 0.1% is easily achievable with this simple configuration. The prototype interface built using off-the-shelf components has confirmed the circuit analyzes and demonstrated the validity in practical applications.

The ratiometric signal processing is performed in the time-domain by measuring the duty ratio of the output signal. Therefore, the interface proposed here allows high-speed measurements. The sampling speed higher than 5 ksps (samples/s) can be expected from using high-speed comparators. A one-chip implementation and applications to practical transducers are future works.

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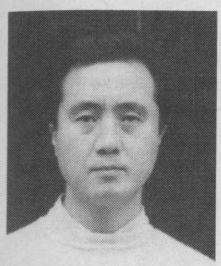

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