A Switched-Capacitor Interface for Differential Capacitance Transducers

Satomi Ogawa, *Member, IEEE*, Yutaka Oisugi, Kouji Mochizuki, *Member, IEEE*, and Kenzo Watanabe, *Fellow, IEEE*

***Abstract*—For high-accuracy signal processing of differential capacitance transducers, an interface circuitry based on a switched-capacitor (SC) sample/hold (S/H) circuit is developed. Driven by nonoverlapping two-phase clocks, the interface produces the output voltage which is proportional to the ratio of difference-to-sum of two capacitors of a differential transducer. Performances of a prototype chip fabricated using 0.6-μm n-well CMOS process were measured and compared with those simulated by HSPICE. The measured results indicate that 0.1% resolution is achievable with the proposed interface and the temperature-dependence of the interface is small. An interface circuit improved for smaller temperature-dependence is also proposed and its operation is confirmed experimentally.**

***Index Terms*—CMOS integrated circuit, differential capacitance transducer, ratiometric signal processing, sample and hold, switched-capacitor circuit.**

I. Introduction

A DIFFERENTIAL capacitance transducer consisting of two capacitors is widely used to detect such physical quantities as pressure difference, linear displacement, acceleration, and rotational angle [1]. Its electrical equivalent is shown in Fig. 1, where C_a and C_b are two capacitors which change complementarily with a measurand. In a rotational angle encoder, C_a and C_b change linearly with the angle x

$$C_{a,b} = \frac{C_o}{2}(1 \pm x) \tag{1}$$

where $C_o = C_a + C_b$ is the total capacitance. In pressure transducers, on the other hand, C_a and C_b change hyperbolically with applied pressure x [2]

$$C_{a,b} = \frac{C_o}{2}\frac{1}{1 \pm x}. \tag{2}$$

In either case, the measurand x can be extracted independently of the total capacitance by the following ratiometric operation:

$$x = \frac{C_a - C_b}{C_a + C_b}. \tag{3}$$

Besides the linear extraction of a measurand x, the ratiometric operation has another distinct feature that capacitance changes due to temperature which would otherwise be a major error source are cancelled and have no effect on the accuracy if signal processing is insensitive to parasitic capacitances C_{pa}, C_{pb}, and $C_{\rm pc}$.

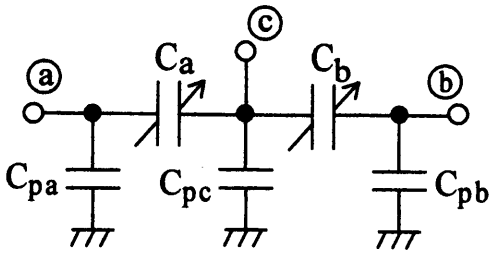

Fig. 1. Equivalent circuit of a differential capacitance transducer.

Several methods have so far been proposed for the ratiometric operation. The most conventional method is based on detection of currents flowing through C_a and C_b. The ratiometric operation is then performed by controlling the amplitude of the excitation such that the total current through C_a and C_b is constant [3]–[6]. The ratiometric operation can also be performed by an analog-to-digital converter (ADC) with the reference being an electrical variable proportional to $C_a + C_b$. Such methods using a charge-balancing [7], oversampling $\Delta\Sigma$ modulating [8], [9], or successive-approximation [10] ADC provide the digital equivalent of a measurand. The other methods use the relaxation oscillator consisting of an integrator and a comparator, providing a measurand in the digital [11] or duty ratio [12] form.

Ratiometric signal processing based on the ADC or relaxation oscillation is suited for cointegration with micromachined transducers, but is limited to low-speed applications. The current detection method has therefore been used exclusively for high-speed ratiometric signal processing. The signal processing is easy, but requires a sinusoidal excitation with the large amplitude to obviate the temperature-dependent voltage drop of a diode detector. To alleviate this problem, a relaxation oscillator including the charge amplifier has recently been proposed.[13]. This modified oscillator allows a signal processing speed up to 10^5 sample/s (samples/s), but requires component matching.

A CMOS interface for high-speed ratiometric operation is required by micromachined differential capacitance transducers for acceleration and rotary angle measurements. To respond to the request, an interface is developed based on a switched-capacitor (SC) sample/hold (S/H) circuit. This paper describes its configuration, accuracy estimates, and simulated and measured performances of a prototype chip integrated by a 0.6-μm n-well CMOS process. An improved circuit is finally given to reduce the temperature dependence.

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S. Ogawa and K. Watanabe are with the Research Institute of Electronics, Shizuoka University, Hamamatsu, Japan.

Y. Oisugi is with Chiba Precision Corporation, Funabashi, Japan,

K. Mochizuki is with the Electrical Engineering Department, Numazu College of Technology, Numazu, Japan,

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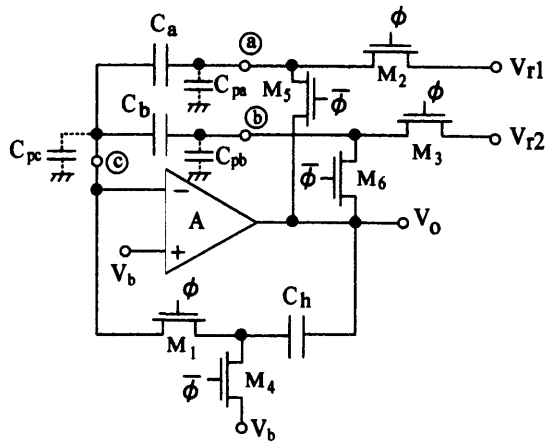


Fig. 2. (a) Circuit diagram of the interface. (b) Timing diagram of the nonoverlapping two-phase clocks.

II. Interface

Fig. 2 shows the interface circuit for ratiometric signal processing of differential capacitance transducers. It is basically the SC S/H circuit with two transducer capacitances C_a and C_b being S/H capacitors. Capacitor C_h is an additional hold capacitor to mitigate the slew rate requirement of op-amp A [14]. If the op-amp is ideal, C_a is charged to $(V_{r1} - V_b)$ and C_b to $(V_{r2} - V_b)$ in the ϕ phase. In the $\bar{\phi}$ phase, two capacitors are connected in parallel, to produce the output voltage $V_o(\bar{\phi})$

$$V_o(\bar{\phi}) = V_b + \frac{C_a(V_{r1} - V_b) + C_b(V_{r2} - V_b)}{C_a + C_b} = \frac{C_a V_{r1} + C_b V_{r2}}{C_a + C_b} \tag{4}$$

where V_b is the bias voltage applied to the noninverting input terminal of an op-amp for the single-supply operation. If V_{r1} and V_{r2} are set to

$$V_{r1} = \frac{V_{\mathrm{DD}}}{2} + V_r, \tag{5}$$

and

$$V_{r2} = \frac{V_{\mathrm{DD}}}{2} - V_r \tag{6}$$

then $V_o(\bar{\phi})$ is given by

$$V_o(\bar{\phi}) = \frac{V_{\mathrm{DD}}}{2} + xV_r. \tag{7}$$

Parasitic capacitances have no effect on the ratiometric operation because C_{pa} and C_{pb} are connected to voltage sources and C_{pc} is kept charged to V_b. This also holds true for the hold capacitor C_h because it merely provides the feedback path in the ϕ phase.

Error sources involved in the interface are the finite gain and the offset voltage of an op-amp and the charge injection from switches. Let the frequency-dependent gain of an op-amp be $A(s)$. The output voltages $V_o(\phi_n)$ and $V_o(\overline{\phi_n})$ in the ϕ and $\bar{\phi}$ phases at the time n, respectively, are then given by (8) and (9), shown at the bottom of the page, where C_{pc} is the parasitic capacitance at the common electrode of a transducer. If $C_h \gg C_a + C_b$, then $V_o(\phi_n)$ in (8) can be approximated by

$$V_o(\phi_n) = V_o(\bar{\phi}_{n-1}) = \frac{C_a - C_b}{C_a + C_b} V_r + \frac{V_{\mathrm{DD}}}{2}. \tag{10}$$

Substituting (10) into (9), we have

$$V_o(\bar{\phi}) = \frac{V_{\mathrm{DD}}}{2} + XV_r. \tag{11}$$

Equation (11) indicates that the error voltage due to the finite gain which is stored into C_a and C_b in the ϕ phase compensates the corresponding output error in the $\bar{\phi}$ phase, thereby making the ratiometric operation insensitive to the finite gain. The offset voltage of the op-amp in the $\bar{\phi}$ phase is also compensated by that stored into C_a and C_b in the ϕ phase. Therefore, no special design strategy is required for the op-amp.

The error factor that limits the operational accuracy is therefore charge injection from switches M_1, M_2,, and M_3. The error voltage $\delta V_o(\bar{\phi})$ due to charge injection is given by

$$\delta V_o(\bar{\phi}) = \frac{Q_{f,\mathrm{total}}}{C_a + C_b} \tag{12}$$

where

$$Q_{f,\mathrm{total}} = Q_{f1} + Q_{f2} + Q_{f3} \tag{13}$$

and Q_{fi} is the charge injected to C_a and C_b from switch $M_i (i = 1, 2, 3)$. The injected charge consists of the channel charge q_{CH} and the clock-feedthrough component q_{CL}

$$Q_f = q_{\mathrm{CH}} = q_{\mathrm{CL}} \tag{14}$$

where

$$q_{\mathrm{CH}} = C_{\mathrm{CH}}(V_G - V_r)/2 \tag{15}$$

$$q_{\mathrm{CL}} = C_{\mathrm{OL}} V_G \tag{16}$$

$$V_o(\phi_n) = V_o(\bar{\phi}_{n-1}) + \frac{1}{C_h} \cdot \frac{(C_a + C_b)V_o(\bar{\phi}_{n-1}) - (C_a - C_b)\left(V_r + \frac{V_{\mathrm{DD}}}{2}\right)}{1 + \frac{C_h + C_a + C_b + C_{\mathrm{pc}}}{C_h} \cdot \frac{1}{A(s)}} \tag{8}$$

$$V_o(\bar{\phi}_n) = \frac{(C_a - C_b)V_r + (C_a + C_b)\frac{V_{\mathrm{DD}}}{2} + (C_a + C_b + C_{\mathrm{pc}})V_o(\phi_n)/A(s)}{(C_a + C_b)\left(1 + \frac{C_h + C_a + C_b + C_{\mathrm{pc}}}{C_h} \cdot \frac{1}{A(S)}\right)} \tag{9}$$

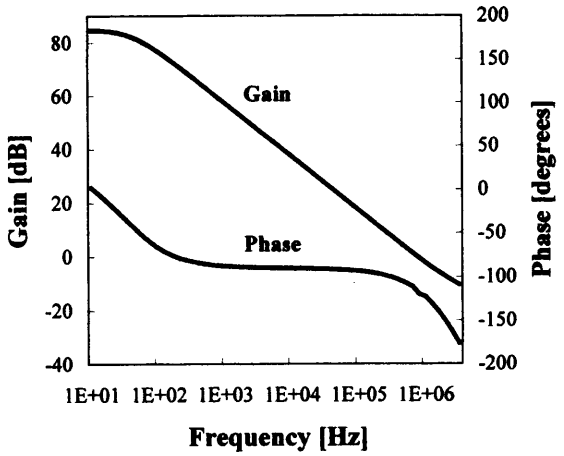


Fig. 3. Op-amp performances.

and C_{CH}, C_{OL}, and V_T are the channel capacitance, the overlap capacitance, and the threshold voltage of the MOS switch, respectively, and V_G is the gate voltage. Substituting (14) into (12) and noting that q_{CH} is independent of C_a and C_b and that q_{CL} is shared between C_{OL} and C_a (or C_b), we have, to the first order

$$\delta V_o(\bar{\phi}) = \frac{q_{\mathrm{CH,total}} + q_{\mathrm{CL,total}}}{C_o} - \frac{2C_{\mathrm{OL}}}{C_o^2(1-x^2)} \cdot q_{\mathrm{CL,total}}. \quad (17)$$

The first term in (17) represents the offset error which can be nullified by the offset adjustment. The second term is the nonlinear error that limits the ultimate accuracy. Specifically, $q_{\mathrm{CL,total}}$ is of the order of 1 pC and C_{OL} is typically 20 fF. Assuming $C_0 = 10$ pF, then the nonlinear error amounts to 2 mV. Reducing the clock-feedthrough component by the use of small-dimensioned switches with the dummy compensation is crucial for high-accuracy signal processing. Reducing the gate aspect ratio, however, increases the on-resistance of a switch and thereby decreases the operational speed. Therefore, the switch should be designed based on the compromise between the accuracy and the speed.

III. Performance Simulated by HSPICE

Performances expected from CMOS realization are simulated by HSPICE with 0.6-μm CMOS process parameters. A simple two-stage CMOS op-amp consisting of a differential pair followed by a rail-to-rail output stage is designed for low voltage and low power operation. Fig. 3 shows performances of the op-amp. The dc gain is typically 84 dB and the dominant pole is located at 30 Hz. Performances of the interface using this op-amp and switches with the aspect ratio $W/L_{\mathrm{PMOS}} = 13.0\,\mu\mathrm{m}/0.9\,\mu\mathrm{m}$, $W/L_{\mathrm{NMOS}} = 4.0\,\mu\mathrm{m}/0.9\,\mu\mathrm{m}$ are compared with those using an ideal op-amp and switches with the same aspect ratio in Fig. 4. These performances are quite similar. This confirms the theoretical analysis described in the previous section that the ratiometric operation is insensitive to nonideal performances of an op-amp. Error voltages for different switch dimensions are compared in Fig. 5. The comparison demonstrates that the charge injection is dependent on temperature, and reducing the charge injection is critical to high-accuracy processing.

Fig. 6 shows the on-resistance of the switch as a function of the input voltage. The on-resistance of the switch is 1.5 kΩ at maximum. Assuming $C_o = 10$ pF, the 0.1% settling time is

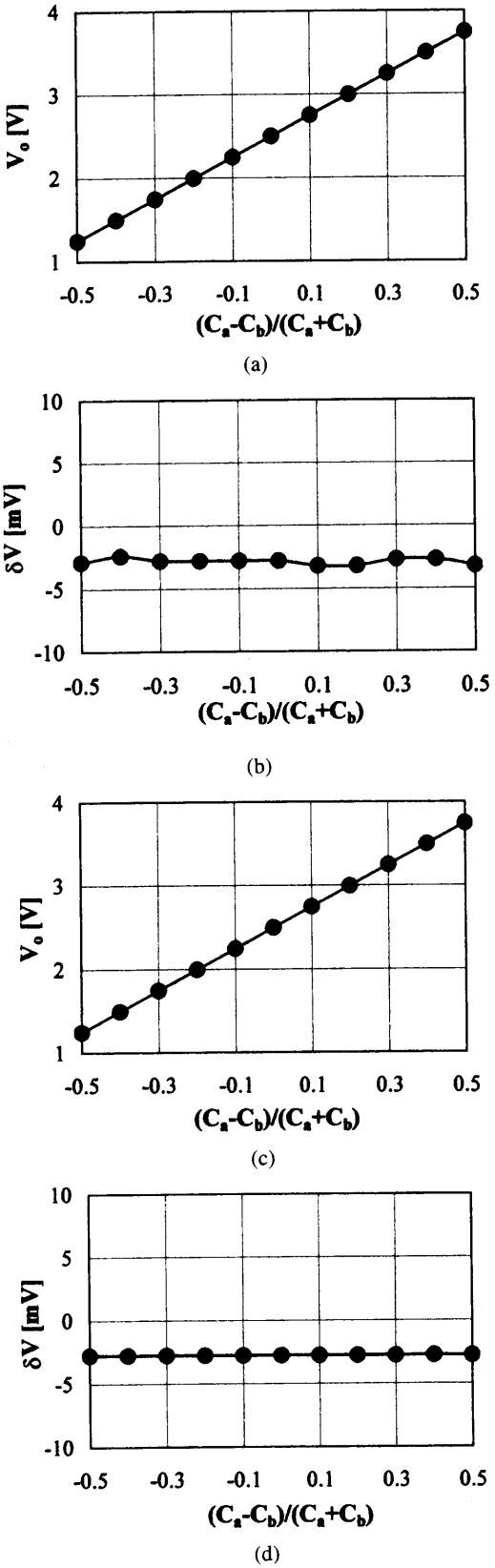
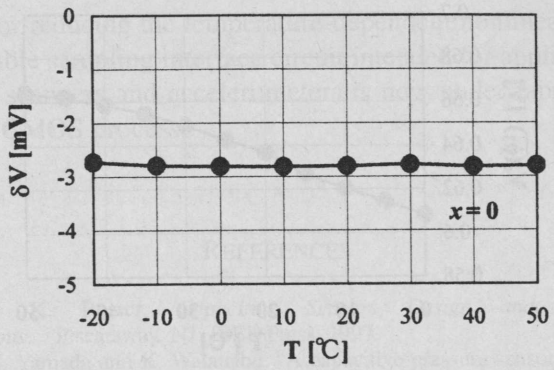
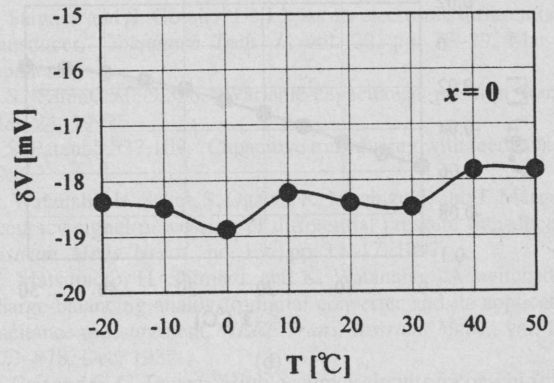


Fig. 4. Simulated performances of a prototype chip. The aspect ratios of switches are $W/L_{\mathrm{PMOS}} = 13.0\,\mu\mathrm{m}/0.9\,\mu\mathrm{m}$, $W/L_{\mathrm{NMOS}} = 4.0\,\mu\mathrm{m}/0.9\,\mu\mathrm{m}$. (a) Output voltage and (b) the deviation from the ideal value as a function of capacitance difference-to-sum ratio, assuming the two-stage op-amp. (c) Output voltage and (d) the deviation from the ideal value as a function of capacitance difference-to-sum ratio, assuming an ideal op-amp.

104 ns. This implies that the clock signal as high as 4.8 MHz is allowed to drive switches. Inferring from the op-amp performances, however, the clock frequency will be limited to 1 MHz in practice. Much higher sampling rate is possible by increasing the power consumption of the op-amp.



(a)



(b)

Fig. 5. Error voltage as a function of temperature. (a) Switch aspect ratio: $W/L_{\mathrm{PMOS}} = 13.0\ \mu\mathrm{m}/0.9\ \mu\mathrm{m}$, $W/L_{\mathrm{NMOS}} = 4.0\ \mu\mathrm{m}/0.9\ \mu\mathrm{m}$. (b) Switch aspect ratio: $W/L_{\mathrm{PMOS}} = 65.0\ \mu\mathrm{m}/1.2\ \mu\mathrm{m}$, $W/L_{\mathrm{NMOS}} = 20.0\ \mu\mathrm{m}/1.2\ \mu\mathrm{m}$.

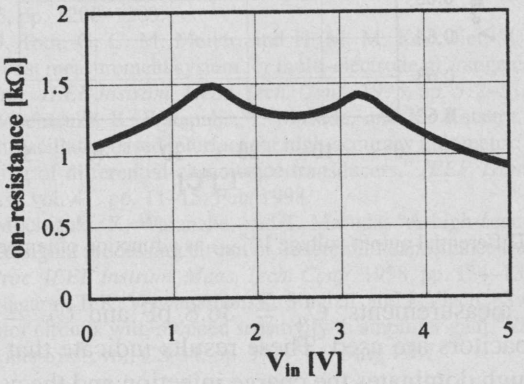


Fig. 6. On-resistance of the switch.

IV. Performances of Prototype Interfaces

The interface of Fig. 2 was integrated using the 0.6-μm n-well CMOS process. The op-amp described in the previous section and CMOS switches with the aspect ratio $W/L_{\mathrm{PMOS}} = 13.0\ \mu\mathrm{m}/0.9\ \mu\mathrm{m}$, $W/L_{\mathrm{NMOS}} = 4.0\ \mu\mathrm{m}/0.9\ \mu\mathrm{m}$ are used for implementation of the interface. Fig. 7 shows a microphotograph of the prototype chip. In addition to the interface circuit shown in Fig. 2, the chip includes a conventional op-amp-based S/H circuit and the two-phase clock generator. The quiescent current of the op-amp and the clock frequency can be adjusted by means of external resistors. To evaluate performance of the chip, pairs of mica capacitors with the total capacitor C_o being 50 pF were used in place of a transducer. The power supply voltage V_{DD} is 5 V. The clock frequency is

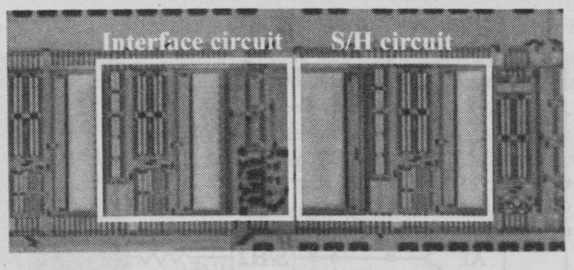
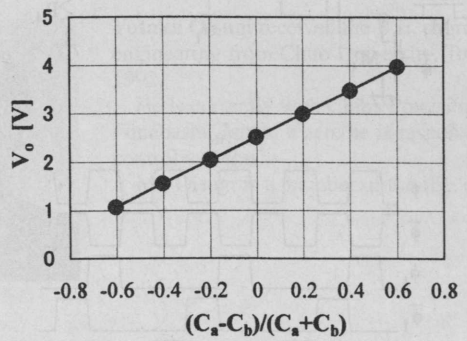
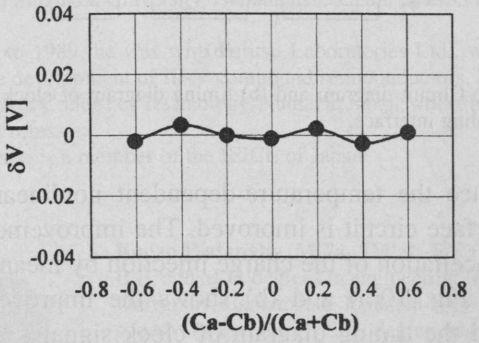


Fig. 7. Microphotograph of the prototype chip.



(a)



(b)

Fig. 8. Measured performances of a prototype chip. (a) Output voltage and (b) the deviation from the ideal value as a function of capacitance difference-to-sum ratio.

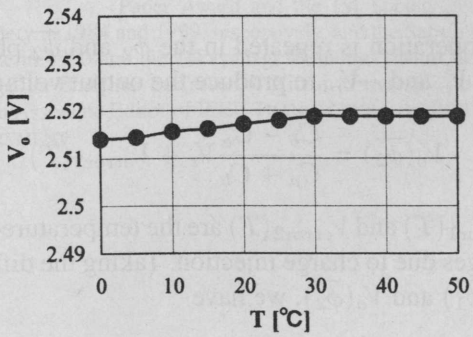


Fig. 9. Output voltage as a function of temperature of the prototype chip.

set to 100 kHz. The reference voltages V_{r1} and V_{r2} are 5 V and 0 V, respectively. Typical measurement results are shown in Fig. 8. The output voltage plotted in Fig. 8(a) is proportional to the difference-to-sum ratio of two capacitors, confirming the ratiometric operation given by (7). The nonlinear error, plotted in Fig. 8(b), is of the order of a few millivolts. These results indicate that 0.1% resolution is achievable with the proposed interface. Fig. 9 shows the output voltage as a function of temperature when $x = 0$. This result shows that the temperature variation is smaller than $2 \times 10^{-3}\%/^{\circ}\mathrm{C}$.

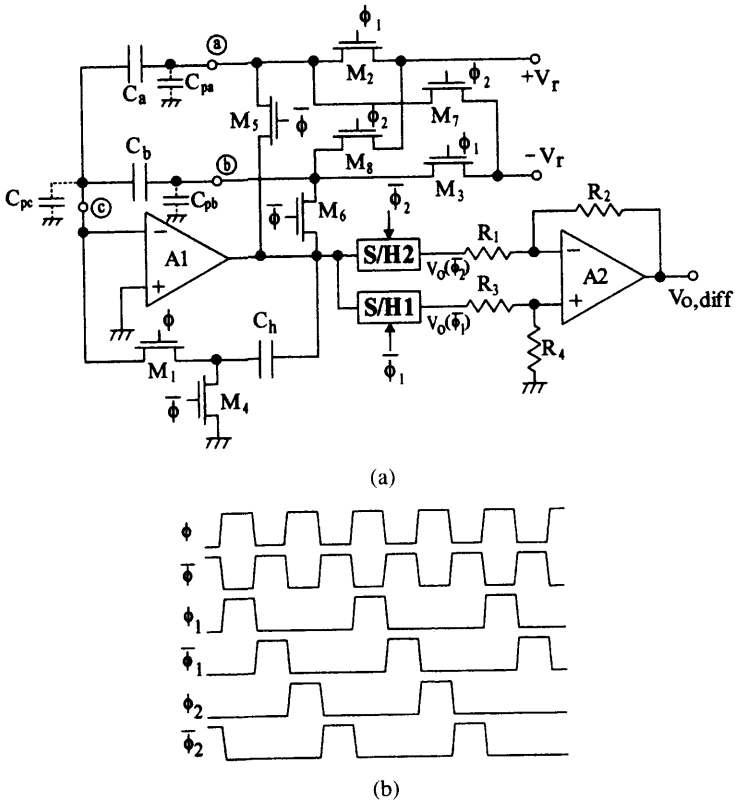


Fig. 10. (a) Circuit diagram and (b) timing diagram of clock signals of the double sampling interface.

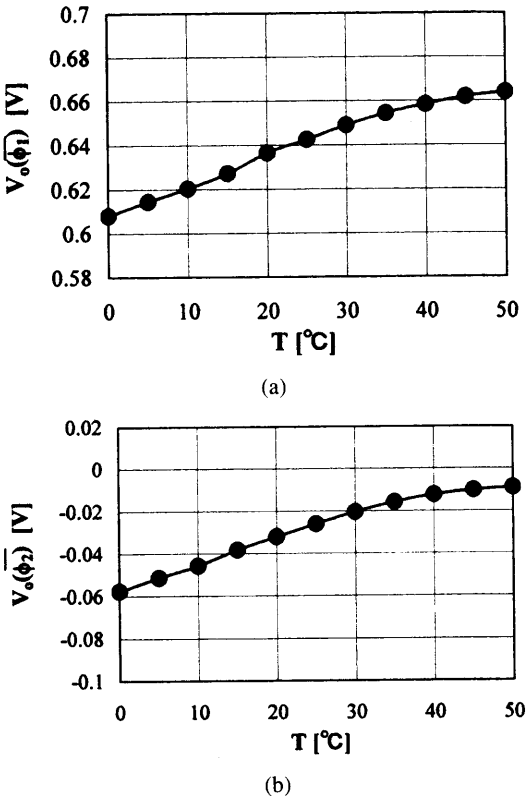


Fig. 11. Output voltage of the double sampling interface in the $\overline{\phi_1}$ phase (a) and $\overline{\phi_2}$ phase (b) as a function of temperature.

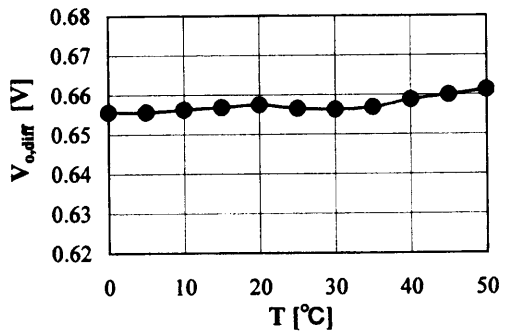


Fig. 12. Differential output voltage $V_{o,\mathrm{diff}}$ as a function of temperature.

To reduce the temperature-dependent nonlinear error, the basic interface circuit is improved. The improvement is based on the cancellation of the charge injection by means of double sampling. Fig. 10(a) and (b) shows the improved interface circuit and the timing diagram of clock signals, respectively. The operation in the ϕ_1 and $\overline{\phi_1}$ phases is the same as that of the basic circuit, producing the output voltage $V_o(\overline{\phi_1})$

$$V_o(\overline{\phi_1}) = \frac{C_a - C_b}{C_a + C_b} V_r + V_{\mathrm{error1}}(T). \tag{18}$$

The same operation is repeated in the ϕ_2 and $\overline{\phi_2}$ phases while alternating V_r and $-V_r$, to produce the output voltage $V_o(\overline{\phi_2})$:

$$V_o(\overline{\phi_2}) = \frac{C_b - C_a}{C_a + C_b} V_r + V_{\mathrm{error2}}(T) \tag{19}$$

where $V_{\mathrm{error1}}(T)$ and $V_{\mathrm{error2}}(T)$ are the temperature-dependent error voltages due to charge injection. Taking the difference between $V_o(\overline{\phi_1})$ and $V_o(\overline{\phi_2})$, we have

$$\begin{aligned} V_{o,\mathrm{diff}} &= V_o(\overline{\phi_1}) - V_o(\overline{\phi_2}) \\ &= 2\frac{C_a - C_b}{C_a + C_b} V_r + V_{\mathrm{error1}}(T) - V_{\mathrm{error1}}(T). \end{aligned} \tag{20}$$

If $V_{\mathrm{error1}}(T) \approx V_{\mathrm{error2}}(T)$, then we have

$$V_{o,\mathrm{diff}} \approx 2\frac{C_a - C_b}{C_a + C_b} V_r. \tag{21}$$

To confirm the circuit operation, the improved circuit was breadboarded using OPA627 op-amps, MAX317 switches, and LF398 S/H circuits. The clock frequency is 100 kHz. Fig. 11(a) and (b) shows the output voltages of the S/H1 and S/H2 circuits as a function of temperature, respectively. In these measurements, $C_a = 36.8$ pF and $C_b = 32.1$ pF mica capacitors are used. These results indicate that the clock feedthrough dominates the charge injection and the assumption $V_{\mathrm{error1}}(T) \approx V_{\mathrm{error2}}(T)$ holds true. Fig. 12 shows the differential output voltage $V_{o,\mathrm{diff}}$ as a function of temperature. The change in the differential output voltage due to temperature is smaller than one tenth that in the basic circuit. Therefore, one can conclude reasonably that a resolution ten times higher than that of the basic circuit is possible with the improved circuit.

V. Conclusion

A CMOS interface circuit of differential capacitance transducers has been described which performs the ratiometric operation with the simple configuration. Simulated and measured performances of the prototype chip integrated by the 0.6-μm n-well CMOS process have demonstrated that 0.1% resolution is achievable, and the higher accuracy will be obtained by using the dummy-compensated switches with small gate areas. A prototype interface has also proved that cancellation of clock-feedthrough charges by double sampling is quite

useful for reducing the temperature-dependent nonlinear error. The double sampling interface circuit intended for applications to laser scanners and accelerometers is now under fabrication using a CMOS process.

REFERENCES

[1] L. K. Baxter, *Capacitive Sensors Design and Applications*. Piscataway, NJ: IEEE Press, 1997.

[2] M. Yamada and K. Watanabe, "A capacitive pressure sensor interface using oversampling $\Delta - \Sigma$ demodulation techniques," *IEEE Trans. Instrum. Meas.*, vol. 46, pp. 3–7, Feb. 1997.

[3] T. Saigusa and S. Gotoh, "UNIΔ series electronic differential pressure transducer," *Yokogawa Tech. J.*, vol. 22, pp. 23–29, Mar. 1978. in Japanese.

[4] U.S. Patent 5,099,386, "Variable-capacitance position transducing," Mar. 24, 1992.

[5] U.S. Patent 5,537,109, "Capacitive transducing with feedback," July 16, 1996.

[6] K. Watanabe, H. Sakai, S. Ogawa, K. Mochizuki, and T. Masuda, "High-accuracy signal processing of differential pressure transducers," *IEEE Instrum. Meas. Newsl.*, no. 135, pp. 11–17, 1997.

[7] H. Matsumoto, H. Shimizu, and K. Watanabe, "A switched-capacitor charge-balancing analog-to-digital converter and its application to capacitance measurement," *IEEE Trans. Instrum. Meas.*, vol. IM-36, pp. 873–878, Dec. 1987.

[8] Y. Cao and G. C. Temes, "High-accuracy circuits for on-chip capacitance ratio testing or sensor readout," *IEEE Trans. Circuits Syst.*, vol. 41, pp. 637–639, Sept. 1994.

[9] B. Wang, T. Kajita, T. Sun, and G. Temes, "High-accuracy circuits for on-chip capacitive ratio testing and sensor readout," *IEEE Trans. Instrum. Meas.*, vol. 47, pp. 16–20, Feb. 1998.

[10] K. Mochizuki, T. Masuda, and K. Watanabe, "An interface circuit for high-accuracy signal processing of differential-capacitance transducers," in *Proc. IEEE Instrum. Meas. Tech. Conf.*, Brussels, Belgium, 1996, pp. 1200–1203.

[11] T. N. Toth, G. C. M. Meijer, and H. M. M. Kerkvliet, "Ultra-linear, low-cost measurement system for multi-electrode pF-range capacitors," in *Proc. IEEE Instrum. Meas. Tech. Conf.*, 1995, pp. 512–515.

[12] K. Mochizuki, K. Watanabe, T. Masuda, and M. Katsura, "A relaxation-oscillator-based interface for high-accuracy ratiometric signal processing of differential-capacitance transducers," *IEEE Trans. Instrum. Meas.*, vol. 47, pp. 11–15, Feb. 1998.

[13] K. Mochizuki, K. Watanabe, and T. Masuda, "A high-accuracy, high-speed signal processing circuit of differential-capacitance transducers," in *Proc. IEEE Instrum. Meas. Tech. Conf.*, 1998, pp. 134–137.

[14] K. Nagaraj, T. R. Viswanathan, K. Singhal, and J. Vlach, "Switched-capacitor circuits with reduced sensitivity to amplifier gain," *IEEE Trans. Circuits Syst.*, vol. CS-34, pp. 571–574, May 1987.

Satomi Ogawa (S'90–M'93) received the B.E. and M.E. degrees in engineering and the Dr.Eng. degree from Shizuoka University, Hamamatsu, Japan, in 1988, 1990, and 1993, respectively.

She is currently a Research Associate at the Research Institute of Electronics, Shizuoka University. Her research interests are CMOS analog integrated circuits and sensor signal processing.

Yutaka Oisugi received the B.E. degree in electrical engineering from Chuo University, Tokyo, Japan, in 1992.

He is currently with Chiba Precision Corporation, Funabashi, Japan, where he is responsible for motor control systems.

Mr. Oisugi is a member of the IEE of Japan.

Kouji Mochizuki (M'98) received the B.E. and M.E. degrees in electronic engineering from Shizukoa University, Hamamatsu, Japan, in 1983 and 1985, respectively.

From 1985 to 1989, he was with Fujitsu Laboratories Ltd., where he was engaged in the development of III-V compound semiconductors. In July 1989, he joined Numazu College of Technology, Numazu, Japan, where he is currently an Associate Professor.

Mr. Mochizuki is a member of the IEICE of Japan.

Kenzo Watanabe (M'74–SM'86–F'93) received the B.E. and M.E. degrees in engineering from Shizuoka University, Hamamatsu, Japan, in 1962 and 1966, respectively, and the Dr.Eng. degree from Kyoto University, Kyoto, Japan, in 1976.

From 1982 to 1983, he was a Visiting Professor at the University of California, Los Angeles. Currently, he is a Professor at the Research Institute of Electronics, Shizuoka University.

Dr. Watanabe received the Andrew R. Chi Best Paper Award and the IM Society Award from the IEEE IM Society in 1984 and 1999, respectively, and the Satio Award from the Chion Institute in 1990 and the Takayanagi Memorial Award in 1994. He was also designated an Emeritus Professor of Xidian University, Xi'an, China, in 1997. He is an Associate Editor of IEEE TRANSACTIONS ON INSTRUMENTATION AND MEASUREMENT.