Characterization of Current-Mode CMOS R-2R Ladder Digital-to-Analog Converters

Lei Wang, Yasunori Fukatsu, and Kenzo Watanabe, *Fellow, IEEE*

***Abstract*—A digital-to-analog (D/A) converter based on the R-2R ladder is first analyzed in terms of the power consumption, to point out that the current-mode is the lowest power dissipation counterpart of the voltage-mode. The integral nonlinearity (INL) analyses and the characterization methods of the current-mode D/A converter are then presented to identify the error sources. The methods are applied to an 8-bit D/A converter fabricated using 0.6 μm CMOS process. Measured results compared with INL analyses indicate that the dominant error source of a prototype converter is the resistance of the metal interconnect between the ladder and the bonding pad, and the INL of the ladder itself is 1.2 LSB.**

***Index Terms*—CMOS integrated circuit, current-mode, digital–analog conversion, low power, resistive ladder.**

I. Introduction

THE CMOS process is commonly used for mixed analog and digital system integration, because the advance in fine-line technology makes it possible to integrate a large system onto a small silicon area. One of the issues accompanying such a high-density integration is the power dissipation, and low-voltage and low-power designs are highly recommended [1], [2]. This is especially true for an analog circuit, and a promising candidate is a current-mode circuit that has the potential capabilities of wideband and wide dynamic signal processing under the low supply voltage. Current-mode analog-to-digital (A/D) and digital-to-analog (D/A) converters will, therefore, be key components in mixed analog and digital ASICs [3].

Any data converter, A/D, or D/A converter, requires the quantized reference. A straightforward way of producing the quantized references is the resistor string or tapped resistor. This architecture is exclusively used for high-speed flash A/D converters, but is seldom applied to a D/A converter because the switch tree to multiplex the quantized references depending on a digital input takes a long time to settle [4], [5]. Another simple architecture is the R-2R ladder. It operates as a high-speed current divider [6], and the small device count is quite attractive to an ASIC in which a large number of D/A converters are required [7], [8]. The main error sources of the R-2R ladder D/A converter are mismatches of the switch on-resistances, but the advances in CMOS fine-line technology have greatly improved the matching accuracy of switches. Based on these technological aspects, the R-2R ladder is revisited.

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This paper first reviews the R-2R ladder D/A converter to point out that the current-or inverse-mode configuration is best suited for low-power operation. Then, methods to characterize the current-mode converter are presented. Performances of an 8-bit D/A converter fabricated using the 0.6 μm CMOS process are finally presented to demonstrate the characterization methods.

II. R-2R Ladder D/A Converters

Fig. 1 shows a circuit diagram of a conventional voltage-mode R-2R ladder D/A converter. V_r is the reference voltage and $d_i (i = 1, 2, \ldots, n)$ is the n-bit binary number to be converted into the analog voltage. Assuming now that all resistors are exactly matched and the switches are ideal, then the impedance seen from the node ⓘ to the right is 2R and the reference voltage switched by d_i is attenuated by 2^{-i} to reach the node ①. The output V_{out} of the D/A converter is thus given by

$$V_{\text{out}} = \left(d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n}\right) \times V_r = \frac{D}{2^n} V_r \quad (1)$$

where

$$D = d_1 2^{n-1} + d_2 2^{n-2} + \cdots + d_n. \quad (2)$$

The current flowing through each leg is given by

$$I_1 = \frac{d_1 V_r - V_{\text{out}}}{2R}, \quad (3)$$

$$I_i = \frac{d_i V_r - \left[V_{\text{out}} - R\sum_{k=1}^{i-1} (i-k) I_k\right]}{2R} \quad (i = 2, 3, \ldots, n+1) \quad (4)$$

where $d_{n+1} = 0$.

If $d_i = 1$, the current I_i is supplied by the reference source. If $d_i = 0$, on the other hand, I_i sinks to the ground. Since no current flows out of the terminal ①, the total source current is equal to the total sink current

$$\sum_{i=1}^{n} d_i I_i = -\sum_{i=1}^{n} \bar{d}_i I_i - I_{n+1} \quad (5)$$

and the power supplied by the reference source is all dissipated in the ladder. The power dissipation is thus

$$P = \sum_{i=1}^{n} d_i I_i V_r. \quad (6)$$

Fig. 2 plots the power dissipation of the 4-bit D/A converter as a function of the input code. Except for a trivial case when $D =$

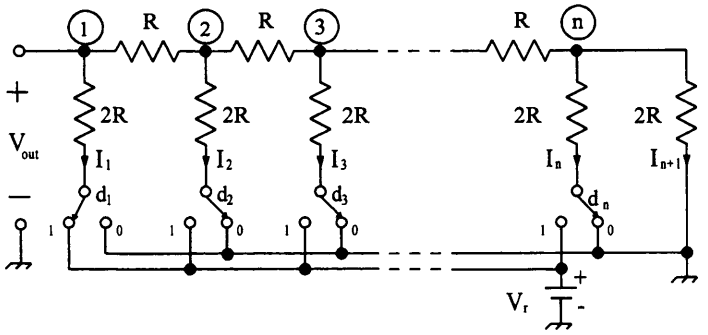

Fig. 1. Voltage-mode R-2R ladder D/A converter.

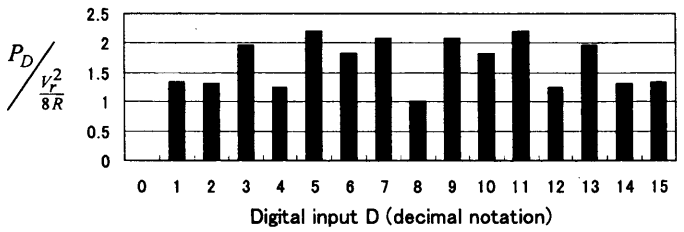

Fig. 2. Normalized power dissipation of a 4-bit R-2R ladder D/A converter as a function of the digital input.

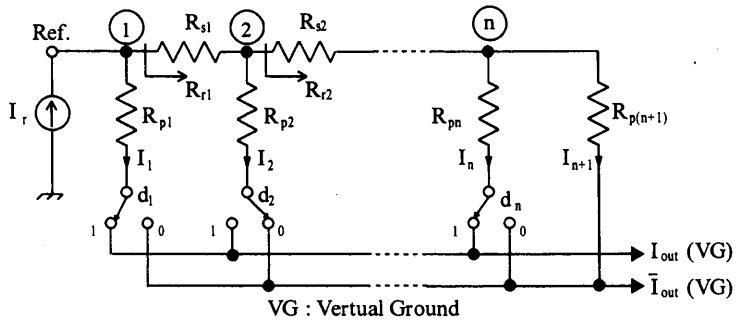

Fig. 3. Current-mode R-2R ladder D/A converter.

0, the plots are symmetrical around $D/2^n = 0.5$, where the dissipation is minimum. This holds true of any R-2R ladder D/A converter. The current flowing through each leg at the minimum power dissipation is given by

$$I_1 = \frac{V_r}{2R} \tag{7}$$

$$I_i = -\frac{1}{2^{i-1}} I_1 \qquad (i = 2, 3, \ldots, n+1). \tag{8}$$

Eq. (8) indicates that if I_1 is replaced by the reference current, the same architecture results in the current-mode D/A converter shown in Fig. 3. This configuration is thus interpreted as the lowest power dissipation counterpart of the R-2R ladder D/A converters.

The current-mode R-2R ladder D/A converter can be characterized by the following procedures [9], [10]. Let ε_i be the resistance mismatch at the node ⓘ

$$\varepsilon_i = \frac{R_{pi} - R_{ri}}{R_{pi} + R_{ri}} \tag{9}$$

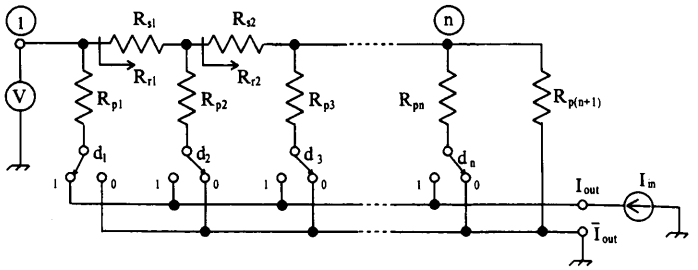

Fig. 4. D/A converter under resistance measurement.

where R_{ri} is the resistance looking toward the right-hand end of the ladder. The current flowing through each leg is then expressed as follows

$$I_i = \frac{I_r}{2^i}(1-\varepsilon_i)\prod_{k=1}^{i-1}(1+\varepsilon_k), \qquad (i = 1, 2, \ldots, n). \tag{10}$$

Introducing the weighting factor

$$w_1 = \tfrac{1}{2}(1-\varepsilon_1) \tag{11}$$

$$w_i = \frac{1}{2^i}(1-\varepsilon_1)\prod_{k=1}^{i-1}(1+\varepsilon_k) \tag{12}$$

we can rewrite (11) in the matrix form

$$\begin{bmatrix} I_1 \\ I_2 \\ \cdot \\ \cdot \\ I_n \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & \cdot & \cdot & 0 \\ 0 & 1 & 0 & \cdot & \cdot & 0 \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ 0 & 0 & 0 & \cdot & \cdot & 1 \end{bmatrix} \begin{bmatrix} w_1 \\ w_2 \\ \cdot \\ \cdot \\ w_n \end{bmatrix} I_r. \tag{13}$$

The matrix representation (13) indicates that the weighting factor, and thereby the mismatch ε_i, can be determined by setting only $d_i = 1$ and measuring I_{out}.

The current measurement described above provides n data for the resistance ratio. An n-bit R-2R ladder D/A converter includes $2n$ resistors. To know each resistance value, n additional data are required. Such data can be obtained by applying a constant current I_{in} to the I_{out} terminal and measuring the voltage at the reference terminal, as shown in Fig. 4. The voltage V_1 when only d_1 is set to 1 and the other bits are set to 0 is given by

$$V_1 = R_{r1} I_{\text{in}}. \tag{14}$$

From V_1 and ε_1, we can know R_{p1} and R_{r1}. Next, the voltage V_2 when only d_2 is set to 1 is given by

$$V_2\left(1 + \frac{R_{s1}}{R_{p1}} + \frac{1-\varepsilon_2}{1+\varepsilon_2}\frac{R_{p2}}{R_{p1}}\right) = \frac{1-\varepsilon_2}{1+\varepsilon_2} R_{p2} I_{\text{in}}. \tag{15}$$

Since R_{r1} given by

$$R_{r1} = R_{s1} + R_{p2}\frac{1-\varepsilon_2}{2} \tag{16}$$

is already known, we can obtain R_{s1} and R_{p2} by (15) and (16). Repeating this process n times, one can measure all the resistance values.

Once the resistance mismatches are known, the integral nonlinearity (INL) of the converter can be easily estimated. Approximating

$$\prod_{k=1}^{i-1}(1+\varepsilon_k) = 1 + \sum_{k=1}^{i-1}\varepsilon_k \tag{17}$$

we can obtain the output current

$$\begin{aligned} I_{\text{out}} &= I_{\text{ideal}} + \Delta I \\ &= \sum_{i=1}^{n} 2^{-i} d_i I_r + \Delta I \end{aligned} \tag{18}$$

where ΔI is the error current due to the resistance mismatch and is given by

$$\begin{aligned} \frac{\Delta I}{I_r} = &-\frac{\varepsilon_1}{2}\left(d_1 - \sum_{k=1}^{n} 2^{-(k-1)} d_k\right) \\ &-\frac{\varepsilon_2}{2^2}\left(d_2 - \sum_{k=3}^{n} 2^{-(k-2)} d_k\right) - \cdots - \frac{\varepsilon_n}{2^n}. \end{aligned} \tag{19}$$

The first-order representation (19) of the error current indicates that INL assumes local maxima at minor carries and maximum at the major carry, as shown in Fig. 5(a). The maximum error current is $2^{-1}\varepsilon_1 I_r$. For the D/A conversion to be accurate down to LSB, the maximum error current should be smaller than $2^{-(n+1)} I_r$. Therefore, $\varepsilon < 2^{-n}$ is required for n-bit resolution.

The other error sources are on-resistances of switches and wire resistances from the ladder to the output terminals. The INLs due to these error sources are also shown in Fig. 5, where an 8-bit D/A converter with the nominal resistance $R = R_s = R_p/2 = 203\ \Omega$ and the resistance mismatch of 0.4% is assumed. Fig. 5(a) shows INL due to resistance mismatch. The profile is asymmetrical with respect to the major carry. The INL profile when the mismatch of on-resistance is present in addition to the resistance mismatch is shown in Fig. 5(b). The on-resistances $R_{\text{on},\,d}$ of those switches which are driven by the digital input d_i are assumed to be 11 Ω while those $R_{\text{on},\,\overline{d}}$ driven by $\overline{d}_i$ are assumed to be 0. It can be seen that INL due to on-resistances is symmetrical with respect to the major carry and assumes the concave-up profile. If $R_{\text{on},\,d} < R_{\text{on},\,\overline{d}}$, then INL assumes the concave-down profile. Fig. 5(c) shows the effect of the wire resistance. The wire resistance R_{out} from the ladder to I_{out} terminal is assumed to be 30 Ω, while that of $R_{\overline{out}}$ to $\overline{I}_{\text{out}}$ terminal is assumed to be 0. The resistance of the wire interconnect loses the symmetry in Fig. 5(a) and (b), and shifts the maximum INL toward LSB if $R_{\text{out}} > R_{\overline{out}}$ and vice versa. These properties of INL profiles can be used to identify the error sources.

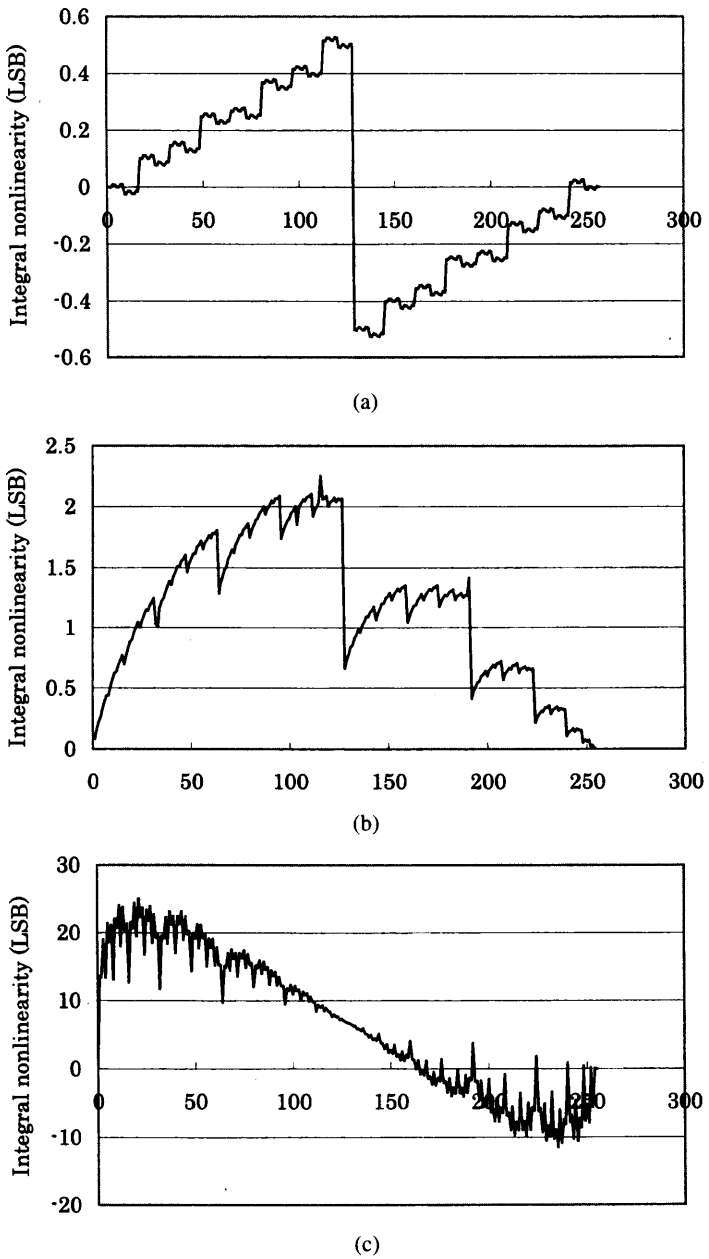

Fig. 5. INL profiles due to mismatches in (a) resistance, (b) on-resistance of switch, and (c) wire resistance.

III. CMOS Ladder D/A Converter

The characterization methods of the R-2R ladder D/A converter described in the previous section have been applied to an 8-bit D/A converter fabricated using the 0.6 μm CMOS process. The circuit diagram of the D/A converter is shown in Fig. 6. The resistor R in Fig. 3 is replaced by the unit nMOS transistor operating in the linear region, and the four unit transistors form the unit cell for 1-bit conversion. Those unit transistors driven by the digital input d_i and $\overline{d}_i$ operate also as switches. The reference current was assumed to be 256 μA.

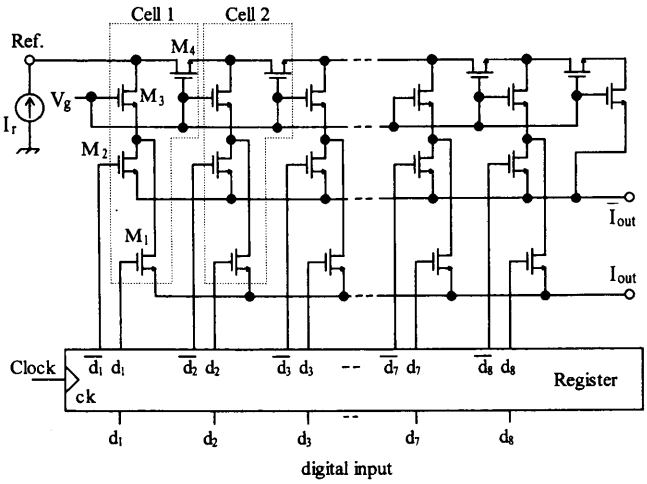

Fig. 6. Circuit diagram of an 8-bit D/A converter fabricated by 0.6 μm CMOS process.

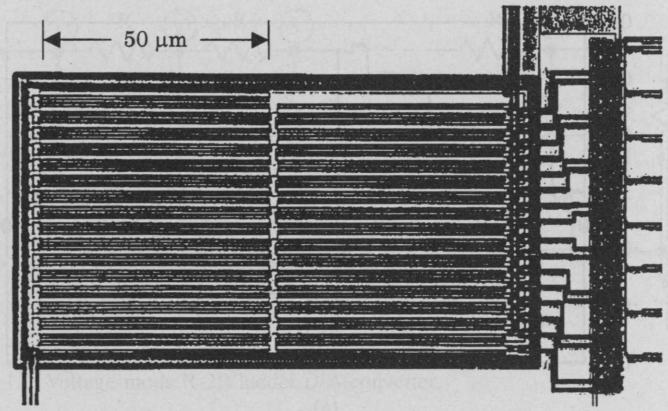

Fig. 7. Microphotograph of the prototype chip.

The drain current I_D of an nMOS transistor operating in the linear region is given by

$$I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS}, \tag{20}$$

where the usual notations are used for transistor parameters. The linear operation is limited to

$$V_{DS} \leq V_{GS} - V_T. \tag{21}$$

The maximum drain current is thus

$$I_{D\,\max} = \mu_n C_{ox}\left(\frac{W}{L}\right)\frac{(V_{GS} - V_T)^2}{2}. \tag{22}$$

The unit transistors in the MSB cell carry the current $I_r/2 = 128\ \mu$A and this current should be smaller than $I_{D\,\max}$.This condition specifies the aspect ratio as follows:

$$\left(\frac{W}{L}\right) \geq 2.2. \tag{23}$$

In deriving (23), the process parameters $\mu_n C_{ox} = 40\ \mu\text{A/V}^2$, $V_T = 0.8$ V, and the bias voltage $V_g = 2.5$ V are assumed.

A much larger aspect ratio than that specified by (23) is preferable to lower the equivalent resistance, thereby the power dissipation, and also to reduce the harmonic distortion when the D/A converter is applied to an attenuator and a multiplier. With this low power and low distortion in mind, three aspect ratios W/L = 200 μm/3 μm, 200 μm/2.4 μm, and 200 μm/1.2 μm are chosen for prototype chips.

Fig. 7 shows a microphotograph of the prototype chip with (W/L) = 200 μm/3 μm. In the central part 33 unit transistors arranged in two columns can be seen forming the ladder stage. It can also be seen that the unit transistor is formed by the parallel connection of 4 transistors with W/L = 50 μm/3 μm. The rightmost part is the register to store the digital input.

Fig. 8 shows the current versus voltage characteristics at the reference node. This result indicates that the unit transistor operates as a linear resistor of 232 Ω over the wide reference current range. Fig. 9 shows the equivalent resistance as a function of the gate length. The linear relation confirms that the aspect ratio linearly scales the equivalent resistance.

Fig. 10 shows the measured transfer characteristics. The transfer characteristics for the source ($I_r = 256\ \mu$A) and sink

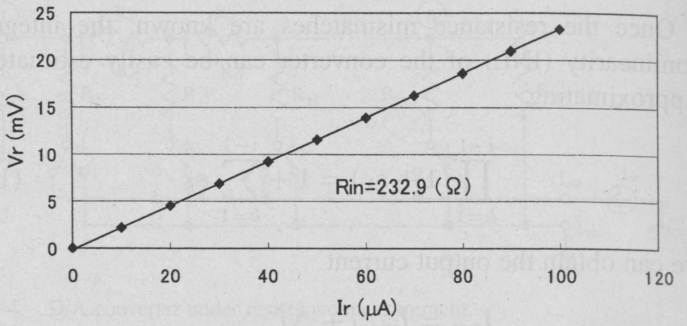

Fig. 8. Current versus voltage characteristics at the reference node.

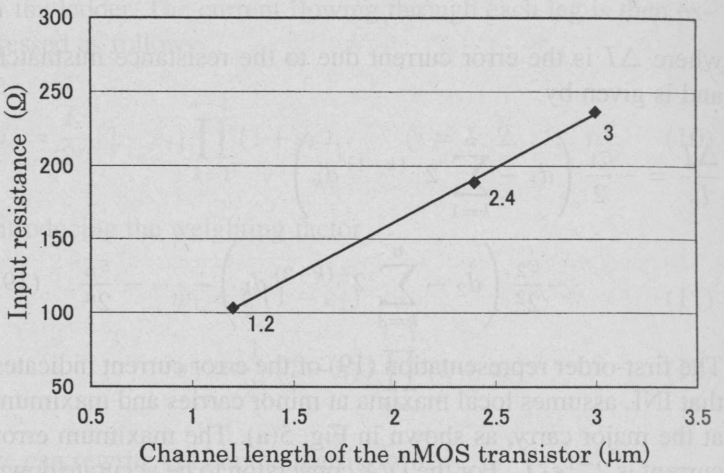

Fig. 9. The equivalent resistance versus the gate length of an nMOS transistor.

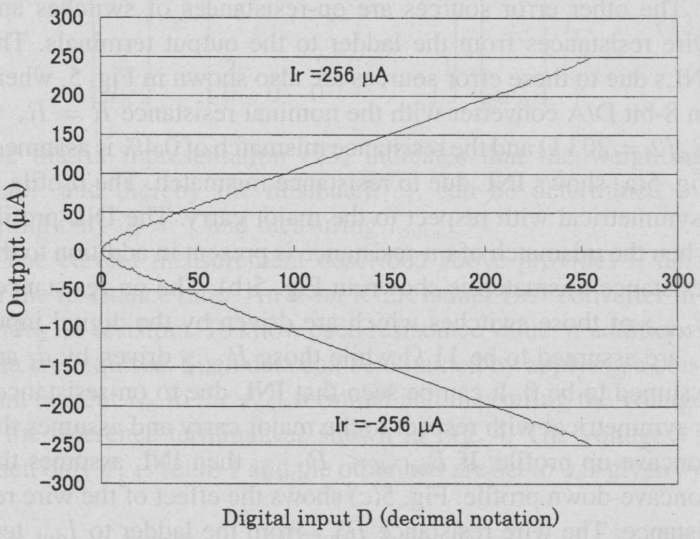

Fig. 10. Transfer characteristics of the prototype D/A converter: W/L = 200 μm/3 μm.

($I_r = -256\ \mu$A) references are symmetrical, which proves that the ladder D/A converter is available also for an attenuator and a multiplier. Fig. 11 shows the INL obtained from the measured transfer characteristics. Comparing the profiles with those shown in Fig. 5, it can be found that the dominant error source is the wire resistance. The best-fit simulation using Spice has estimated that the wire resistances from the ladder to the I_{out} and $\overline{I}_{\text{out}}$ pads are 8.8 Ω and 12.8 Ω, respectively. These values are quite reasonable in view of the fine-line CMOS process.

Performances of the CMOS ladder itself are evaluated by excluding the effect of the wire resistances. Table I lists equivalent

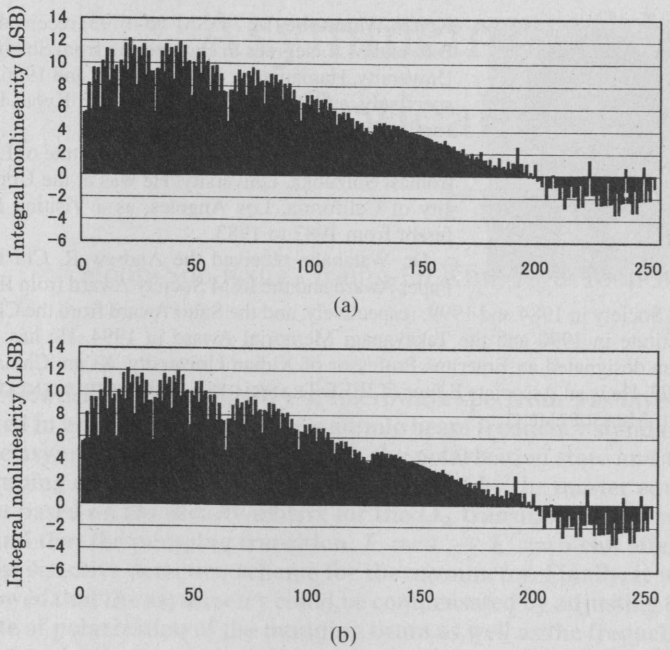

Fig. 11. Integral nonlinearity of the prototype D/A converter: (a) $I_r = 256\ \mu$A; (b) $I_r = -256\ \mu$A. W/L = 200 μm/3 μm.

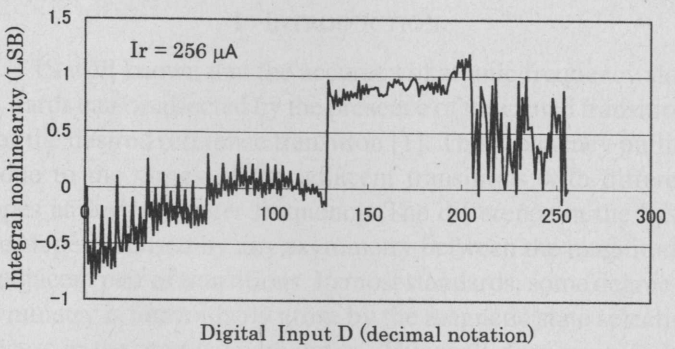

Fig. 12. Integral nonlinearity of the CMOS ladder. W/L = 200 μm/3 μm.

TABLE I
RESISTANCES AND RESISTANCE MISMATCHES OF THE FIRST FOUR MSB CELLS OF THE PROTOTYPE CONVERTER. W/L = 200 μm/3 μm

Cell No.	Resistance (Ω)		Mismatch
	R_p	R_s	ε (%)
1	438.6	442.6	-0.45
2	447.4	455.6	-0.91
3	413.5	429.4	-1.9
4	344.9	371	-3.6

resistances and mismatches in the first four MSB cells evaluated by the current and voltage measurements described in the previous section. R_p includes the resistance of the switch transistor. The deviation of the equivalent resistance from the nominal value, and the mismatch increase with the latter cell. This is due to the accumulated uncertainty in the wire resistances. The 0.4% resistance mismatch in the first cell, which dominates INL of the CMOS ladder, suggests that INL be 1 LSB. Fig. 12 shows the practical INL of the CMOS ladder. Comparing the profile with that shown in Fig. 5(b), it is clear that the mismatch in switch on-resistance also degrades INL to 1.2 LSB.

IV. CONCLUSION

Current and voltage measurements to characterize the R-2R ladder and the INL profiles to identify the error sources of the ladder-based D/A converter were described. These techniques were applied to the 8-bit CMOS ladder D/A converter fabricated using the 0.6 μm CMOS process. The measured results have indicated that the dominant error source of the prototype converter is the wire resistance from the CMOS ladder stage to the ponding pad, and the INL of the CMOS ladder is 1.2 LSB.

The prototype converter was fabricated by fully digital-compatible process. The circuit configuration is simple, and the device count is small. The analog bandwidth extends up to 100 MHz, and the total harmonic distortion is less than 0.1%. Owing to these distinct features, the CMOS ladder D/A converter described herein is quite useful for high-speed D/A conversion and video signal processing in a mixed analog and digital ASIC. Improving INL by lowering the wire resistances is a future work.

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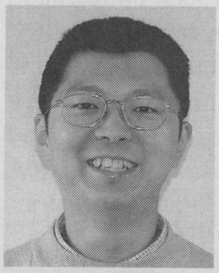

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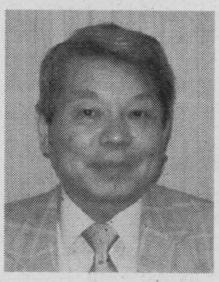

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